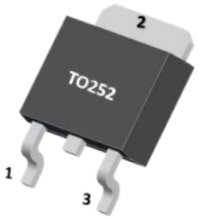
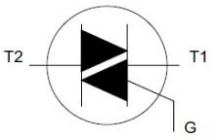
■ GENERAL DESCRIPTION

Glass passivated, sensitive gate triac in a plastic envelope, intended for use in general purpose bidirectional switching and phase control aplications, where high sensitivity is required in all four quadrants.





Pin1:T1 Pin2:T2 Pin3:G

■ ABSOLUTE MAXIMUM RATINGS (TC=25°C, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITION	VALUE	UNIT
V_{DRM}	Repetitive Peak off-state voltage	T_j=25℃	800	V
$I_{T(RMS)}$	RMS on-state current full sine wave; Tmb ≤107°C		4	A
I_{TSM}	Non-repetitive peak on-state current (Full sine wave TJ = 25°C prior to surge)	t = 20ms	25	A
		t = 16.7ms	27	A
I^2t	I^2t for fusing	t=10ms	3.1	A^2S
dI/dt	Repetitive rate of rise of on-state current after triggering I_{TM} = 6 A; I_G = 0.2A;dI_G /dt = 0.2A/μs	T2+, G+	50	A/μs
		T2+, G -	50	A/μs
		T2-, G -	50	A/μs
		T2-, G+	10	A/μs
V_{GM}	Peak gate voltage		5	V
I_{GM}	Peak gate current		2	A
P_{GM}	Peak gate Power		5	W
$P_{G(AV)}$	Average gate Power(over any 20ms period)		0.5	W
Tj	Operating Junction Temperature		125	℃
Tstg	Storage Temperature		-40 to +150	℃

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2.The device is guaranteed to meet performance specification within 0°C~70°C operating temperature range and assured by design from –20°C ~ 85°C.

3.Although not recommended, off-state voltages up to 800V may be applied without damage, but the traic may switch to the on-state. The rate of rise of current should not exceed 3A/μs.

■ THERMAL RESISTANCES

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	RθJA	62.5	℃/W
Junction to Case	TO-252	RθJC	2.6	℃/W

■ ELECTRICAL CHARACTERISTICS(Tj=25℃ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	T2+ G+	V_D=12V I_T=0.1A		2.5	10	mA
		T2+ G-			4	10	mA
		T2- G-			5	10	mA
		T2- G+			11	25	mA
Latching Voltage	I_L	T2+ G+	V_D=12V, I_T=0.1A		3.0	15	mA
		T2+ G-			10	20	mA
		T2- G-			2.5	15	mA
		T2- G+			4.0	20	mA
Holding current	I_H	V_D=12V, I_{GT}=0.1A			2.2	15	mA
On-State Voltage	V_T	I_T=5A			1.4	1.7	V
Gate Trigger Voltage	V_{GT}	V_D=12V, I_T=0.1A			0.7	1.5	V
		V_D=400V, I_T=0.1A, T_J=125°C		0.25	0.40		
Off-state leakage current	I_D	V_D=$V_{DRM(max)}$, Tj=125°C			0.1	0.5	mA

DYNAMIC CHARACTERISTICS(TJ=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off-state Voltage	dV_D/dt	V_{DM}=67%$V_{DRM(max)}$,T_j=125° Exponential waveform,Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t_{gt}	I_{TM}=20A,V_D=V_{DRM},I_G=0.1A dI_G/dt=5A/μs		2		μs

■ TYPICAL CHARACTERISTICS（1）

Fig 1. Maximum On-State Dissipation, P_{tot} Versus Rms On-state Current, $I_{T(RMS)}$ where α=conduction angle.

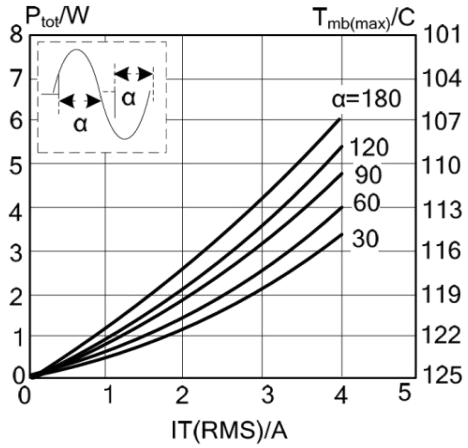


Fig 2. Maximum Permissible Non-repetitive Peak On-state Current, ITSM, Versus Pulse Width tp For Sinusoidal Currents, tp≤ 20ms

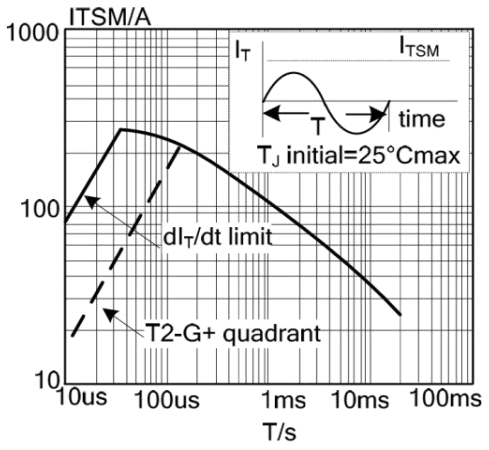


Fig 3. Maximum Permissible Non-repetitive Peak On-state Current, I_{TSM}, Versus Number Of Cycles, For Sinusoidal Currents, f=50Hz.

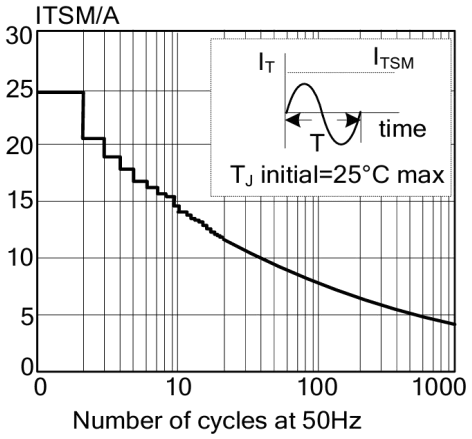


Fig 4. Maximum Permissible Rms Current, $I_{T(RMS)}$ Versus Mounting Base Temperature, T_{mb}

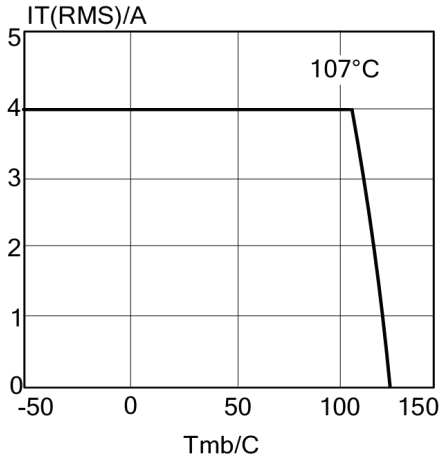


Fig 5. Maximum Permissible Repetitive Rms On-State Current , $I_{T(RMS)}$,Versus Surge Duration, For Sinusoidal Currents, f=50HZ, Tmb≤ 107°C

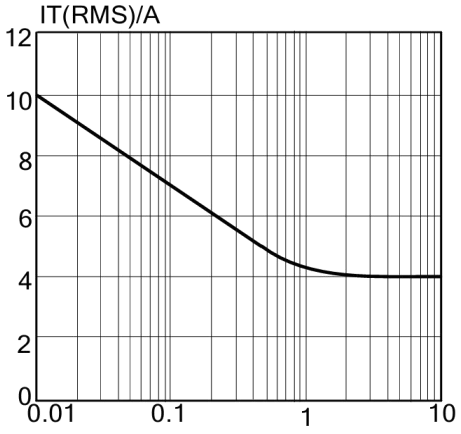
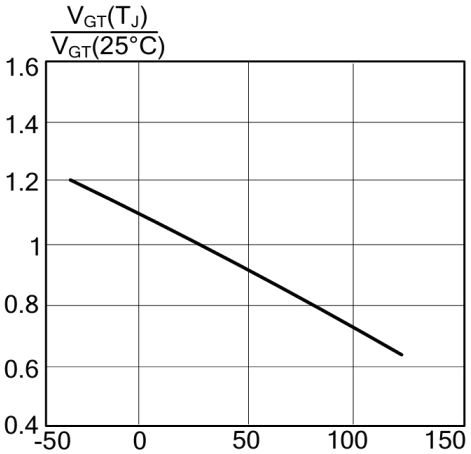


Fig 6. Normalised Gate Trigger Voltage, $V_{GT}(T_J)/V_{GT}(25°C)$, Versus Junction Temperature, T_J



■ TYPICAL CHARACTERISTICS（Con.t）

Fig 7. Normalised Gate Trigger Current, $I_{GT}(T_J)/I_GT(25°C)$, VersusJunction Temperature, T_J

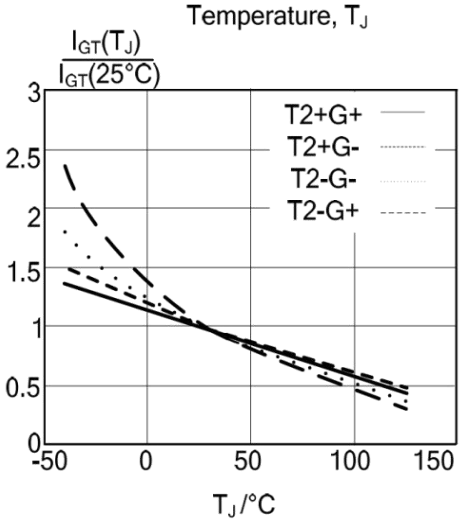


Fig 8. Normalised Latching Current, $I_L(T_J)/I_L(25°C)$ Versus Junction Temperature, T_J

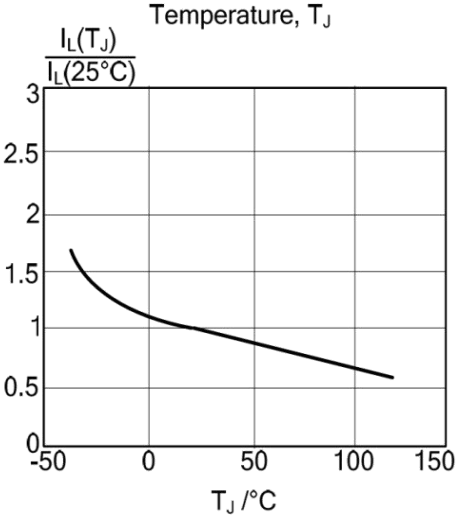


Fig 9. Normalised Holding Current, $I_H(T_J)/I_H(25°C)$, versus junction temperature, T_J

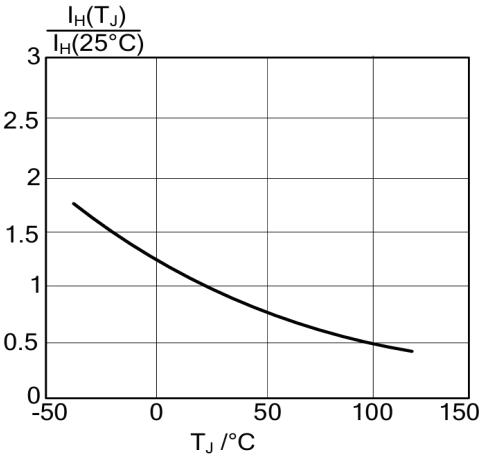


Fig 10. Typical And Maximum On-state Characteristic

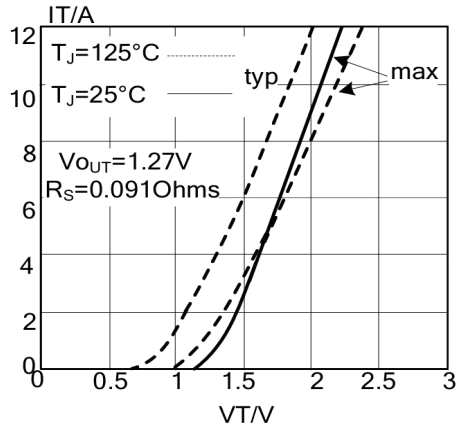


Fig 11. Transient Thermal Impedance Zthj-mb,Versus Pulse Width tp

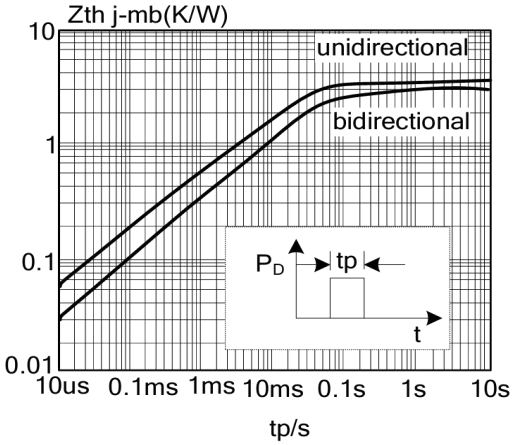
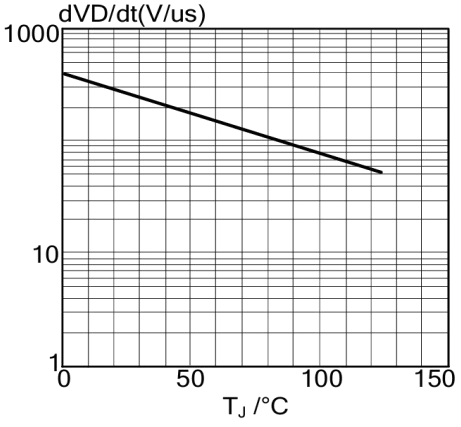
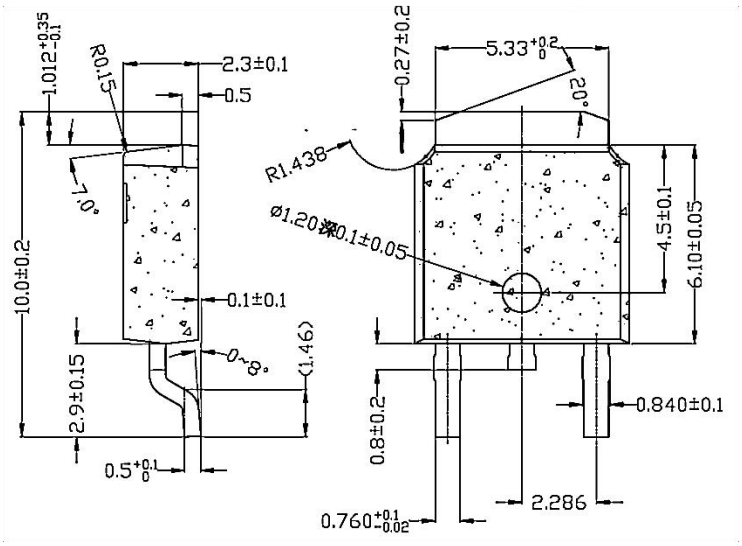
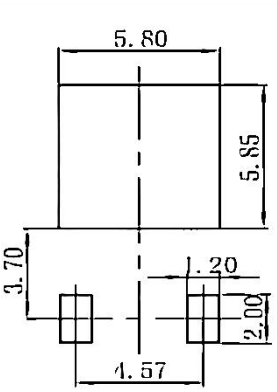


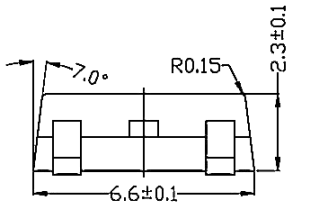
Fig 12. Typical Critical Rate Of Rise Of Off-satate Voltage, dV_D/dt Versus Junction Temperature, T_J



■ TO-252 PACKAGE OUTLINE DIMENSIONS







Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.