

# REALTEK

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## **RTL8380M-VB-CG**

**MULTI-LAYER MANAGED 10\*10/100/1000M-PORT SWITCH CONTROLLER**

## **RTL8382M-VB-CG**

**MULTI-LAYER MANAGED 28\*10/100/1000M-PORT SWITCH CONTROLLER**

## **RTL8382L-VB-CG**

**UN-MANAGED 26\*10/100/1000M-PORT SWITCH CONTROLLER**

## **DATASHEET**

**(CONFIDENTIAL: Development Partners Only)**

**Rev. 1.0**

**20 January 2014**

**Track ID: JATR-8275-15**



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## **USING THIS DOCUMENT**

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek Ethernet Switch Controllers.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## **REVISION HISTORY**

| <b>Revision</b> | <b>Release Date</b> | <b>Summary</b> |
|-----------------|---------------------|----------------|
| 1.0             | 2014/01/20          | First release. |

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# 1. General Description

The RTL8380M-VB-CG, RTL8382M-VB-CG, and RTL8382L-VB-CG are new generation Gigabit switches supporting Energy Efficient Ethernet (EEE). The RTL8380M-VB is an 10-port 10/100/1000M switch controller, and the RTL8382M-VB is a 28-port 10/100/1000M switch controller. The RTL8382L-VB is a 26-port 10/100/1000M switch controller. All have an 8-port 10/100/1000M Ethernet PHY embedded.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB are provided via a 55nm CMOS process in an LQFP-216 E-PAD package. The Memory interface of the RTL8380M-VB/RTL8382M-VB supports DDR1/DDR2/DDR3 and SPI Flash. The RTL8382L-VB supports only SPI Flash.

The following table lists the main differences between the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB:

| Features        | RTL8380M-VB           | RTL8382M-VB       | RTL8382L-VB            |
|-----------------|-----------------------|-------------------|------------------------|
| Port Capacity   | 8G*UTP + 2*1000Base-X | 24G*UTP + 4GCombo | 24G*UTP + 2*1000Base-X |
| Management Mode | Managed Mode Only     | Managed Mode Only | Unmanaged Mode Only    |
| DDR1/2/3        | Yes                   | Yes               | No                     |
| SPI Flash       | Yes                   | Yes               | Yes                    |
| EEPROM Config.  | Yes                   | Yes               | Yes                    |
| Internal CPU    | Yes                   | Yes               | Yes                    |

The RTL8380M-VB supports two-pairs of SGMII/1000Base-X.

The RTL8382M-VB/RTL8382L-VB support four pairs of serially connected QSGMII interface ports to connect to two Octal Gigabit PHYs (RTL8218B). The RTL8382M-VB also supports one serially connected QSGMII interface port to connect to 1 Quad Gigabit PHY (RTL8214FC).

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB have an embedded 500MHz MIPS-4KEc CPU that supports a 32MByte (max.) SPI flash (Only the RTL8380M-VB/RTL8382M-VB support DDR1/DDR2/DDR3). Two 16C550 compatible UARTs are integrated for low speed serial data, and one E-JTAG is supported for on-chip debugging.

There are 8K entries in the 4-way hash L2 table for MAC address learning and searching. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports two hash algorithms. An independent 512-entry Multicast table supports Layer 2 and IP multicast functions.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB has a 4K-entry VLAN table for 802.1Q port-based, protocol-and-port-based, 802.1Q-based, IP-subnet-based, and ACL Rules-based VLAN operation to separate logical connectivity from physical connectivity. Support is provided for IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (both Independent and Shared VLAN Learning) for flexible network topology architecture. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports a 1.5K-entry Access Control List (ACL) that parses various protocol packet types and performs configurable actions, e.g., Permit/Drop, redirect, and traffic policing.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports per-port ingress/egress bandwidth control and per-queue egress bandwidth control. It has 8 physical queues in each port. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provides three types of packet scheduling; SP (Strict Priority), WFQ

(Weighted Fair Queuing), and WRR (Weighted Round Robin). Each queue provides a leaky-bucket to shape the incoming traffic into the average rate behavior.

Port-based 802.1X and MAC-based 802.1X authentication prevent unauthorized users from accessing internal servers. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports port isolation to enhance port security. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB also supports a 4-set port mirror configuration to mirror ingress and egress traffic. For network management purposes, complete MIB counter support reflects the switch status in real time. Support is provided for link aggregation to increase link redundancy, and increase linear bandwidth.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB adopts advanced technologies such as Realtek Cable Test (RTCT), Automatic loop detection and prevention (RLPP/RLDP), Attack Prevention, and MAC Address Learning Constraints.

## 2. Features

### ■ Hardware Interface

- ◆ RTL8380M-VB
  - 10-port Gigabit wire speed forwarding capability
  - Supports 8-port 10/100/1000M Ethernet PHY
  - Supports two pairs of SGMII/1000Base-X
- ◆ RTL8382M-VB/RTL8382L-VB
  - RTL8382M-VB provides 28-port Gigabit wire speed forwarding capability
  - RTL8382L-VB provides 26-port Gigabit wire speed forwarding capability
  - Supports 8-port 10/100/1000M Ethernet PHY
  - Supports 4-pairs of QSGMII to connect to external 8-port 10/100/1000M Ethernet PHYs
  - RTL8382M-VB supports an extra 1 pair of QSGMII or 2 pairs of SGMII/1000Base-X
  - RTL8382L-VB supports 2 pairs of SGMII/1000Base-X
- ◆ DRAM and Flash Interface
  - RTL8380M-VB/RTL8382M-VB support one 8-bit 128MByte DDR1/DDR2 or one 8-bit 256MByte DDR3 for internal CPU
  - Supports one 32MByte SPI flash interface
- ◆ Embedded MIPS-4KEc with MMU
  - MIPS32 instruction set and 5-stage pipeline
  - 500MHz CPU clock rate
  - 16KByte I-Cache and 16KByte D-Cache
  - Built-in 128KByte SRAM
  - 32 Translation Look-aside Buffer (TLB) entries

- Two UART interfaces to control the internal CPU via a Command Line Interface (CLI)

- ◆ Supports EJTAG interface
- ◆ I2C and slave SPI interface for external master interface to access internal registers

### ■ L2 VLAN Function

- ◆ Supports IVL, SVL, and IVL/SVL
- ◆ Supports IEEE 802.1Q VLAN
  - 4K-entry VLAN Table
  - Port-based VLAN
  - Port-and-protocol-based VLAN
  - ACL-based VLAN
  - Supports up to 64 spanning tree instances for MSTP (IEEE 802.1s), RSTP, and STP
- ◆ Supports flexible Q-in-Q and VLAN Tag function

### ■ L2 MAC Function

- ◆ 4.1 Mbit SRAM Packet Buffer
- ◆ Packet length of 10000Bytes
- ◆ 8K-entry L2 MAC table with 4-way hashing algorithm
- ◆ Independent 512-entry L2/IP Multicast table for multicast function
- ◆ 2-hash algorithm selection for L2 table searching/learning
- ◆ Aging timer range from 0.2s to 1600000s
- ◆ Supports IGMPv1/2/3 and MLDv1/2 snooping
- ◆ Supports Reserved Multicast Addresses processing
- ◆ Limited learned L2 MAC entry on each port and each VLAN

## ■ L2 Miscellaneous Functions

- ◆ Supports broadcast, multicast, unknown-multicast, and unknown-unicast packet suppression control
- ◆ Software supports IEEE 802.1x,
- ◆ Supports Port Mirroring
  - Supports 4-sets of port mirrors
  - Flow-based mirror function
  - RSPAN function for remote mirroring
- ◆ Supports Link Aggregation (IEEE 802.3ad) for 8 groups of link aggregators with up to 8 ports per-group
- ◆ Port isolation function to enhance port security
- ◆ Attack Prevention
  - Land attack
  - Blat attack
  - TCP control flag attack
  - Ping attack
  - Packet length attack
- ◆ Supports Automatic loop detection and isolation (RLPP/RLDP)

## ■ Access Control List (ACL) Function

- ◆ 1.5K-entry ACL table
- ◆ L2/L3/L4 format (e.g., DMAC, SMAC, and Ether-Type)
- ◆ IPv6 Parsing
- ◆ Per-flow traffic policing
- ◆ 16-entry VID range checking
- ◆ 8-entry IPv4 or 2-entry IPv6 range checking
- ◆ 256 leaky-buckets for flow traffic policing; in 16Kbps steps up to 1Gbps maximum
- ◆ 256 log counters to enhance MIB count functionality

- ◆ Supports multiple actions
- ◆ Supports L3 Unicast Routing, 512 next hop MAC Support

## ■ QoS Functions

- ◆ 8 physical queues per port
- ◆ Strict Priority (SP) and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
- ◆ QoS remarking for 802.1p and DSCP (includes IPv4/IPv6)
- ◆ Supports average packet rate control leaky-bucket per queue, in 16Kbps steps up to 1Gbps maximum
- ◆ Ingress port bandwidth control, in 16Kbps steps up to 1Gbps maximum
- ◆ Egress port bandwidth control, in 16Kbps steps up to 1Gbps maximum

## ■ EAV, 1588v2

## ■ Cable Diagnostics (RTCT)

## ■ IEEE 802.3az Energy Efficient Ethernet (EEE)

## ■ MIB Functions

- ◆ Ethernet-like MIB (RFC 3635)
- ◆ Interface Group MIB (RFC 2863)
- ◆ RMON (RFC 2819)
- ◆ Bridge MIB (RFC 1493)
- ◆ Bridge MIB Extension (RFC 2674)

## ■ Others

- ◆ 55nm CMOS process
- ◆ 3.3V/1.1V dual power input
- ◆ LQFP216 E-PAD package

### 3. System Applications

#### 3.1. *RTL8380M-VB: Managed 8\*1000M UTP+2\*1000Base-X Switch*

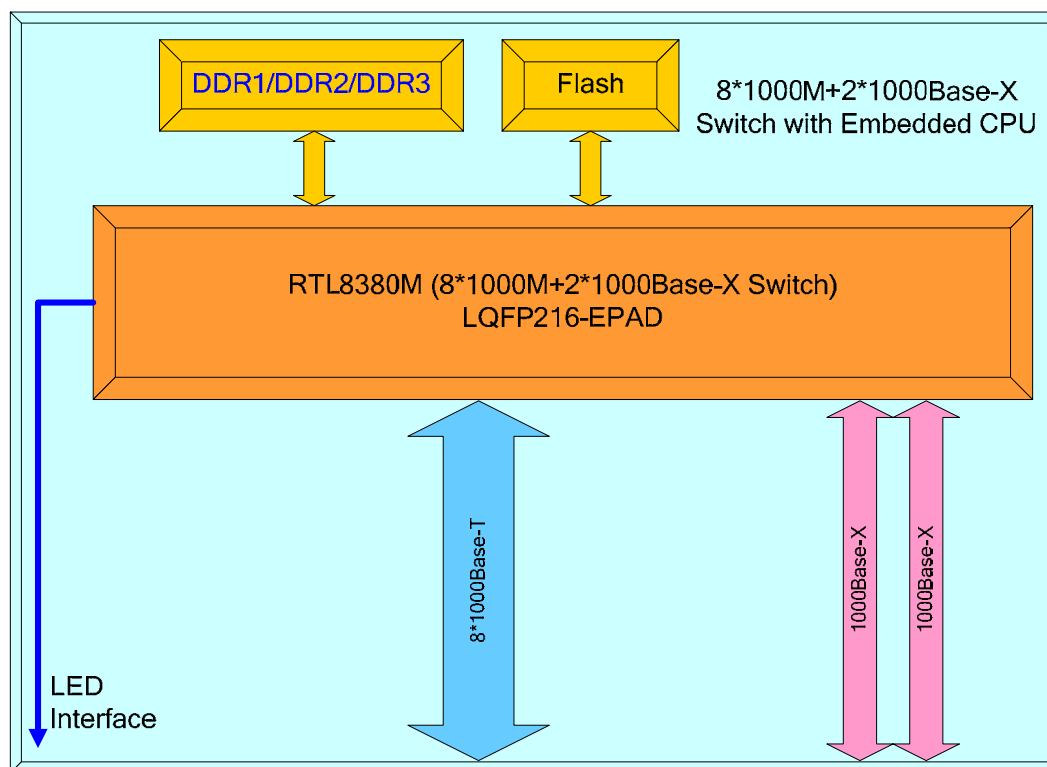


Figure 1. Managed 8\*1000M UTP+2\*1000Base-X Switch



## 3.2. *RTL8382M-VB: Managed 28\*1000M Switch via RTL8218B PHY*

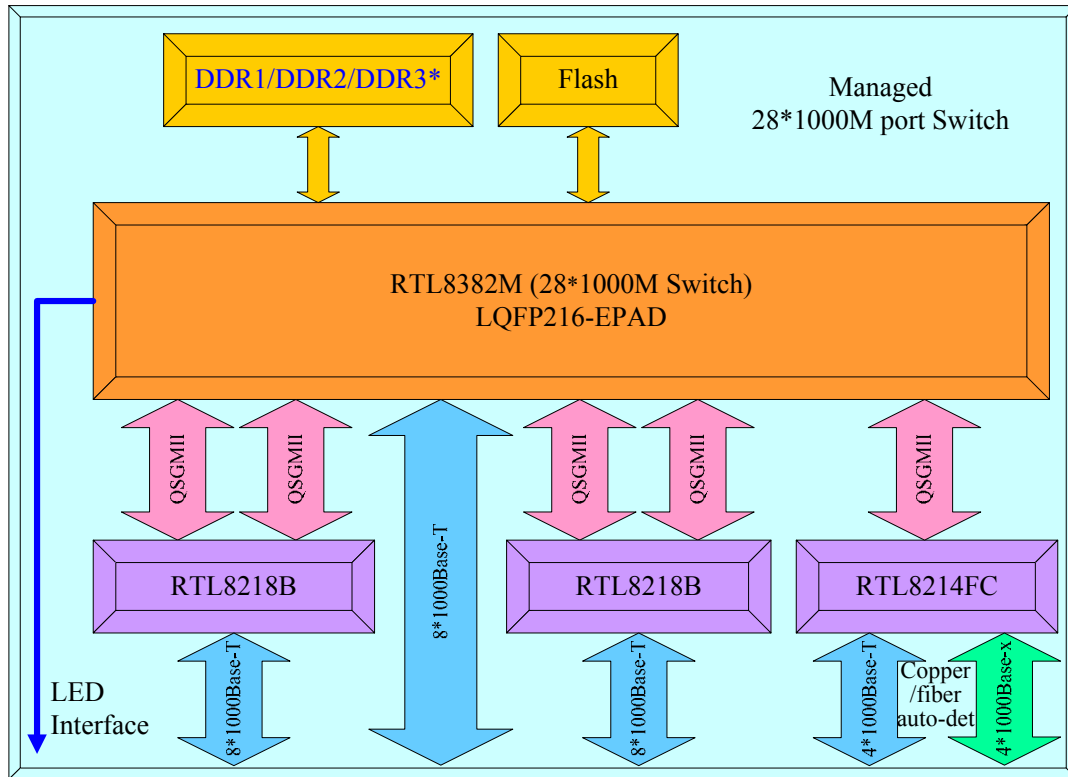


Figure 2. Managed 28\*1000M Switch via RTL8218B PHY



### 3.3. *RTL8382M-VB: Managed 20\*1000M UTP+4\*1000M Combo Switch*

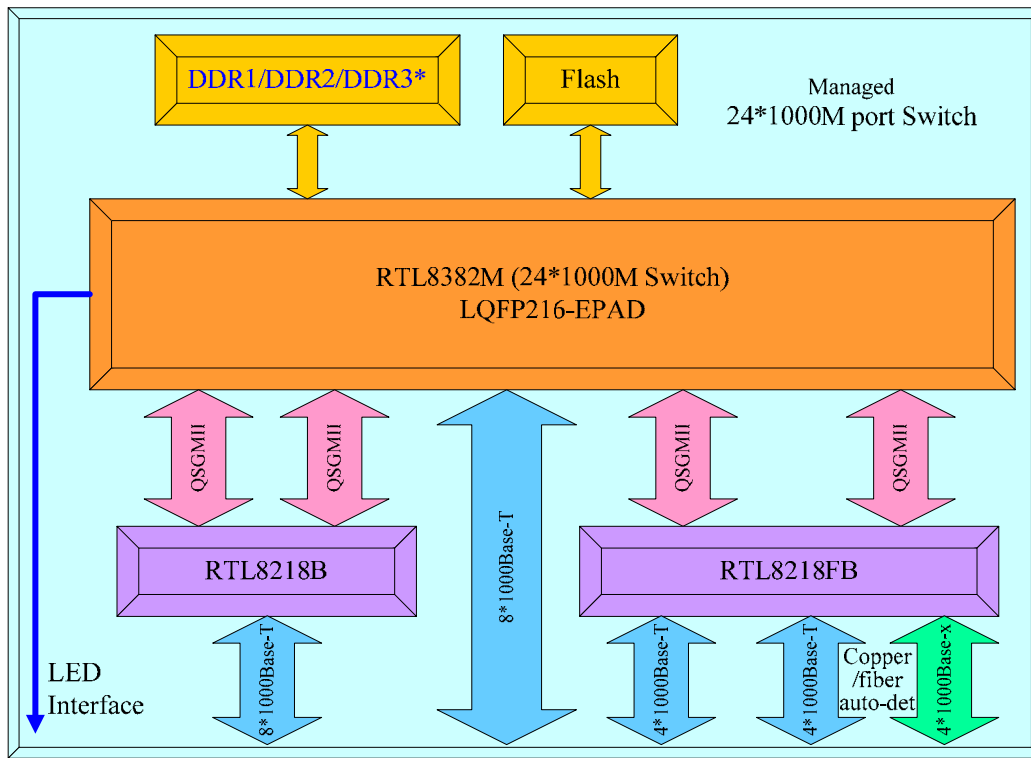
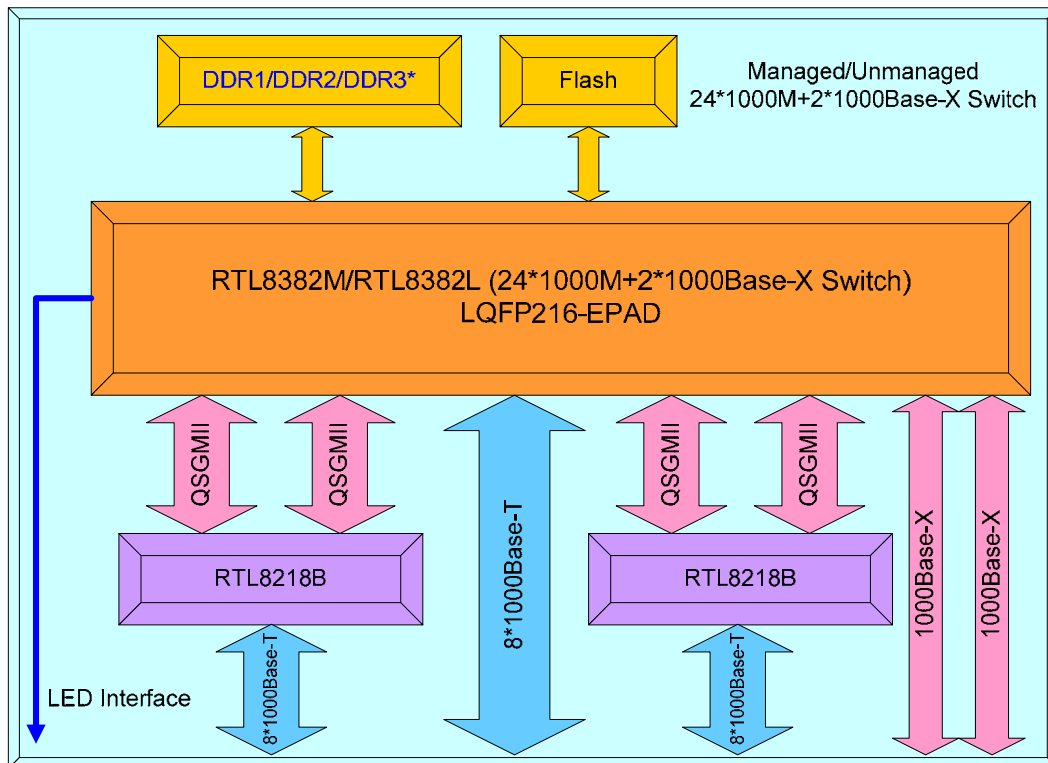


Figure 3. Managed 20\*1000M UTP+4\*1000M Combo Switch



### 3.4. *RTL8382M-VB/RTL8382L-VB: Managed/Unmanaged 24\*1000M UTP+2\*1000Base-X Switch*



Note: Only the RTL8382M supports DDR1/DDR2/DDR3.

**Figure 4. Managed/Unmanaged 24\*1000M UTP+2\*1000Base-X Switch**

## 4. Block Diagrams

### 4.1. RTL8380M-VB Block Diagram

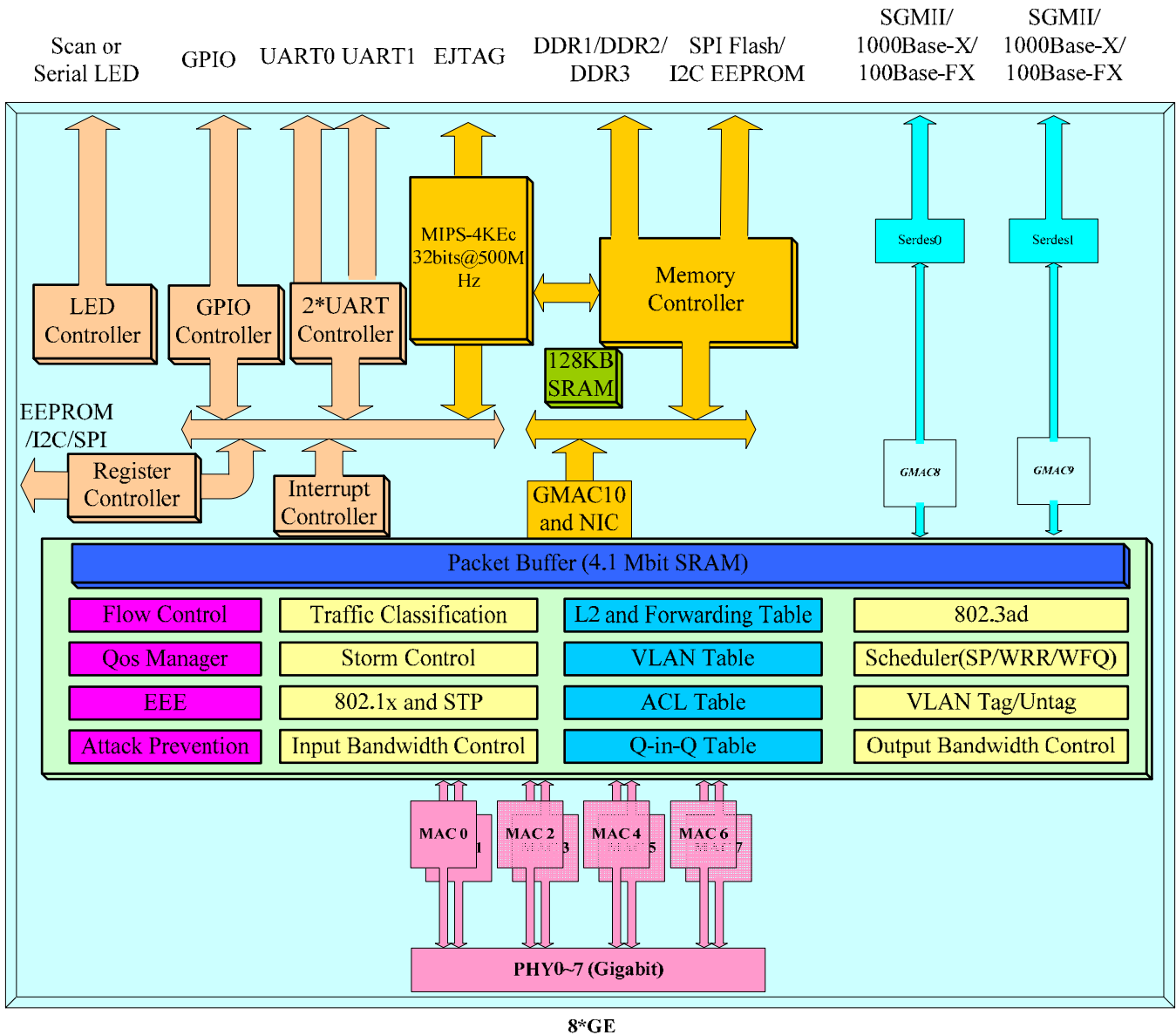


Figure 5. RTL8380M-VB Block Diagram

## 4.2. RTL8382M-VB Block Diagram

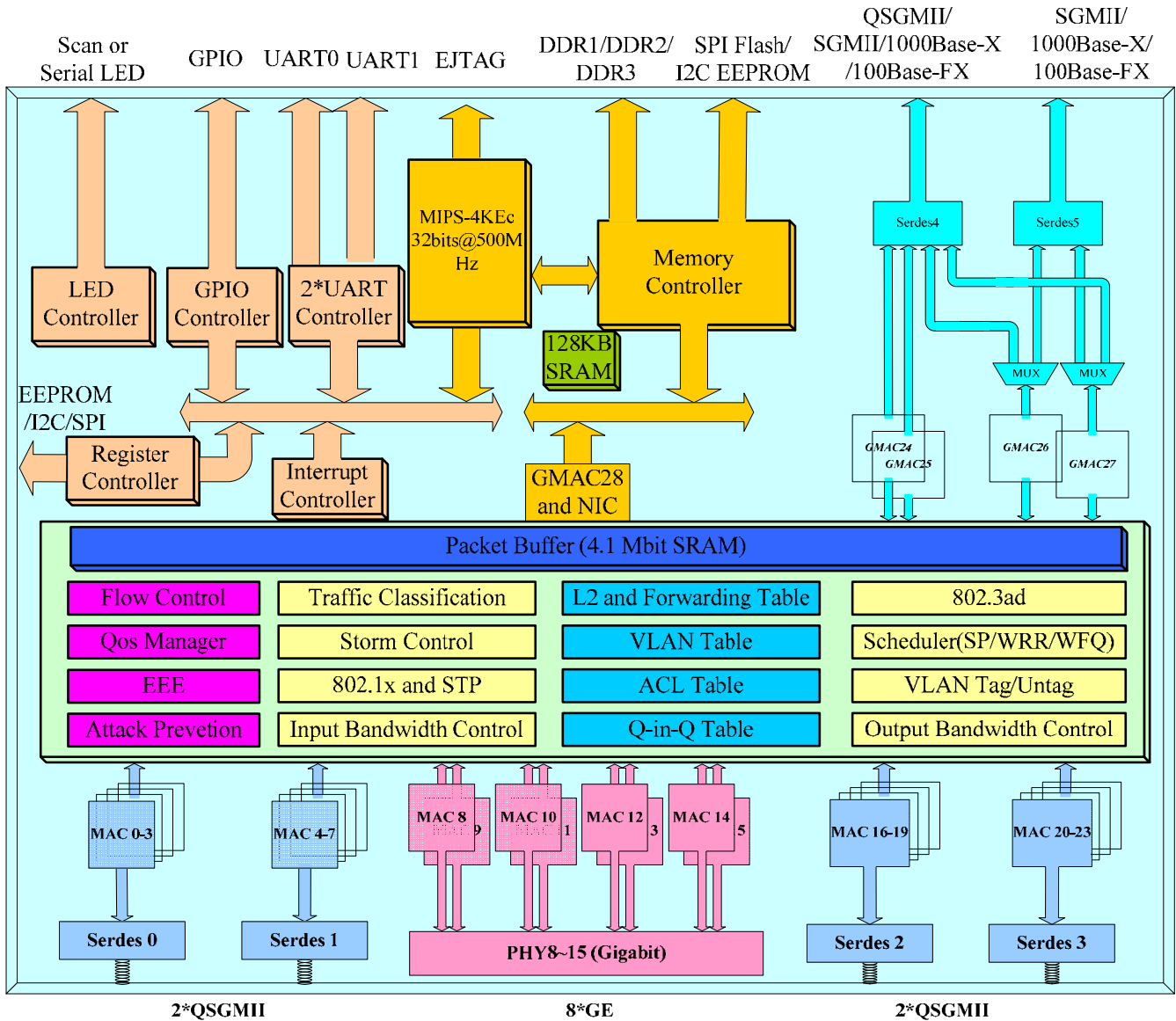


Figure 6. RTL8382M-VB Block Diagram

### 4.3. RTL8382L-VB Block Diagram

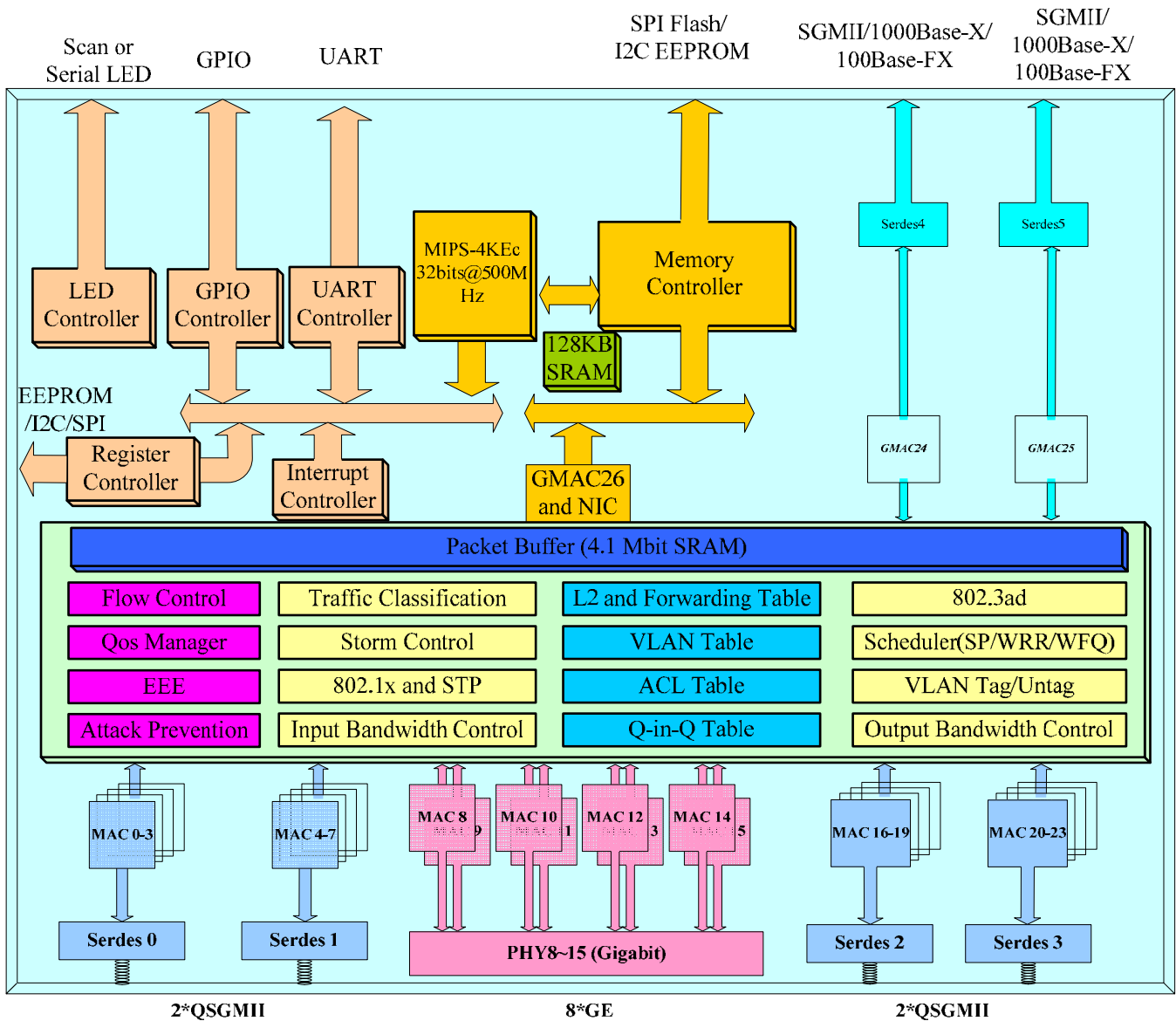
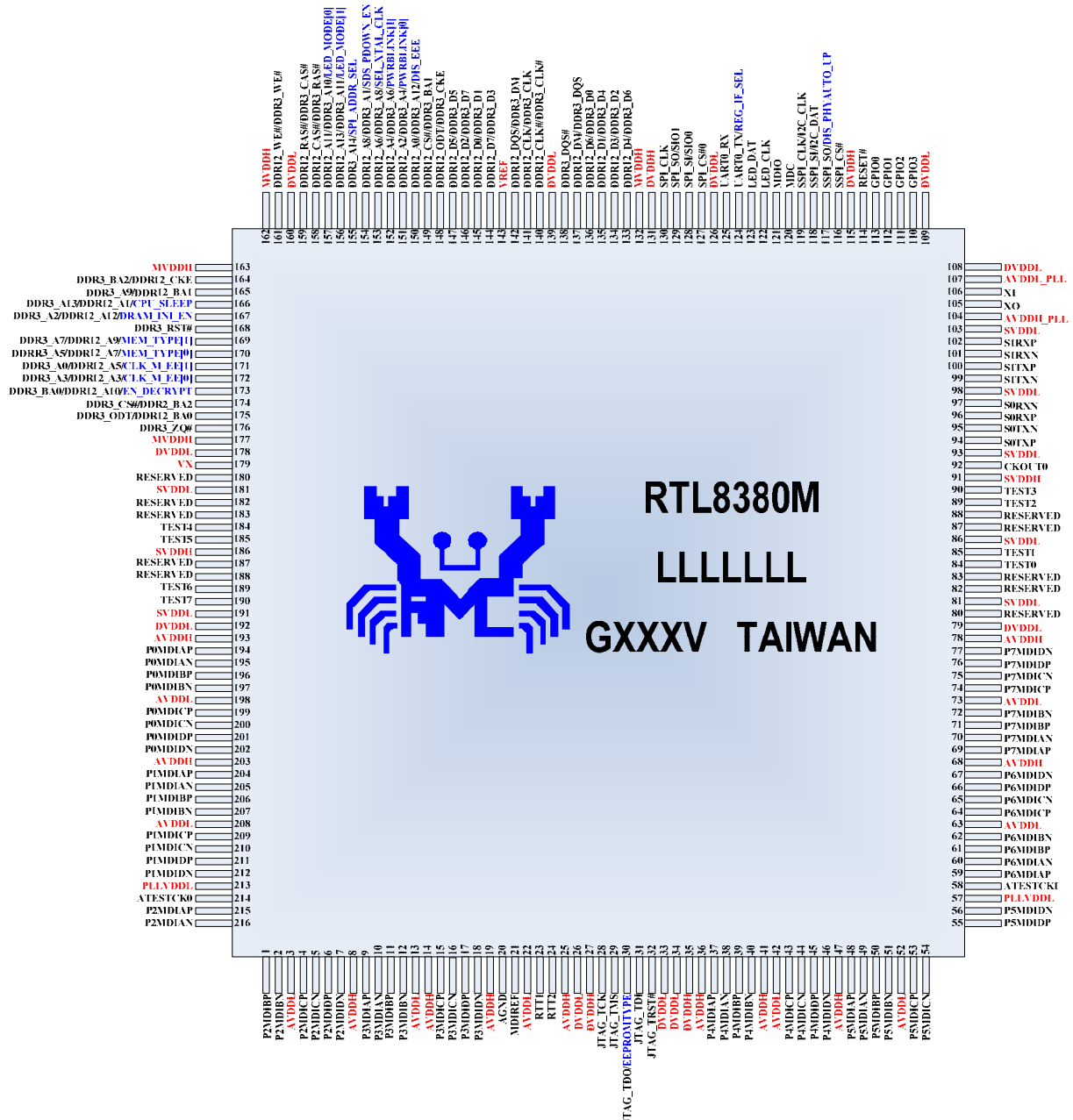


Figure 7. RTL8382L-VB Block Diagram

## 5. Pin Assignments and Description (RTL8380M-VB)

### 5.1. Pin Assignments Figure (RTL8380M-VB)



### 5.2. Package Identification

Green package is indicated by a 'G' in 'GXXXX' (Figure 8). The version number is shown in the location marked 'V'.

### 5.3. Pin Assignments Table Codes (RTL8380M-VB)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

|                                                                                         |                                                                                          |
|-----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
| I: Input Pin                                                                            | AI: Analog Input Pin                                                                     |
| O: Output Pin                                                                           | AO: Analog Output Pin                                                                    |
| I/O: Bi-Directional Input/Output Pin                                                    | AI/O: Analog Bi-Directional Input/Output Pin                                             |
| P: Digital Power Pin                                                                    | AP: Analog Power Pin                                                                     |
| G: Digital Ground Pin                                                                   | AG: Analog Ground Pin                                                                    |
| I <sub>PU</sub> : Input Pin With Pull-Up Resistor;<br>(Typical Value = 75K $\Omega$ )   | O <sub>PU</sub> : Output Pin With Pull-Up Resistor;<br>(Typical Value = 75K $\Omega$ )   |
| I <sub>PD</sub> : Input Pin With Pull-Down Resistor;<br>(Typical Value = 75K $\Omega$ ) | O <sub>PD</sub> : Output Pin With Pull-Down Resistor;<br>(Typical Value = 75K $\Omega$ ) |

### 5.4. Pin Assignments Table (RTL8380M-VB)

**Table 1. Pin Assignments Table (RTL8380M-VB)**

| Name    | Pin No. | Type | Name                | Pin No. | Type              |
|---------|---------|------|---------------------|---------|-------------------|
| P2MDIBP | 1       | AI/O | AVDDH               | 19      | AP                |
| P2MDIBN | 2       | AI/O | AGND                | 20      | AG                |
| AVDDL   | 3       | AP   | MDIREF              | 21      | AO                |
| P2MDICP | 4       | AI/O | AVDDL               | 22      | AP                |
| P2MDICN | 5       | AI/O | RTT1                | 23      | AI/O              |
| P2MDIDP | 6       | AI/O | RTT2                | 24      | AI/O              |
| P2MDIDN | 7       | AI/O | AVDDH               | 25      | AP                |
| AVDDH   | 8       | AP   | DVDDL               | 26      | DP                |
| P3MDIAP | 9       | AI/O | DVDDH               | 27      | DP                |
| P3MDIAN | 10      | AI/O | JTAG_TCK            | 28      | I/O <sub>PU</sub> |
| P3MDIBP | 11      | AI/O | JTAG_TMS            | 29      | I/O <sub>PU</sub> |
| P3MDIBN | 12      | AI/O | JTAG_TDO/EEPROMTYPE | 30      | I/O <sub>PD</sub> |
| AVDDL   | 13      | AP   | JTAG_TDI            | 31      | I/O <sub>PD</sub> |
| AVDDH   | 14      | AP   | JTAG_TRST#          | 32      | I/O <sub>PU</sub> |
| P3MDICP | 15      | AI/O | DVDDL               | 33      | DP                |
| P3MDICN | 16      | AI/O | DVDDH               | 34      | DP                |
| P3MDIDP | 17      | AI/O | DVDDH               | 35      | DP                |
| P3MDIDN | 18      | AI/O | AVDDH               | 36      | AP                |

| Name     | Pin No. | Type |
|----------|---------|------|
| P4MDIAP  | 37      | AI/O |
| P4MDIAN  | 38      | AI/O |
| P4MDIBP  | 39      | AI/O |
| P4MDIBN  | 40      | AI/O |
| AVDDH    | 41      | AP   |
| AVDDL    | 42      | AP   |
| P4MDICP  | 43      | AI/O |
| P4MDICN  | 44      | AI/O |
| P4MDIDP  | 45      | AI/O |
| P4MDIDN  | 46      | AI/O |
| AVDDH    | 47      | AP   |
| P5MDIAP  | 48      | AI/O |
| P5MDIAN  | 49      | AI/O |
| P5MDIBP  | 50      | AI/O |
| P5MDIBN  | 51      | AI/O |
| AVDDL    | 52      | AP   |
| P5MDICP  | 53      | AI/O |
| P5MDICN  | 54      | AI/O |
| P5MDIDP  | 55      | AI/O |
| P5MDIDN  | 56      | AI/O |
| PLLVDL   | 57      | AP   |
| ATESTCK1 | 58      | AO   |
| P6MDIAP  | 59      | AI/O |
| P6MDIAN  | 60      | AI/O |
| P6MDIBP  | 61      | AI/O |
| P6MDIBN  | 62      | AI/O |
| AVDDL    | 63      | AP   |
| P6MDICP  | 64      | AI/O |
| P6MDICN  | 65      | AI/O |
| P6MDIDP  | 66      | AI/O |
| P6MDIDN  | 67      | AI/O |
| AVDDH    | 68      | AP   |
| P7MDIAP  | 69      | AI/O |
| P7MDIAN  | 70      | AI/O |
| P7MDIBP  | 71      | AI/O |
| P7MDIBN  | 72      | AI/O |
| AVDDL    | 73      | AP   |
| P7MDICP  | 74      | AI/O |
| P7MDICN  | 75      | AI/O |
| P7MDIDP  | 76      | AI/O |
| P7MDIDN  | 77      | AI/O |

| Name                       | Pin No. | Type              |
|----------------------------|---------|-------------------|
| AVDDH                      | 78      | AP                |
| DVDDL                      | 79      | DP                |
| RESERVED                   | 80      | -                 |
| SVDDL                      | 81      | AP                |
| RESERVED                   | 82      | -                 |
| RESERVED                   | 83      | -                 |
| TEST0                      | 84      | -                 |
| TEST1                      | 85      | -                 |
| SVDDL                      | 86      | AP                |
| RESERVED                   | 87      | -                 |
| RESERVED                   | 88      | -                 |
| TEST2                      | 89      | -                 |
| TEST3                      | 90      | -                 |
| SVDDH                      | 91      | AP                |
| CKOUT0                     | 92      | AO                |
| SVDDL                      | 93      | AP                |
| S0TXP                      | 94      | AO                |
| S0TXN                      | 95      | AO                |
| S0RXP                      | 96      | AI                |
| S0RXN                      | 97      | AI                |
| SVDDL                      | 98      | AP                |
| S1TXN                      | 99      | AO                |
| S1TXP                      | 100     | AO                |
| S1RXN                      | 101     | AI                |
| S1RXP                      | 102     | AI                |
| SVDDL                      | 103     | AP                |
| AVDDH_PLL                  | 104     | AP                |
| XO                         | 105     | AO                |
| XI                         | 106     | AI                |
| AVDDL_PLL                  | 107     | AP                |
| DVDDL                      | 108     | P                 |
| DVDDL                      | 109     | P                 |
| GPIO3                      | 110     | I/O <sub>PD</sub> |
| GPIO2                      | 111     | I/O <sub>PD</sub> |
| GPIO1                      | 112     | I/O <sub>PD</sub> |
| GPIO0                      | 113     | I/O <sub>PD</sub> |
| RESET#                     | 114     | AI                |
| DVDDH                      | 115     | P                 |
| SSPI_CS#                   | 116     | I <sub>PU</sub>   |
| SSPI_SO/<br>DIS_PHYAUTO_UP | 117     | I/O <sub>PD</sub> |
| SSPI_SI/I2C_DAT            | 118     | I/O <sub>PU</sub> |

| Name                              | Pin No. | Type              |
|-----------------------------------|---------|-------------------|
| SSPI_CLK/I2C_CLK                  | 119     | I/O <sub>PU</sub> |
| MDC                               | 120     | O <sub>PU</sub>   |
| MDIO                              | 121     | I/O <sub>PU</sub> |
| LED_CLK                           | 122     | O <sub>PU</sub>   |
| LED_DAT                           | 123     | I/O <sub>PU</sub> |
| UART0_TX/REG_IF_SEL               | 124     | I/O <sub>PD</sub> |
| UART0_RX                          | 125     | I <sub>PD</sub>   |
| DVDDL                             | 126     | P                 |
| SPI_CS#0                          | 127     | I <sub>PU</sub>   |
| SPI_SI/SIO0                       | 128     | I/O <sub>PD</sub> |
| SPI_SO/SIO1                       | 129     | I/O <sub>PD</sub> |
| SPI_CLK                           | 130     | O <sub>PD</sub>   |
| DVDDH                             | 131     | P                 |
| MVDDH                             | 132     | P                 |
| DDR12_D4/DDR3_D6                  | 133     | I/O               |
| DDR12_D3/DDR3_D2                  | 134     | I/O               |
| DDR12_D1/DDR3_D4                  | 135     | I/O               |
| DDR12_D6/DDR3_D0                  | 136     | I/O               |
| DDR12_DM/DDR3_DQS                 | 137     | I/O               |
| DDR3_DQS#                         | 138     | I/O               |
| DVDDL                             | 139     | P                 |
| DDR12_CLK#/DDR3_CLK#              | 140     | O                 |
| DDR12_CLK/DDR3_CLK                | 141     | O                 |
| DDR12_DQS/DDR3_DM                 | 142     | I/O               |
| VREF                              | 143     | P                 |
| DDR12_D7/DDR3_D3                  | 144     | I/O               |
| DDR12_D0/DDR3_D1                  | 145     | I/O               |
| DDR12_D2/DDR3_D7                  | 146     | I/O               |
| DDR12_D5/DDR3_D5                  | 147     | I/O               |
| DDR2_ODT/DDR3_CKE                 | 148     | O                 |
| DDR12_CS#/DDR3_BA1                | 149     | O                 |
| DDR12_A0/DDR3_A12/<br>DIS_EEE     | 150     | I/O               |
| DDR12_A2/DDR3_A4/<br>PWRBLINK[0]  | 151     | I/O               |
| DDR12_A4/DDR3_A6/<br>PWRBLINK[1]  | 152     | I/O               |
| DDR12_A6/DDR3_A8/<br>SEL_XTAL_CLK | 153     | I/O               |
| DDR12_A8/DDR3_A1/<br>SDS_PDOWN_EN | 154     | I/O               |
| DDR3_A14/SPI_ADDR_SEL             | 155     | I/O               |

| Name                               | Pin No. | Type |
|------------------------------------|---------|------|
| DDR12_A13/DDR3_A11/<br>LED/MODE[1] | 156     | I/O  |
| DDR12_A11/DDR3_A10/<br>LED/MODE[0] | 157     | I/O  |
| DDR12_CAS#/DDR3_RAS#               | 158     | O    |
| DDR12_RAS#/DDR3_CAS#               | 159     | O    |
| DVDDL                              | 160     | P    |
| DDR12_WE#/DDR3_WE#                 | 161     | O    |
| MVDDH                              | 162     | P    |
| MVDDH                              | 163     | P    |
| DDR12_CKE/DDR3_BA2                 | 164     | O    |
| DDR12_BA1/DDR3_A9                  | 165     | O    |
| DDR12_A1/DDR3_A13/<br>CPU_SLEEP    | 166     | I/O  |
| DDR12_A12/DDR3_A2/<br>DRAM_INI_EN  | 167     | I/O  |
| DDR3_RST#                          | 168     | O    |
| DDR12_A9/DDR3_A7/<br>MEM_TYPE[1]   | 169     | I/O  |
| DDR12_A7/DDR3_A5/<br>MEM_TYPE[0]   | 170     | I/O  |
| DDR12_A5/DDR3_A0/<br>CLK_M_EE[1]   | 171     | I/O  |
| DDR12_A3/DDR3_A3/<br>CLK_M_EE[0]   | 172     | I/O  |
| DDR12_A10/DDR3_BA0/<br>EN_DECRYPT  | 173     | I/O  |
| DDR2_BA2/DDR3_CS#                  | 174     | O    |
| DDR12_BA0/DDR3_ODT                 | 175     | O    |
| DDR3_ZQ#                           | 176     | O    |
| MVDDH                              | 177     | P    |
| DVDDL                              | 178     | P    |
| VX                                 | 179     | A    |
| RESERVED                           | 180     | AO   |
| SVDDL                              | 181     | AP   |
| RESERVED                           | 182     | AO   |
| RESERVED                           | 183     | AO   |
| TEST4                              | 184     | -    |
| TEST5                              | 185     | -    |
| SVDDH                              | 186     | AP   |
| RESERVED                           | 187     | AO   |
| RESERVED                           | 188     | AO   |
| TEST6                              | 189     | -    |
| TEST7                              | 190     | -    |

| Name    | Pin No. | Type |
|---------|---------|------|
| SVDDL   | 191     | AP   |
| DVDDL   | 192     | P    |
| AVDDH   | 193     | AP   |
| P0MDIAP | 194     | AI/O |
| P0MDIAN | 195     | AI/O |
| P0MDIBP | 196     | AI/O |
| P0MDIBN | 197     | AI/O |
| AVDDL   | 198     | AP   |
| P0MDICP | 199     | AI/O |
| P0MDICN | 200     | AI/O |
| P0MDIDP | 201     | AI/O |
| P0MDIDN | 202     | AI/O |
| AVDDH   | 203     | AP   |
| P1MDIAP | 204     | AI/O |

| Name     | Pin No. | Type |
|----------|---------|------|
| P1MDIAN  | 205     | AI/O |
| P1MDIBP  | 206     | AI/O |
| P1MDIBN  | 207     | AI/O |
| AVDDL    | 208     | AP   |
| P1MDICP  | 209     | AI/O |
| P1MDICN  | 210     | AI/O |
| P1MDIDP  | 211     | AI/O |
| P1MDIDN  | 212     | AI/O |
| PLLVDL   | 213     | AP   |
| ATESTCK0 | 214     | AO   |
| P2MDIAP  | 215     | AI/O |
| P2MDIAN  | 216     | AI/O |
| DGND     | EPAD    | G    |

## 5.5. Pin Descriptions (RTL8380M-VB)

### 5.5.1. 1000M Ethernet PHY MDI Interface Pins

**Table 2. 1000M Ethernet PHY MDI Interface Pins**

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P0MDIAP  | 194     | AI/O | Port 0 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P0MDIAN  | 195     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBP  | 196     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBN  | 197     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICP  | 199     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICN  | 200     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDP  | 201     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDN  | 202     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIAP  | 204     | AI/O | Port 1 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P1MDIAN  | 205     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBP  | 206     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBN  | 207     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICP  | 209     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICN  | 210     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDP  | 211     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDN  | 212     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIAP  | 215     | AI/O | Port 2 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P2MDIAN  | 216     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBP  | 1       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBN  | 2       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICP  | 4       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICN  | 5       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDP  | 6       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDN  | 7       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIAP  | 9       | AI/O | Port 3 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P3MDIAN  | 10      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBP  | 11      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBN  | 12      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICP  | 15      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICN  | 16      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDP  | 17      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDN  | 18      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P4MDIAP  | 37      | AI/O | Port 4 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P4MDIAN  | 38      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBP  | 39      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBN  | 40      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICP  | 43      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICN  | 44      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDP  | 45      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDN  | 46      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIAP  | 48      | AI/O | Port 5 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P5MDIAN  | 49      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBP  | 50      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBN  | 51      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICP  | 53      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICN  | 54      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDP  | 55      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDN  | 56      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIAP  | 59      | AI/O | Port 6 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P6MDIAN  | 60      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBP  | 61      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBN  | 62      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICP  | 64      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICN  | 65      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDP  | 66      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDN  | 67      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIAP  | 69      | AI/O | Port 7 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P7MDIAN  | 70      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBP  | 71      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBN  | 72      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICP  | 74      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICN  | 75      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDP  | 76      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDN  | 77      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

### 5.5.2. SGMII Interface Pins

**Table 3. SGMII Interface Pins**

| Pin Name | Pin No. | Type | Description                                             |
|----------|---------|------|---------------------------------------------------------|
| S0RXP    | 96      | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S0RXN    | 97      | AI   |                                                         |
| S0TXP    | 94      | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S0TXN    | 95      | AO   |                                                         |
| S1RXP    | 102     | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S1RXN    | 101     | AI   |                                                         |
| S1TXP    | 100     | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S1TXN    | 99      | AO   |                                                         |

### 5.5.3. 1000Base-X/100Base-FX Interface Pins

**Table 4. 1000Base-X/100Base-FX Interface Pins**

| Pin Name | Pin No. | Type | Description                                                             |
|----------|---------|------|-------------------------------------------------------------------------|
| S0RXP    | 96      | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S0RXN    | 97      | AI   |                                                                         |
| S0TXP    | 94      | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S0TXN    | 95      | AO   |                                                                         |
| S1RXP    | 102     | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S1RXN    | 101     | AI   |                                                                         |
| S1TXP    | 100     | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S1TXN    | 99      | AO   |                                                                         |

## 5.5.4. DDR1/2 SDRAM Interface Pins

**Table 5. DDR1/2 SDRAM Interface Pins**

| Pin Name      | Pin No.                                                                       | Type | Drive (mA) | Description                                                      |
|---------------|-------------------------------------------------------------------------------|------|------------|------------------------------------------------------------------|
| DDR12_D[7:0]  | 144, 136, 147, 133,<br>134, 146, 135, 145                                     | I/O  | 8          | DDR SDRAM Data Bus.                                              |
| DDR12_A[13:0] | 156, 167, 157, 173,<br>169, 154, 170, 153,<br>171, 152, 172, 151,<br>166, 150 | I/O  | 8          | DDR SDRAM Address Select.                                        |
| DDR2_BA[2]    | 174                                                                           | O    | 8          | DDR SDRAM Bank Address Select.                                   |
| DDR12_BA[1:0] | 165, 175                                                                      | O    | 8          | DDR SDRAM Bank Address Select.                                   |
| DDR12_WE#     | 161                                                                           | O    | 8          | DDR SDRAM Write Enable.                                          |
| DDR12_CKE     | 164                                                                           | O    | 8          | DDR SDRAM Clock Enable.                                          |
| DDR12_RAS#    | 159                                                                           | O    | 8          | DDR SDRAM Row Address Strobe.                                    |
| DDR12_CAS#    | 158                                                                           | O    | 8          | DDR SDRAM Column Address Strobe.                                 |
| DDR12_CS#0    | 149                                                                           | O    | 8          | DDR SDRAM Chip Select 0.                                         |
| DDR2_ODT      | 148                                                                           | O    | 8          | DDR SDRAM On-Die Termination.                                    |
| DDR12_DQS     | 142                                                                           | I/O  | 8          | DDR SDRAM Data Strobe.                                           |
| DDR12_CLK     | 141                                                                           | O    | 8          | DDR SDRAM Clock.<br>CLK and CLK# are differential clock outputs. |
| DDR12_CLK#    | 140                                                                           | O    | 8          | DDR SDRAM Clock.<br>CLK and CLK# are differential clock outputs. |

### 5.5.5. DDR3 SDRAM Interface Pins

**Table 6. DDR3 SDRAM Interface Pins**

| Pin Name      | Pin No.                                     | Type | Drive (mA) | Description                                                                                                                                 |
|---------------|---------------------------------------------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| DDR3_D[7:0]   | 146, 133, 147, 135, 144, 134, 145, 136      | I/O  | 8          | DDR SDRAM Data Bus.                                                                                                                         |
| DDR3_A[14]    | 155                                         | O    | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[13:10] | 166, 150, 156, 157                          | I/O  | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[9]     | 165                                         | O    | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[8:0]   | 153, 169, 152, 170, 151, 172, 167, 154, 171 | I/O  | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_DQS#     | 138                                         | I/O  | 8          | DDR SDRAM Data Strobe.                                                                                                                      |
| DDR3_DQS      | 137                                         | I/O  | 8          | DDR SDRAM Data Strobe.                                                                                                                      |
| DDR3_CLK#     | 140                                         | O    | 8          | DDR SDRAM Clock.                                                                                                                            |
| DDR3_CLK      | 141                                         | O    | 8          | DDR SDRAM Clock.                                                                                                                            |
| DDR3_DM       | 142                                         | I/O  | 8          | DDR SDRAM Data Mask.                                                                                                                        |
| DDR3_CKE      | 148                                         | O    | 8          | DDR SDRAM Clock Enable.                                                                                                                     |
| DDR3_BA[2:1]  | 164, 149                                    | O    | 8          | DDR SDRAM Bank Address Select.                                                                                                              |
| DDR3_BA[0]    | 173                                         | I/O  | 8          | DDR SDRAM Bank Address Select.                                                                                                              |
| DDR3_RAS#     | 158                                         | O    | 8          | DDR SDRAM Row Address Strobe.                                                                                                               |
| DDR3_CAS#     | 159                                         | O    | 8          | DDR SDRAM Column Address Strobe.                                                                                                            |
| DDR3_WE#      | 161                                         | O    | 8          | DDR SDRAM Write Enable.                                                                                                                     |
| DDR3_RST#     | 168                                         | O    | 8          | DDR SDRAM Reset.                                                                                                                            |
| DDR3_CS#      | 174                                         | O    | 8          | DDR SDRAM Chip Select.                                                                                                                      |
| DDR3_ODT      | 175                                         | O    | 8          | DDR SDRAM On-Die Termination.                                                                                                               |
| DDR3_ZQ#      | 176                                         | O    | 8          | DDR SDRAM External Reference Ball for Output Drive Calibration.<br>This ball is tied to an external 240 Ohm resistor, which is tied to GND. |

### 5.5.6. Master Mode SPI Flash Interface Pins

**Table 7. Master Mode SPI Flash Interface Pins**

| Pin Name    | Pin No. | Type              | Drive (mA) | Description                                                                                                                                 |
|-------------|---------|-------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| SPI_CLK     | 130     | O <sub>PD</sub>   | 12         | Serial Clock Output Pin.                                                                                                                    |
| SPI_SO/SIO1 | 129     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip output pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is MSB first.</i> |
| SPI_SI/SIO0 | 128     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip input pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is LSB first.</i>  |
| SPI_CS#0    | 127     | O                 | 12         | Chip Select Output Pin.<br>Slave Transmit Enable and active low.                                                                            |

### 5.5.7. UART Interface Pins

**Table 8. UART Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                    |
|----------|---------|-------------------|------------|--------------------------------|
| UART0_RX | 125     | I <sub>PD</sub>   | 4          | UART0 Interface Receive Data.  |
| UART0_TX | 124     | I/O <sub>PD</sub> | 4          | UART0 Interface Transmit Data. |
| UART1_RX | 116     | I <sub>PU</sub>   | 4          | UART1 Interface Receive Data.  |
| UART1_TX | 117     | I/O <sub>PD</sub> | 4          | UART1 Interface Transmit Data. |

### 5.5.8. LED Interface Pins

**Table 9. LED Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                                                                                                                                                                                         |
|----------|---------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LED_CLK  | 122     | O <sub>PU</sub>   | 12         | (1) In Serial LED Mode<br>Reference output clock for serial LED interface and Data is latched on the rising of LEDCK.<br>(2) In SMI-like LED Mode<br>Reference output clock for I2C-like interface. |
| LED_DAT  | 123     | I/O <sub>PU</sub> | 12         | (1) In Serial LED Mode<br>Serial bit stream of link status information.<br>(2) In I2C-like LED Mode<br>The data written to the LED IC.                                                              |

### 5.5.9. GPIO Interface Pins

**Table 10. GPIO Interface Pins**

| Pin Name    | Pin No.       | Type              | Drive (mA) | Description                                                                                   |
|-------------|---------------|-------------------|------------|-----------------------------------------------------------------------------------------------|
| GPIO0       | 113           | I/O <sub>PD</sub> | 4          | This pin default set as system LED.<br>Can be configured as General Purpose Input/Output Pin. |
| GPIO[3:1]   | 110, 111, 112 | I/O <sub>PD</sub> | 4          | General Purpose Input/Output Pins.                                                            |
| GPO10       | 30            | I/O <sub>PD</sub> | 4          | General Purpose Output Pins.                                                                  |
| GPIO11      | 31            | I/O <sub>PD</sub> | 4          | General Purpose Input/Output Pins.                                                            |
| GPIO[14:12] | 32,28,29      | I/O <sub>PU</sub> | 4          | General Purpose Input/Output Pins.                                                            |

### 5.5.10. EJTAG Interface Pins

**Table 11. EJTAG Interface Pins**

| Pin Name   | Pin No. | Type              | Drive (mA) | Description            |
|------------|---------|-------------------|------------|------------------------|
| JTAG_TMS   | 29      | I/O <sub>PU</sub> | 4          | JTAG Test Mode Select. |
| JTAG_TCK   | 28      | I/O <sub>PU</sub> | 4          | JTAG Test Clock Input. |
| JTAG_TRST# | 32      | I/O <sub>PU</sub> | 4          | JTAG Test Reset.       |
| JTAG_TDI   | 31      | I/O <sub>PD</sub> | 4          | JTAG Test Data Input.  |
| JTAG_TDO   | 30      | I/O <sub>PD</sub> | 4          | JTAG Test Data Output. |

### Table 12. Configuration Strapping Pins

| Pin Name       | Pin No.  | Default | Description                                                                                                                                              |
|----------------|----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| EEPROMTYPE     | 30       | 0b0     | Select EEPROM Address Byte Size.<br>0b0: 1-byte<br>0b1: 2-byte                                                                                           |
| DIS_PHYAUTO_UP | 117      | 0b0     | Disable ASIC Auto Power Up PHY.<br>0b0: Enable ASIC auto power up PHY<br>0b1: Disable ASIC auto power up PHY                                             |
| REG_IF_SEL     | 124      | 0b0     | Select Switch Core Register Access Interface.<br>0b0: I2C<br>0b1: SPI slave                                                                              |
| DIS_EEE        | 150      | 0b0     | Disable 1000M EEE and 100M EEE Function.<br>0b0: Enable<br>0b1: Disable                                                                                  |
| PWRBLINK[1:0]  | 152, 151 | 0b00    | Select LED Power On Blinking Timer.<br>0b00: Disable<br>0b01: 800ms<br>0b10: 1.6s<br>0b11: 3.2s                                                          |
| SEL_XTAL_CLK   | 153      | 0b0     | Select XTAL Input is 25M or 125M.<br>0b0: 25M<br>0b1: 125M<br><i>Note: This option is only for sync Ethernet.</i>                                        |
| SDS_PDOWN_EN   | 154      | 0b0     | Enable SerDes Power Down Mode.<br>0b0: SerDes 0/1 operate in normal mode<br>0b1: SerDes0/1 operate in power down mode                                    |
| SPI_ADDR_SEL   | 155      | 0b0     | Select Address Mode for SPI Flash.<br>0b0: 3-byte address<br>0b1: 4-byte address                                                                         |
| LED_MODE[1:0]  | 156, 157 | 0b0     | Select LED Mode.<br>0b00: Serial LED mode<br>0b01: Scan Single mode<br>0b10: Scan Bicolor mode<br>0b11: Disable LED                                      |
| CPU_SLEEP      | 166      | 0b0     | Enable CPU Function.<br>0b0: CPU is always under reset state<br>0b1: CPU is enabled                                                                      |
| DRAM_INI_EN    | 167      | 0b0     | Enable DRAM Initialization Procedure.<br>0b0: Enable DRAM Initialization procedure<br>0b1: Bypass DRAM Initialization procedure                          |
| MEM_TYPE[1:0]  | 169, 170 | 0b00    | Select Memory Type for SOC.<br>0b00: Select SPI flash + DDR-3<br>0b01: Select SPI flash + DDR-2<br>0b10: Select SPI flash + DDR-1<br>0b11: Select EEPROM |

| Pin Name      | Pin No.  | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK_M_EE[1:0] | 171, 172 | 0b00    | <p>When MEM_TYPE Select is SPI Flash:<br/>This Strapping Pin Selects the Initial Clock for The Memory Controller.<br/>For DDR2:<br/>0b00: Reserved for test;                      0b01: Reserved for test;<br/>0b10: 100MHz                                      0b11: Reserved for test;<br/>For DDR3:<br/>0b00: Reserved for test;                      0b01: Reserved for test;<br/>0b10: 125MHz                                      0b11: Reserved for test;<br/><i>Note: The initial value for this strapping pin must be set as recommended in the reference design guide.</i></p> <p>When MEM_TYPE Select is EEPROM:<br/>CLK_M_EE[0] is used to select SOC EEPROM address byte size.<br/>0b0: 1-byte address                              0b1: 2-byte address</p> |
| EN_DECRYPT    | 173      | 0b0     | <p>Enable or Disable Decrypt for Flash.<br/>0b0: Disable decrypt                              0b1: Enable decrypt</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

## 5.5.12. Miscellaneous Interface Pins

**Table 13. Miscellaneous Interface Pins**

| Pin Name         | Pin No.                                 | Type              | Drive (mA) | Description                                                                                                                                                     |
|------------------|-----------------------------------------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDC              | 120                                     | O <sub>PU</sub>   | 12         | MII Management Interface Clock Pin.                                                                                                                             |
| MDIO             | 121                                     | I/O <sub>PU</sub> | 12         | MII Management Interface Data Pin.                                                                                                                              |
| SSPI_CLK/I2C_CLK | 119                                     | I/O <sub>PU</sub> | 4          | SPI Serial Clock Input (Slave Mode).<br>I2C Interface Clock Input (Slave Mode).<br>I2C Interface Clock Output (Master Mode).                                    |
| SSPI_SI/I2C_DAT  | 118                                     | I/O <sub>PU</sub> | 4          | SPI Serial Data Input (Slave Mode).<br>I2C Interface Bi-Directional data (Slave Mode).                                                                          |
| SSPI_SO          | 117                                     | I/O <sub>PD</sub> | 4          | SPI Serial Data Output (Slave Mode).                                                                                                                            |
| SSPI_CS#         | 116                                     | O <sub>UP</sub>   | 4          | SPI Serial Chip Select (Slave Mode).                                                                                                                            |
| RESET#           | 114                                     | AI                | -          | System Pin Reset Input (Low Active).<br>To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled up for normal operation. |
| XI               | 106                                     | AI                | -          | 25MHz Crystal Clock Input and Feedback Pin.                                                                                                                     |
| XO               | 105                                     | AO                | -          | 25MHz Crystal Clock Output Pin.                                                                                                                                 |
| MDIREF           | 21                                      | AO                | -          | MDI Bias Resistor.<br>Adjust the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.                                        |
| RTT1             | 23                                      | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| RTT2             | 24                                      | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| VX               | 179                                     | A                 | -          | Low Voltage Power Control Resistor.                                                                                                                             |
| CKOUT0           | 92                                      | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |
| ATESTCK[1:0]     | 58, 214                                 | AO                | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| RESERVED         | 82, 83, 87, 88, 180, 182, 183, 187, 188 | -                 | -          | Reserved pins (Must be Left Floating).                                                                                                                          |

| Pin Name  | Pin No.                                  | Type | Drive (mA) | Description           |
|-----------|------------------------------------------|------|------------|-----------------------|
| TEST[7:0] | 84, 85, 89, 90,<br>184, 185, 189,<br>190 | -    | -          | Reserved for Testing. |

### 5.5.13. Power and Ground Pins

**Table 14. Power and Ground Pins**

| Pin Name  | Pin No.                                                 | Type | Description                       |
|-----------|---------------------------------------------------------|------|-----------------------------------|
| AVDDL     | 3, 13, 22, 42, 52, 63,<br>73, 198, 208                  | AP   | Analog Low Voltage Power.         |
| PLLVDL    | 57, 213                                                 | AP   | Analog PLL Low Voltage Power.     |
| AVDDH     | 8, 14, 19, 25, 36, 41,<br>47, 68, 78, 193, 203          | AP   | Analog High Voltage Power.        |
| DVDDL     | 26, 33, 34, 79, 108,<br>109, 126, 139, 160,<br>178, 192 | P    | Digital Low Voltage Power.        |
| DVDDH     | 27, 35, 115, 131                                        | P    | Digital High Voltage Power.       |
| SVDDL     | 81, 86, 93, 98, 103,<br>181, 191                        | AP   | SerDes Low Voltage Power.         |
| AVDDL_PLL | 107                                                     | AP   | PLL Low Voltage Power.            |
| SVDDH     | 91, 186                                                 | AP   | SerDes High Voltage Power.        |
| AVDDH_PLL | 104                                                     | AP   | PLL High Voltage Power.           |
| MVDDH     | 132, 162, 163, 177                                      | P    | SDRAM High Voltage Power.         |
| VREF      | 143                                                     | P    | SSTL Reference Voltage (MVDDH/2). |
| AGND      | 20                                                      | AG   | Analog Ground.                    |
| DGND      | E-PAD                                                   | G    | Digital Ground.                   |



### 6.3. Pin Assignments Table Codes (RTL8382M-VB)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

|                                                                                |                                                                                 |
|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| I: Input Pin                                                                   | AI: Analog Input Pin                                                            |
| O: Output Pin                                                                  | AO: Analog Output Pin                                                           |
| I/O: Bi-Directional Input/Output Pin                                           | AI/O: Analog Bi-Directional Input/Output Pin                                    |
| P: Digital Power Pin                                                           | AP: Analog Power Pin                                                            |
| G: Digital Ground Pin                                                          | AG: Analog Ground Pin                                                           |
| I <sub>PU</sub> : Input Pin With Pull-Up Resistor;<br>(Typical Value = 75KΩ)   | O <sub>PU</sub> : Output Pin With Pull-Up Resistor;<br>(Typical Value = 75KΩ)   |
| I <sub>PD</sub> : Input Pin With Pull-Down Resistor;<br>(Typical Value = 75KΩ) | O <sub>PD</sub> : Output Pin With Pull-Down Resistor;<br>(Typical Value = 75KΩ) |

### 6.4. Pin Assignments Table (RTL8382M-VB)

**Table 15. Pin Assignments Table (RTL8382M-VB)**

| Name    | Pin No. | Type | Name                | Pin No. | Type              |
|---------|---------|------|---------------------|---------|-------------------|
| P2MDIBP | 1       | AI/O | AVDDH               | 19      | AP                |
| P2MDIBN | 2       | AI/O | AGND                | 20      | AG                |
| AVDDL   | 3       | AP   | MDIREF              | 21      | AO                |
| P2MDICP | 4       | AI/O | AVDDL               | 22      | AP                |
| P2MDICN | 5       | AI/O | RTT1                | 23      | AI/O              |
| P2MDIDP | 6       | AI/O | RTT2                | 24      | AI/O              |
| P2MDIDN | 7       | AI/O | AVDDH               | 25      | AP                |
| AVDDH   | 8       | AP   | DVDDL               | 26      | DP                |
| P3MDIAP | 9       | AI/O | DVDDH               | 27      | DP                |
| P3MDIAN | 10      | AI/O | JTAG_TCK            | 28      | I/O <sub>PU</sub> |
| P3MDIBP | 11      | AI/O | JTAG_TMS            | 29      | I/O <sub>PU</sub> |
| P3MDIBN | 12      | AI/O | JTAG_TDO/EEPROMTYPE | 30      | I/O <sub>PD</sub> |
| AVDDL   | 13      | AP   | JTAG_TDI            | 31      | I/O <sub>PD</sub> |
| AVDDH   | 14      | AP   | JTAG_TRST#          | 32      | I/O <sub>PU</sub> |
| P3MDICP | 15      | AI/O | DVDDL               | 33      | DP                |
| P3MDICN | 16      | AI/O | DVDDH               | 34      | DP                |
| P3MDIDP | 17      | AI/O | DVDDH               | 35      | DP                |
| P3MDIDN | 18      | AI/O | AVDDH               | 36      | AP                |

| Name     | Pin No. | Type |
|----------|---------|------|
| P4MDIAP  | 37      | AI/O |
| P4MDIAN  | 38      | AI/O |
| P4MDIBP  | 39      | AI/O |
| P4MDIBN  | 40      | AI/O |
| AVDDH    | 41      | AP   |
| AVDDL    | 42      | AP   |
| P4MDICP  | 43      | AI/O |
| P4MDICN  | 44      | AI/O |
| P4MDIDP  | 45      | AI/O |
| P4MDIDN  | 46      | AI/O |
| AVDDH    | 47      | AP   |
| P5MDIAP  | 48      | AI/O |
| P5MDIAN  | 49      | AI/O |
| P5MDIBP  | 50      | AI/O |
| P5MDIBN  | 51      | AI/O |
| AVDDL    | 52      | AP   |
| P5MDICP  | 53      | AI/O |
| P5MDICN  | 54      | AI/O |
| P5MDIDP  | 55      | AI/O |
| P5MDIDN  | 56      | AI/O |
| PLLVDL   | 57      | AP   |
| ATESTCK1 | 58      | AO   |
| P6MDIAP  | 59      | AI/O |
| P6MDIAN  | 60      | AI/O |
| P6MDIBP  | 61      | AI/O |
| P6MDIBN  | 62      | AI/O |
| AVDDL    | 63      | AP   |
| P6MDICP  | 64      | AI/O |
| P6MDICN  | 65      | AI/O |
| P6MDIDP  | 66      | AI/O |
| P6MDIDN  | 67      | AI/O |
| AVDDH    | 68      | AP   |
| P7MDIAP  | 69      | AI/O |
| P7MDIAN  | 70      | AI/O |
| P7MDIBP  | 71      | AI/O |
| P7MDIBN  | 72      | AI/O |
| AVDDL    | 73      | AP   |
| P7MDICP  | 74      | AI/O |
| P7MDICN  | 75      | AI/O |
| P7MDIDP  | 76      | AI/O |
| P7MDIDN  | 77      | AI/O |

| Name                       | Pin No. | Type              |
|----------------------------|---------|-------------------|
| AVDDH                      | 78      | AP                |
| DVDDL                      | 79      | DP                |
| CKOUT2                     | 80      | AO                |
| SVDDL                      | 81      | AP                |
| S2TXP                      | 82      | AO                |
| S2TXN                      | 83      | AO                |
| S2RXP                      | 84      | AI                |
| S2RXN                      | 85      | AI                |
| SVDDL                      | 86      | AP                |
| S3TXN                      | 87      | AO                |
| S3TXP                      | 88      | AO                |
| S3RXN                      | 89      | AI                |
| S3RXP                      | 90      | AI                |
| SVDDH                      | 91      | AP                |
| CKOUT4                     | 92      | AO                |
| SVDDL                      | 93      | AP                |
| S4TXP                      | 94      | AO                |
| S4TXN                      | 95      | AO                |
| S4RXP                      | 96      | AI                |
| S4RXN                      | 97      | AI                |
| SVDDL                      | 98      | AP                |
| S5TXN                      | 99      | AO                |
| S5TXP                      | 100     | AO                |
| S5RXN                      | 101     | AI                |
| S5RXP                      | 102     | AI                |
| SVDDL                      | 103     | AP                |
| AVDDH_PLL                  | 104     | AP                |
| XO                         | 105     | AO                |
| XI                         | 106     | AI                |
| AVDDL_PLL                  | 107     | AP                |
| DVDDL                      | 108     | P                 |
| DVDDL                      | 109     | P                 |
| GPIO3                      | 110     | I/O <sub>PD</sub> |
| GPIO2                      | 111     | I/O <sub>PD</sub> |
| GPIO1                      | 112     | I/O <sub>PD</sub> |
| GPIO0                      | 113     | I/O <sub>PD</sub> |
| RESET#                     | 114     | AI                |
| DVDDH                      | 115     | P                 |
| SSPI_CS#                   | 116     | I <sub>PU</sub>   |
| SSPI_SO/<br>DIS_PHYAUTO_UP | 117     | I/O <sub>PD</sub> |
| SSPI_SI/I2C_DAT            | 118     | I/O <sub>PU</sub> |

| Name                              | Pin No. | Type              |
|-----------------------------------|---------|-------------------|
| SSPI_CLK/I2C_CLK                  | 119     | I/O <sub>PU</sub> |
| MDC                               | 120     | O <sub>PU</sub>   |
| MDIO                              | 121     | I/O <sub>PU</sub> |
| LED_CLK                           | 122     | O <sub>PU</sub>   |
| LED_DAT                           | 123     | I/O <sub>PU</sub> |
| UART0_TX/REG_IF_SEL               | 124     | I/O <sub>PD</sub> |
| UART0_RX                          | 125     | I <sub>PD</sub>   |
| DVDDL                             | 126     | P                 |
| SPI_CS#0                          | 127     | O                 |
| SPI_SI/SIO0                       | 128     | I/O <sub>PD</sub> |
| SPI_SO/SIO1                       | 129     | I/O <sub>PD</sub> |
| SPI_CLK                           | 130     | O <sub>PD</sub>   |
| DVDDH                             | 131     | P                 |
| MVDDH                             | 132     | P                 |
| DDR12_D4/DDR3_D6                  | 133     | I/O               |
| DDR12_D3/DDR3_D2                  | 134     | I/O               |
| DDR12_D1/DDR3_D4                  | 135     | I/O               |
| DDR12_D6/DDR3_D0                  | 136     | I/O               |
| DDR12_DM/DDR3_DQS                 | 137     | I/O               |
| DDR3_DQS#                         | 138     | I/O               |
| DVDDL                             | 139     | P                 |
| DDR12_CLK#/DDR3_CLK#              | 140     | O                 |
| DDR12_CLK/DDR3_CLK                | 141     | O                 |
| DDR12_DQS/DDR3_DM                 | 142     | I/O               |
| VREF                              | 143     | P                 |
| DDR12_D7/DDR3_D3                  | 144     | I/O               |
| DDR12_D0/DDR3_D1                  | 145     | I/O               |
| DDR12_D2/DDR3_D7                  | 146     | I/O               |
| DDR12_D5/DDR3_D5                  | 147     | I/O               |
| DDR2_ODT/DDR3_CKE                 | 148     | O                 |
| DDR12_CS#/DDR3_BA1                | 149     | O                 |
| DDR12_A0/DDR3_A12/<br>DIS_EEE     | 150     | I/O               |
| DDR12_A2/DDR3_A4/<br>PWRBLINK[0]  | 151     | I/O               |
| DDR12_A4/DDR3_A6/<br>PWRBLINK[1]  | 152     | I/O               |
| DDR12_A6/DDR3_A8/<br>SEL_XTAL_CLK | 153     | I/O               |
| DDR12_A8/DDR3_A1/<br>SDS_PDOWN_EN | 154     | I/O               |
| DDR3_A14/SPI_ADDR_SEL             | 155     | I/O               |

| Name                               | Pin No. | Type |
|------------------------------------|---------|------|
| DDR12_A13/DDR3_A11/<br>LED/MODE[1] | 156     | I/O  |
| DDR12_A11/DDR3_A10/<br>LED/MODE[0] | 157     | I/O  |
| DDR12_CAS#/DDR3_RAS#               | 158     | O    |
| DDR12_RAS#/DDR3_CAS#               | 159     | O    |
| DVDDL                              | 160     | P    |
| DDR12_WE#/DDR3_WE#                 | 161     | O    |
| MVDDH                              | 162     | P    |
| MVDDH                              | 163     | P    |
| DDR12_CKE/DDR3_BA2                 | 164     | O    |
| DDR12_BA1/DDR3_A9                  | 165     | O    |
| DDR12_A1/DDR3_A13/<br>CPU_SLEEP    | 166     | I/O  |
| DDR12_A12/DDR3_A2/<br>DRAM_INI_EN  | 167     | I/O  |
| DDR3_RST#                          | 168     | O    |
| DDR12_A9/DDR3_A7/<br>MEM_TYPE[1]   | 169     | I/O  |
| DDR12_A7/DDR3_A5/<br>MEM_TYPE[0]   | 170     | I/O  |
| DDR12_A5/DDR3_A0/<br>CLK_M_EE[1]   | 171     | I/O  |
| DDR12_A3/DDR3_A3/<br>CLK_M_EE[0]   | 172     | I/O  |
| DDR12_A10/DDR3_BA0/<br>EN_DECRYPT  | 173     | I/O  |
| DDR2_BA2/DDR3_CS#                  | 174     | O    |
| DDR12_BA0/DDR3_ODT                 | 175     | O    |
| DDR3_ZQ#                           | 176     | -    |
| MVDDH                              | 177     | P    |
| DVDDL                              | 178     | P    |
| VX                                 | 179     | A    |
| CKOUT0                             | 180     | AO   |
| SVDDL                              | 181     | AP   |
| S0TXP                              | 182     | AO   |
| S0TXN                              | 183     | AO   |
| S0RXP                              | 184     | AI   |
| S0RXN                              | 185     | AI   |
| SVDDH                              | 186     | AP   |
| S1TXN                              | 187     | AO   |
| S1TXP                              | 188     | AO   |
| S1RXN                              | 189     | AI   |
| S1RXP                              | 190     | AI   |

| Name    | Pin No. | Type |
|---------|---------|------|
| SVDDL   | 191     | AP   |
| DVDDL   | 192     | P    |
| AVDDH   | 193     | AP   |
| P0MDIAP | 194     | AI/O |
| P0MDIAN | 195     | AI/O |
| P0MDIBP | 196     | AI/O |
| P0MDIBN | 197     | AI/O |
| AVDDL   | 198     | AP   |
| P0MDICP | 199     | AI/O |
| P0MDICN | 200     | AI/O |
| P0MDIDP | 201     | AI/O |
| P0MDIDN | 202     | AI/O |
| AVDDH   | 203     | AP   |
| P1MDIAP | 204     | AI/O |

| Name     | Pin No. | Type |
|----------|---------|------|
| P1MDIAN  | 205     | AI/O |
| P1MDIBP  | 206     | AI/O |
| P1MDIBN  | 207     | AI/O |
| AVDDL    | 208     | AP   |
| P1MDICP  | 209     | AI/O |
| P1MDICN  | 210     | AI/O |
| P1MDIDP  | 211     | AI/O |
| P1MDIDN  | 212     | AI/O |
| PLLVDL   | 213     | AP   |
| ATESTCK0 | 214     | AO   |
| P2MDIAP  | 215     | AI/O |
| P2MDIAN  | 216     | AI/O |
| DGND     | EPAD    | G    |

## 6.5. Pin Descriptions (RTL8382M-VB)

### 6.5.1. 1000M Ethernet PHY MDI Interface Pins

**Table 16. 1000M Ethernet PHY MDI Interface Pins**

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P0MDIAP  | 194     | AI/O | Port 0 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P0MDIAN  | 195     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBP  | 196     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBN  | 197     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICP  | 199     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICN  | 200     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDP  | 201     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDN  | 202     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIAP  | 204     | AI/O | Port 1 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P1MDIAN  | 205     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBP  | 206     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBN  | 207     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICP  | 209     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICN  | 210     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDP  | 211     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDN  | 212     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIAP  | 215     | AI/O | Port 2 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P2MDIAN  | 216     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBP  | 1       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBN  | 2       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICP  | 4       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICN  | 5       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDP  | 6       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDN  | 7       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIAP  | 9       | AI/O | Port 3 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P3MDIAN  | 10      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBP  | 11      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBN  | 12      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICP  | 15      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICN  | 16      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDP  | 17      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDN  | 18      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P4MDIAP  | 37      | AI/O | Port 4 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P4MDIAN  | 38      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBP  | 39      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBN  | 40      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICP  | 43      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICN  | 44      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDP  | 45      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDN  | 46      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIAP  | 48      | AI/O | Port 5 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P5MDIAN  | 49      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBP  | 50      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBN  | 51      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICP  | 53      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICN  | 54      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDP  | 55      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDN  | 56      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIAP  | 59      | AI/O | Port 6 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P6MDIAN  | 60      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBP  | 61      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBN  | 62      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICP  | 64      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICN  | 65      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDP  | 66      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDN  | 67      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIAP  | 69      | AI/O | Port 7 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P7MDIAN  | 70      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBP  | 71      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBN  | 72      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICP  | 74      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICN  | 75      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDP  | 76      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDN  | 77      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

## 6.5.2. SGMII Interface Pins

**Table 17. SGMII Interface Pins**

| Pin Name | Pin No. | Type | Description                                             |
|----------|---------|------|---------------------------------------------------------|
| S4RXP    | 96      | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S4RXN    | 97      | AI   |                                                         |
| S4TXP    | 94      | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S4TXN    | 95      | AO   |                                                         |
| S5RXP    | 102     | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S5RXN    | 101     | AI   |                                                         |
| S5TXP    | 100     | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S5TXN    | 99      | AO   |                                                         |

## 6.5.3. QSGMII Interface Pins

**Table 18. QSGMII Interface Pins**

| Pin Name | Pin No. | Type | Description                                              |
|----------|---------|------|----------------------------------------------------------|
| S0RXP    | 184     | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S0RXN    | 185     | AI   |                                                          |
| S0TXP    | 182     | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S0TXN    | 183     | AO   |                                                          |
| S1RXP    | 190     | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S1RXN    | 189     | AI   |                                                          |
| S1TXP    | 188     | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S1TXN    | 187     | AO   |                                                          |
| S2RXP    | 84      | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S2RXN    | 85      | AI   |                                                          |
| S2TXP    | 82      | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S2TXN    | 83      | AO   |                                                          |
| S3RXP    | 90      | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S3RXN    | 89      | AI   |                                                          |
| S3TXP    | 88      | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S3TXN    | 87      | AO   |                                                          |
| S4RXP    | 96      | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S4RXN    | 97      | AI   |                                                          |
| S4TXP    | 94      | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S4TXN    | 95      | AO   |                                                          |

#### 6.5.4. 1000Base-X/100Base-FX Interface Pins

**Table 19. 1000Base-X/100Base-FX Interface Pins**

| Pin Name | Pin No. | Type | Description                                                             |
|----------|---------|------|-------------------------------------------------------------------------|
| S4RXP    | 96      | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S4RXN    | 97      | AI   |                                                                         |
| S4TXP    | 94      | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S4TXN    | 95      | AO   |                                                                         |
| S5RXP    | 102     | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S5RXN    | 101     | AI   |                                                                         |
| S5TXP    | 100     | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S5TXN    | 99      | AO   |                                                                         |

#### 6.5.5. DDR1/2 SDRAM Interface Pins

**Table 20. DDR1/2 SDRAM Interface Pins**

| Pin Name      | Pin No.                                                              | Type | Drive (mA) | Description                                                      |
|---------------|----------------------------------------------------------------------|------|------------|------------------------------------------------------------------|
| DDR12_D[7:0]  | 144, 136, 147, 133, 134, 146, 135, 145                               | I/O  | 8          | DDR SDRAM Data Bus.                                              |
| DDR12_A[13:0] | 156, 167, 157, 173, 169, 154, 170, 153, 171, 152, 172, 151, 166, 150 | I/O  | 8          | DDR SDRAM Address Select.                                        |
| DDR2_BA[2]    | 174                                                                  | O    | 8          | DDR SDRAM Bank Address Select.                                   |
| DDR12_BA[1:0] | 165, 175                                                             | O    | 8          | DDR SDRAM Bank Address Select.                                   |
| DDR12_WE#     | 161                                                                  | O    | 8          | DDR SDRAM Write Enable.                                          |
| DDR12_CKE     | 164                                                                  | O    | 8          | DDR SDRAM Clock Enable.                                          |
| DDR12_RAS#    | 159                                                                  | O    | 8          | DDR SDRAM Row Address Strobe.                                    |
| DDR12_CAS#    | 158                                                                  | O    | 8          | DDR SDRAM Column Address Strobe.                                 |
| DDR12_CS#0    | 149                                                                  | O    | 8          | DDR SDRAM Chip Select 0.                                         |
| DDR2_ODT      | 148                                                                  | O    | 8          | DDR SDRAM On-Die Termination.                                    |
| DDR12_DQS     | 142                                                                  | I/O  | 8          | DDR SDRAM Data Strobe.                                           |
| DDR12_CLK     | 141                                                                  | O    | 8          | DDR SDRAM Clock.<br>CLK and CLK# are differential clock outputs. |
| DDR12_CLK#    | 140                                                                  | O    | 8          | DDR SDRAM Clock.<br>CLK and CLK# are differential clock outputs. |

## 6.5.6. DDR3 SDRAM Interface Pins

**Table 21. DDR3 SDRAM Interface Pins**

| Pin Name      | Pin No.                                           | Type | Drive (mA) | Description                                                                                                                                 |
|---------------|---------------------------------------------------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| DDR3_D[7:0]   | 146, 133, 147, 135,<br>144, 134, 145, 136         | I/O  | 8          | DDR SDRAM Data Bus.                                                                                                                         |
| DDR3_A[14]    | 155                                               | O    | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[13:10] | 166, 150, 156, 157                                | I/O  | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[9]     | 165                                               | O    | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_A[8:0]   | 153, 169, 152, 170,<br>151, 172, 167, 154,<br>171 | I/O  | 8          | DDR SDRAM Address Select.                                                                                                                   |
| DDR3_DQS#     | 138                                               | I/O  | 8          | DDR SDRAM Data Strobe.                                                                                                                      |
| DDR3_DQS      | 137                                               | I/O  | 8          | DDR SDRAM Data Strobe.                                                                                                                      |
| DDR3_CLK#     | 140                                               | O    | 8          | DDR SDRAM Clock.                                                                                                                            |
| DDR3_CLK      | 141                                               | O    | 8          | DDR SDRAM Clock.                                                                                                                            |
| DDR3_DM       | 142                                               | I/O  | 8          | DDR SDRAM Data Mask.                                                                                                                        |
| DDR3_CKE      | 148                                               | O    | 8          | DDR SDRAM Clock Enable.                                                                                                                     |
| DDR3_BA[2:1]  | 164, 149                                          | O    | 8          | DDR SDRAM Bank Address Select.                                                                                                              |
| DDR3_BA[0]    | 173                                               | I/O  | 8          | DDR SDRAM Bank Address Select.                                                                                                              |
| DDR3_RAS#     | 158                                               | O    | 8          | DDR SDRAM Row Address Strobe.                                                                                                               |
| DDR3_CAS#     | 159                                               | O    | 8          | DDR SDRAM Column Address Strobe.                                                                                                            |
| DDR3_WE#      | 161                                               | O    | 8          | DDR SDRAM Write Enable.                                                                                                                     |
| DDR3_RST#     | 168                                               | O    | 8          | DDR SDRAM Reset.                                                                                                                            |
| DDR3_CS#      | 174                                               | O    | 8          | DDR SDRAM Chip Select.                                                                                                                      |
| DDR3_ODT      | 175                                               | O    | 8          | DDR SDRAM On-Die Termination.                                                                                                               |
| DDR3_ZQ#      | 176                                               | -    | 8          | DDR SDRAM External Reference Ball for Output Drive Calibration.<br>This ball is tied to an external 240 Ohm resistor, which is tied to GND. |

## 6.5.7. Master Mode SPI Flash Interface Pins

**Table 22. Master Mode SPI Flash Interface Pins**

| Pin Name    | Pin No. | Type              | Drive (mA) | Description                                                                                                                                 |
|-------------|---------|-------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| SPI_CLK     | 130     | O <sub>PD</sub>   | 12         | Serial Clock Output Pin.                                                                                                                    |
| SPI_SO/SIO1 | 129     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip output pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is MSB first.</i> |
| SPI_SI/SIO0 | 128     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip input pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is LSB first.</i>  |
| SPI_CS#0    | 127     | O                 | 12         | Chip Select Output Pin.<br>Slave Transmit Enable and active low.                                                                            |

## 6.5.8. UART Interface Pins

**Table 23. UART Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                    |
|----------|---------|-------------------|------------|--------------------------------|
| UART0_RX | 125     | I <sub>PD</sub>   | 4          | UART0 Interface Receive Data.  |
| UART0_TX | 124     | I/O <sub>PD</sub> | 4          | UART0 Interface Transmit Data. |
| UART1_RX | 116     | I <sub>PU</sub>   | 4          | UART1 Interface Receive Data.  |
| UART1_TX | 117     | I/O <sub>PD</sub> | 4          | UART1 Interface Transmit Data. |

## 6.5.9. LED Interface Pins

**Table 24. LED Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                                                                                                                                                                                         |
|----------|---------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LED_CLK  | 122     | O <sub>PU</sub>   | 12         | (1) In Serial LED Mode<br>Reference output clock for serial LED interface and Data is latched on the rising of LEDCK.<br>(2) In SMI-like LED Mode<br>Reference output clock for I2C-like interface. |
| LED_DAT  | 123     | I/O <sub>PU</sub> | 12         | (1) In Serial LED Mode<br>Serial bit stream of link status information.<br>(2) In I2C-like LED Mode<br>The data written to the LED IC.                                                              |

## 6.5.10. GPIO Interface Pins

**Table 25. GPIO Interface Pins**

| Pin Name    | Pin No.       | Type              | Drive (mA) | Description                                                                                   |
|-------------|---------------|-------------------|------------|-----------------------------------------------------------------------------------------------|
| GPIO0       | 113           | I/O <sub>PD</sub> | 4          | This pin default set as system LED.<br>Can be configured as General Purpose Input/Output Pin. |
| GPIO[3:1]   | 110, 111, 112 | I/O <sub>PD</sub> | 4          | General Purpose Input/Output Pins.                                                            |
| GPO10       | 30            | I/O <sub>PD</sub> | 4          | General Purpose Output Pins.                                                                  |
| GPIO11      | 31            | I/O <sub>PD</sub> | 4          | General Purpose Input/Output Pins.                                                            |
| GPIO[14:12] | 32,28,29      | I/O <sub>PU</sub> | 4          | General Purpose Input/Output Pins.                                                            |

## 6.5.11. EJTAG Interface Pins

**Table 26. EJTAG Interface Pins**

| Pin Name   | Pin No. | Type              | Drive (mA) | Description            |
|------------|---------|-------------------|------------|------------------------|
| JTAG_TMS   | 29      | I/O <sub>PU</sub> | 4          | JTAG Test Mode Select. |
| JTAG_TCK   | 28      | I/O <sub>PU</sub> | 4          | JTAG Test Clock Input. |
| JTAG_TRST# | 32      | I/O <sub>PU</sub> | 4          | JTAG Test Reset.       |
| JTAG_TDI   | 31      | I/O <sub>PD</sub> | 4          | JTAG Test Data Input.  |
| JTAG_TDO   | 30      | I/O <sub>PD</sub> | 4          | JTAG Test Data Output. |



| Pin Name      | Pin No.  | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK_M_EE[1:0] | 171, 172 | 0b00    | <p>When MEM_TYPE Select is SPI Flash:<br/>This Strapping Pin Selects the Initial Clock for The Memory Controller.<br/>For DDR2:<br/>0b00: Reserved for test;                      0b01: Reserved for test;<br/>0b10: 100MHz                                      0b11: Reserved for test;<br/>For DDR3:<br/>0b00: Reserved for test;                      0b01: Reserved for test;<br/>0b10: 125MHz                                      0b11: Reserved for test;<br/><i>Note: The initial value for this strapping pin must be set as recommended in the reference design guide.</i></p> <p>When MEM_TYPE Select is EEPROM:<br/>CLK_M_EE[0] is used to select SOC EEPROM address byte size.<br/>0b0: 1-byte address<br/>0b1: 2-byte address</p> |
| EN_DECRYPT    | 173      | 0b0     | <p>Enable or Disable Decrypt for Flash.<br/>0b0: Disable decrypt<br/>0b1: Enable decrypt</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

### 6.5.13. Miscellaneous Interface Pins

**Table 28. Miscellaneous Interface Pins**

| Pin Name         | Pin No. | Type              | Drive (mA) | Description                                                                                                                                                     |
|------------------|---------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDC              | 120     | O <sub>PU</sub>   | 12         | MII Management Interface Clock Pin.                                                                                                                             |
| MDIO             | 121     | I/O <sub>PU</sub> | 12         | MII Management Interface Data Pin.                                                                                                                              |
| SSPI_CLK/I2C_CLK | 119     | I/O <sub>PU</sub> | 4          | SPI Serial Clock Input (Slave Mode).<br>I2C Interface Clock Input (Slave Mode).<br>I2C Interface Clock Output (Master Mode).                                    |
| SSPI_SI/I2C_DAT  | 118     | I/O <sub>PU</sub> | 4          | SPI Serial Data Input (Slave Mode).<br>I2C Interface Bi-Directional data (Slave Mode).                                                                          |
| SSPI_SO          | 117     | I/O <sub>PD</sub> | 4          | SPI Serial Data Output (Slave Mode).                                                                                                                            |
| SSPI_CS#         | 116     | O <sub>UP</sub>   | 4          | SPI Serial Chip Select (Slave Mode).                                                                                                                            |
| RESET#           | 114     | AI                | -          | System Pin Reset Input (Low Active).<br>To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled up for normal operation. |
| XI               | 106     | AI                | -          | 25MHz Crystal Clock Input and Feedback Pin.                                                                                                                     |
| XO               | 105     | AO                | -          | 25MHz Crystal Clock Output Pin.                                                                                                                                 |
| MDIREF           | 21      | AO                | -          | MDI Bias Resistor.<br>Adjust the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.                                        |
| RTT1             | 23      | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| RTT2             | 24      | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| VX               | 179     | A                 | -          | Low Voltage Power Control Resistor.                                                                                                                             |
| CKOUT0           | 180     | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |
| CKOUT2           | 80      | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |

| Pin Name     | Pin No. | Type | Drive (mA) | Description                                        |
|--------------|---------|------|------------|----------------------------------------------------|
| CKOUT4       | 92      | AO   | 8          | 25MHz Clock Output.                                |
| ATESTCK[1:0] | 58, 214 | AO   | -          | Reserved for Internal Use (Must be Left Floating). |

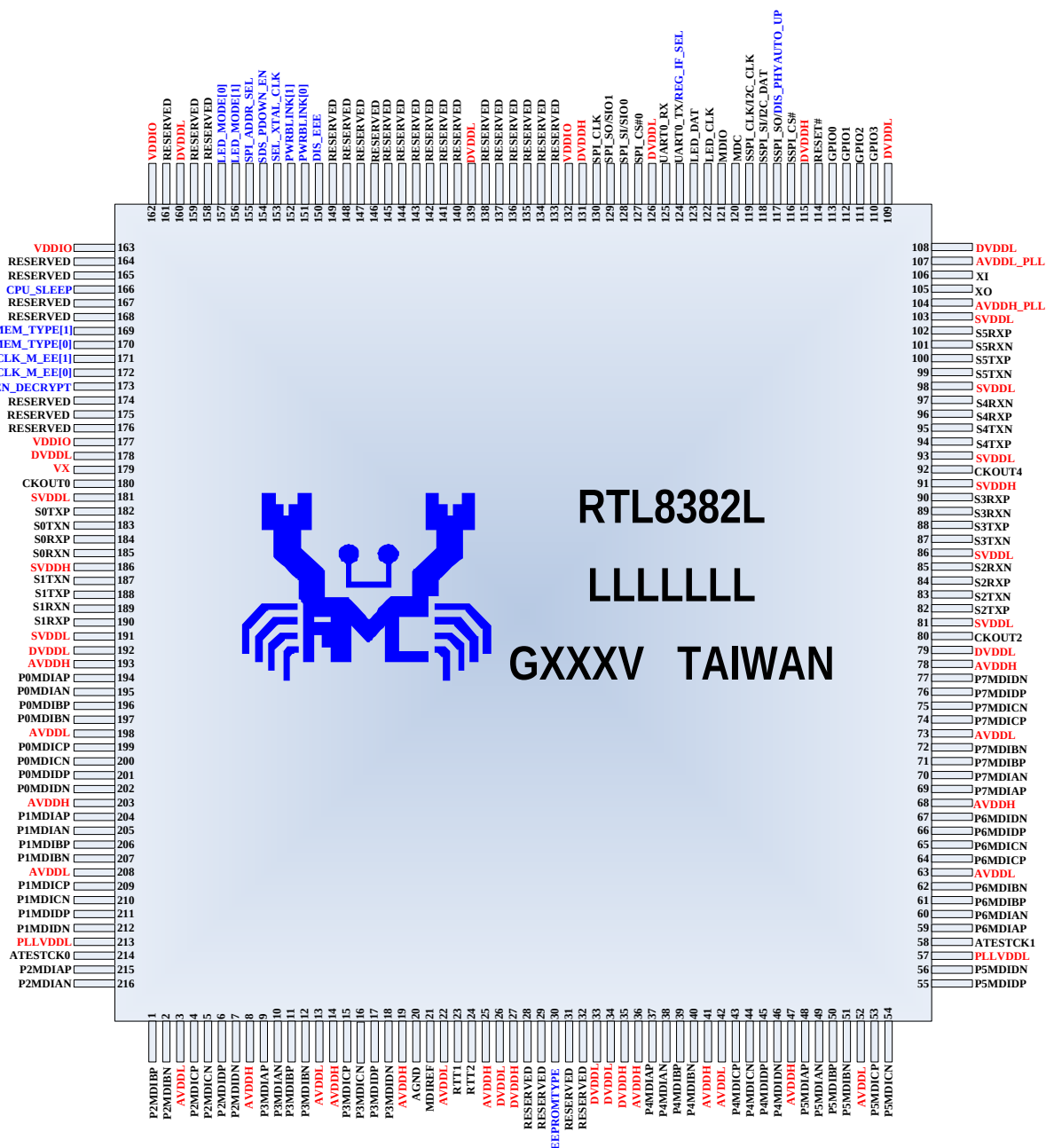
## 6.5.14. Power and Ground Pins

**Table 29. Power and Ground Pins**

| Pin Name  | Pin No.                                           | Type | Description                       |
|-----------|---------------------------------------------------|------|-----------------------------------|
| AVDDL     | 3, 13, 22, 42, 52, 63, 73, 198, 208               | AP   | Analog Low Voltage Power.         |
| PLLVDL    | 57, 213                                           | AP   | Analog PLL Low Voltage Power.     |
| AVDDH     | 8, 14, 19, 25, 36, 41, 47, 68, 78, 193, 203       | AP   | Analog High Voltage Power.        |
| DVDDL     | 26, 33, 34, 79, 108, 109, 126, 139, 160, 178, 192 | P    | Digital Low Voltage Power.        |
| DVDDH     | 27, 35, 115, 131                                  | P    | Digital High Voltage Power.       |
| SVDDL     | 81, 86, 93, 98, 103, 181, 191                     | AP   | SerDes Low Voltage Power.         |
| AVDDL_PLL | 107                                               | AP   | PLL Low Voltage Power.            |
| SVDDH     | 91, 186                                           | AP   | SerDes High Voltage Power.        |
| AVDDH_PLL | 104                                               | AP   | PLL High Voltage Power.           |
| MVDDH     | 132, 162, 163, 177                                | P    | SDRAM High Voltage Power.         |
| VREF      | 143                                               | P    | SSTL Reference Voltage (MVDDH/2). |
| AGND      | 20                                                | AG   | Analog Ground.                    |
| DGND      | E-PAD                                             | G    | Digital Ground.                   |

## 7. Pin Assignments and Descriptions (RTL8382L-VB)

### 7.1. Pin Assignments Figure (RTL8382L-VB)



### Figure 10. Pin Assignments (RTL8382L-VB)

## 7.2. Package Identification

Green package is indicated by a ‘G’ in ‘GXXXX’ (Figure 10). The version number is shown in the location marked ‘v’.

### 7.3. Pin Assignments Table Codes (RTL8382L-VB)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

|                                                                                |                                                                                 |
|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| I: Input Pin                                                                   | AI: Analog Input Pin                                                            |
| O: Output Pin                                                                  | AO: Analog Output Pin                                                           |
| I/O: Bi-Directional Input/Output Pin                                           | AI/O: Analog Bi-Directional Input/Output Pin                                    |
| P: Digital Power Pin                                                           | AP: Analog Power Pin                                                            |
| G: Digital Ground Pin                                                          | AG: Analog Ground Pin                                                           |
| I <sub>PU</sub> : Input Pin With Pull-Up Resistor;<br>(Typical Value = 75KΩ)   | O <sub>PU</sub> : Output Pin With Pull-Up Resistor;<br>(Typical Value = 75KΩ)   |
| I <sub>PD</sub> : Input Pin With Pull-Down Resistor;<br>(Typical Value = 75KΩ) | O <sub>PD</sub> : Output Pin With Pull-Down Resistor;<br>(Typical Value = 75KΩ) |

### 7.4. Pin Assignments Table (RTL8382L-VB)

**Table 30. Pin Assignments Table (RTL8382L-VB)**

| Name    | Pin No. | Type | Name       | Pin No. | Type              |
|---------|---------|------|------------|---------|-------------------|
| P2MDIBP | 1       | AI/O | AVDDH      | 19      | AP                |
| P2MDIBN | 2       | AI/O | AGND       | 20      | AG                |
| AVDDL   | 3       | AP   | MDIREF     | 21      | A                 |
| P2MDICP | 4       | AI/O | AVDDL      | 22      | AP                |
| P2MDICN | 5       | AI/O | RTT1       | 23      | AI/O              |
| P2MDIDP | 6       | AI/O | RTT2       | 24      | AI/O              |
| P2MDIDN | 7       | AI/O | AVDDH      | 25      | AP                |
| AVDDH   | 8       | AP   | DVDDL      | 26      | DP                |
| P3MDIAP | 9       | AI/O | DVDDH      | 27      | DP                |
| P3MDIAN | 10      | AI/O | RESERVED   | 28      | -                 |
| P3MDIBP | 11      | AI/O | RESERVED   | 29      | -                 |
| P3MDIBN | 12      | AI/O | EEPROMTYPE | 30      | I/O <sub>PD</sub> |
| AVDDL   | 13      | AP   | RESERVED   | 31      | -                 |
| AVDDH   | 14      | AP   | RESERVED   | 32      | -                 |
| P3MDICP | 15      | AI/O | DVDDL      | 33      | DP                |
| P3MDICN | 16      | AI/O | DVDDL      | 34      | DP                |
| P3MDIDP | 17      | AI/O | DVDDH      | 35      | DP                |
| P3MDIDN | 18      | AI/O | AVDDH      | 36      | AP                |

| Name     | Pin No. | Type |
|----------|---------|------|
| P4MDIAP  | 37      | AI/O |
| P4MDIAN  | 38      | AI/O |
| P4MDIBP  | 39      | AI/O |
| P4MDIBN  | 40      | AI/O |
| AVDDH    | 41      | AP   |
| AVDDL    | 42      | AP   |
| P4MDICP  | 43      | AI/O |
| P4MDICN  | 44      | AI/O |
| P4MDIDP  | 45      | AI/O |
| P4MDIDN  | 46      | AI/O |
| AVDDH    | 47      | AP   |
| P5MDIAP  | 48      | AI/O |
| P5MDIAN  | 49      | AI/O |
| P5MDIBP  | 50      | AI/O |
| P5MDIBN  | 51      | AI/O |
| AVDDL    | 52      | AP   |
| P5MDICP  | 53      | AI/O |
| P5MDICN  | 54      | AI/O |
| P5MDIDP  | 55      | AI/O |
| P5MDIDN  | 56      | AI/O |
| PLLVDL   | 57      | AP   |
| ATESTCK1 | 58      | AO   |
| P6MDIAP  | 59      | AI/O |
| P6MDIAN  | 60      | AI/O |
| P6MDIBP  | 61      | AI/O |
| P6MDIBN  | 62      | AI/O |
| AVDDL    | 63      | AP   |
| P6MDICP  | 64      | AI/O |
| P6MDICN  | 65      | AI/O |
| P6MDIDP  | 66      | AI/O |
| P6MDIDN  | 67      | AI/O |
| AVDDH    | 68      | AP   |
| P7MDIAP  | 69      | AI/O |
| P7MDIAN  | 70      | AI/O |
| P7MDIBP  | 71      | AI/O |
| P7MDIBN  | 72      | AI/O |
| AVDDL    | 73      | AP   |
| P7MDICP  | 74      | AI/O |
| P7MDICN  | 75      | AI/O |
| P7MDIDP  | 76      | AI/O |
| P7MDIDN  | 77      | AI/O |
| AVDDH    | 78      | AP   |

| Name                   | Pin No. | Type              |
|------------------------|---------|-------------------|
| DVDDL                  | 79      | DP                |
| CKOUT2                 | 80      | AO                |
| SVDDL                  | 81      | AP                |
| S2TXP                  | 82      | AO                |
| S2TXN                  | 83      | AO                |
| S2RXP                  | 84      | AI                |
| S2RXN                  | 85      | AI                |
| SVDDL                  | 86      | AP                |
| S3TXN                  | 87      | AO                |
| S3TXP                  | 88      | AO                |
| S3RXN                  | 89      | AI                |
| S3RXP                  | 90      | AI                |
| SVDDH                  | 91      | AP                |
| CKOUT4                 | 92      | AO                |
| SVDDL                  | 93      | AP                |
| S4TXP                  | 94      | AO                |
| S4TXN                  | 95      | AO                |
| S4RXP                  | 96      | AI                |
| S4RXN                  | 97      | AI                |
| SVDDL                  | 98      | AP                |
| S5TXN                  | 99      | AO                |
| S5TXP                  | 100     | AO                |
| S5RXN                  | 101     | AI                |
| S5RXP                  | 102     | AI                |
| SVDDL                  | 103     | AP                |
| AVDDH_PLL              | 104     | AP                |
| XO                     | 105     | AO                |
| XI                     | 106     | AI                |
| AVDDL_PLL              | 107     | AP                |
| DVDDL                  | 108     | P                 |
| DVDDL                  | 109     | P                 |
| GPIO3                  | 110     | I/O <sub>PD</sub> |
| GPIO2                  | 111     | I/O <sub>PD</sub> |
| GPIO1                  | 112     | I/O <sub>PD</sub> |
| GPIO0                  | 113     | I/O <sub>PD</sub> |
| RESET#                 | 114     | AI                |
| DVDDH                  | 115     | P                 |
| SSPI_CS#               | 116     | I <sub>PU</sub>   |
| SSPI_SO/DIS_PHYAUTO_UP | 117     | I/O <sub>PD</sub> |
| SSPI_SI/I2C_DAT        | 118     | I/O <sub>PU</sub> |
| SSPI_CLK/I2C_CLK       | 119     | I/O <sub>PU</sub> |

| Name                | Pin No. | Type              |
|---------------------|---------|-------------------|
| MDC                 | 120     | O <sub>PU</sub>   |
| MDIO                | 121     | I/O <sub>PU</sub> |
| LED_CLK             | 122     | O <sub>PU</sub>   |
| LED_DAT             | 123     | I/O <sub>PU</sub> |
| UART0_TX/REG_IF_SEL | 124     | I/O <sub>PD</sub> |
| UART0_RX            | 125     | I <sub>PD</sub>   |
| DVDDL               | 126     | P                 |
| SPI_CS#0            | 127     | O                 |
| SPI_SI/SIO0         | 128     | I/O <sub>PD</sub> |
| SPI_SO/SIO1         | 129     | I/O <sub>PD</sub> |
| SPI_CLK             | 130     | O <sub>PD</sub>   |
| DVDDH               | 131     | P                 |
| VDDIO               | 132     | P                 |
| RESERVED            | 133     | I/O               |
| RESERVED            | 134     | I/O               |
| RESERVED            | 135     | I/O               |
| RESERVED            | 136     | I/O               |
| RESERVED            | 137     | I/O               |
| RESERVED            | 138     | I/O               |
| DVDDL               | 139     | P                 |
| RESERVED            | 140     | O                 |
| RESERVED            | 141     | O                 |
| RESERVED            | 142     | I/O               |
| RESERVED            | 143     | P                 |
| RESERVED            | 144     | I/O               |
| RESERVED            | 145     | I/O               |
| RESERVED            | 146     | I/O               |
| RESERVED            | 147     | I/O               |
| RESERVED            | 148     | O                 |
| RESERVED            | 149     | O                 |
| DIS_EEE             | 150     | I                 |
| PWRBLINK[0]         | 151     | I                 |
| PWRBLINK[1]         | 152     | I                 |
| SEL_XTAL_CLK        | 153     | I                 |
| SDS_PDOWN_EN        | 154     | I                 |
| SPI_ADDR_SEL        | 155     | I                 |
| LED/MODE[1]         | 156     | I                 |
| LED/MODE[0]         | 157     | I                 |
| RESERVED            | 158     | -                 |
| RESERVED            | 159     | -                 |
| DVDDL               | 160     | P                 |

| Name        | Pin No. | Type              |
|-------------|---------|-------------------|
| RESERVED    | 161     | -                 |
| VDDIO       | 162     | P                 |
| VDDIO       | 163     | P                 |
| RESERVED    | 164     | -                 |
| RESERVED    | 165     | -                 |
| CPU_SLEEP   | 166     | I/O <sub>PD</sub> |
| RESERVED    | 167     | -                 |
| RESERVED    | 168     | -                 |
| MEM_TYPE[1] | 169     | I/O <sub>PD</sub> |
| MEM_TYPE[0] | 170     | I/O <sub>PD</sub> |
| CLK_M_EE[1] | 171     | I/O <sub>PD</sub> |
| CLK_M_EE[0] | 172     | I/O <sub>PD</sub> |
| EN_DECRYPT  | 173     | I/O <sub>PD</sub> |
| RESERVED    | 174     | -                 |
| RESERVED    | 175     | -                 |
| RESERVED    | 176     | -                 |
| VDDIO       | 177     | P                 |
| DVDDL       | 178     | P                 |
| VX          | 179     | A                 |
| CKOUT0      | 180     | AO                |
| SVDDL       | 181     | AP                |
| S0TXP       | 182     | AO                |
| S0TXN       | 183     | AO                |
| S0RXP       | 184     | AI                |
| S0RXN       | 185     | AI                |
| SVDDH       | 186     | AP                |
| S1TXN       | 187     | AO                |
| S1TXP       | 188     | AO                |
| S1RXN       | 189     | AI                |
| S1RXP       | 190     | AI                |
| SVDDL       | 191     | AP                |
| DVDDL       | 192     | P                 |
| AVDDH       | 193     | AP                |
| P0MDIAP     | 194     | AI/O              |
| P0MDIAN     | 195     | AI/O              |
| P0MDIBP     | 196     | AI/O              |
| P0MDIBN     | 197     | AI/O              |
| AVDDL       | 198     | AP                |
| P0MDICP     | 199     | AI/O              |
| P0MDICN     | 200     | AI/O              |
| P0MDIDP     | 201     | AI/O              |
| P0MDIDN     | 202     | AI/O              |

| Name    | Pin No. | Type |
|---------|---------|------|
| AVDDH   | 203     | AP   |
| P1MDIAP | 204     | AI/O |
| P1MDIAN | 205     | AI/O |
| P1MDIBP | 206     | AI/O |
| P1MDIBN | 207     | AI/O |
| AVDDL   | 208     | AP   |
| P1MDICP | 209     | AI/O |
| P1MDICN | 210     | AI/O |

| Name     | Pin No. | Type |
|----------|---------|------|
| P1MDIDP  | 211     | AI/O |
| P1MDIDN  | 212     | AI/O |
| PLLVDDL  | 213     | AP   |
| ATESTCK0 | 214     | AO   |
| P2MDIAP  | 215     | AI/O |
| P2MDIAN  | 216     | AI/O |
| DGND     | EPAD    | G    |

## 7.5. Pin Descriptions (RTL8382L-VB)

### 7.5.1. 1000M Ethernet PHY MDI Interface Pins

**Table 31. 1000M Ethernet PHY MDI Interface Pins**

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P0MDIAP  | 194     | AI/O | Port 0 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P0MDIAN  | 195     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBP  | 196     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIBN  | 197     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICP  | 199     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDICN  | 200     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDP  | 201     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P0MDIDN  | 202     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIAP  | 204     | AI/O | Port 1 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P1MDIAN  | 205     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBP  | 206     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIBN  | 207     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICP  | 209     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDICN  | 210     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDP  | 211     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P1MDIDN  | 212     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIAP  | 215     | AI/O | Port 2 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P2MDIAN  | 216     | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBP  | 1       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIBN  | 2       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICP  | 4       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDICN  | 5       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDP  | 6       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P2MDIDN  | 7       | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIAP  | 9       | AI/O | Port 3 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P3MDIAN  | 10      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBP  | 11      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIBN  | 12      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICP  | 15      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDICN  | 16      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDP  | 17      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P3MDIDN  | 18      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P4MDIAP  | 37      | AI/O | Port 4 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P4MDIAN  | 38      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBP  | 39      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIBN  | 40      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICP  | 43      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDICN  | 44      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDP  | 45      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P4MDIDN  | 46      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIAP  | 48      | AI/O | Port 5 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P5MDIAN  | 49      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBP  | 50      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIBN  | 51      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICP  | 53      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDICN  | 54      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDP  | 55      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P5MDIDN  | 56      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIAP  | 59      | AI/O | Port 6 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P6MDIAN  | 60      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBP  | 61      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIBN  | 62      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICP  | 64      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDICN  | 65      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDP  | 66      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P6MDIDN  | 67      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIAP  | 69      | AI/O | Port 7 Media Dependent Interface A~D.<br>For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N.<br><br>Each of the differential pairs has an internal 100 ohm termination resistor. |
| P7MDIAN  | 70      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBP  | 71      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIBN  | 72      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICP  | 74      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDICN  | 75      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDP  | 76      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |
| P7MDIDN  | 77      | AI/O |                                                                                                                                                                                                                                                                                                                                                                       |

## 7.5.2. SGMII Interface Pins

**Table 32. SGMII Interface Pins**

| Pin Name | Pin No. | Type | Description                                             |
|----------|---------|------|---------------------------------------------------------|
| S4RXP    | 96      | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S4RXN    | 97      | AI   |                                                         |
| S4TXP    | 94      | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S4TXN    | 95      | AO   |                                                         |
| S5RXP    | 102     | AI   | SGMII Interface Receive Data Differential Input Pair.   |
| S5RXN    | 101     | AI   |                                                         |
| S5TXP    | 100     | AO   | SGMII Interface Transmit Data Differential Output Pair. |
| S5TXN    | 99      | AO   |                                                         |

## 7.5.3. QSGMII Interface Pins

**Table 33. QSGMII Interface Pins**

| Pin Name | Pin No. | Type | Description                                              |
|----------|---------|------|----------------------------------------------------------|
| S0RXP    | 184     | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S0RXN    | 185     | AI   |                                                          |
| S0TXP    | 182     | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S0TXN    | 183     | AO   |                                                          |
| S1RXP    | 190     | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S1RXN    | 189     | AI   |                                                          |
| S1TXP    | 188     | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S1TXN    | 187     | AO   |                                                          |
| S2RXP    | 84      | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S2RXN    | 85      | AI   |                                                          |
| S2TXP    | 82      | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S2TXN    | 83      | AO   |                                                          |
| S3RXP    | 90      | AI   | QSGMII Interface Receive Data Differential Input Pair.   |
| S3RXN    | 89      | AI   |                                                          |
| S3TXP    | 88      | AO   | QSGMII Interface Transmit Data Differential Output Pair. |
| S3TXN    | 87      | AO   |                                                          |

## 7.5.4. 1000Base-X/100Base-FX Interface Pins

**Table 34. 1000Base-X/100Base-FX Interface Pins**

| Pin Name | Pin No. | Type | Description                                                             |
|----------|---------|------|-------------------------------------------------------------------------|
| S4RXP    | 96      | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S4RXN    | 97      | AI   |                                                                         |
| S4TXP    | 94      | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S4TXN    | 95      | AO   |                                                                         |
| S5RXP    | 102     | AI   | 1000Base-X/100Base-FX Interface Receive Data Differential Input Pair.   |
| S5RXN    | 101     | AI   |                                                                         |
| S5TXP    | 100     | AO   | 1000Base-X/100Base-FX Interface Transmit Data Differential Output Pair. |
| S5TXN    | 99      | AO   |                                                                         |

## 7.5.5. Master Mode SPI Flash Interface Pins

**Table 35. Master Mode SPI Flash Interface Pins**

| Pin Name    | Pin No. | Type              | Drive (mA) | Description                                                                                                                                 |
|-------------|---------|-------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| SPI_CLK     | 130     | O <sub>PD</sub>   | 12         | Serial Clock Output Pin.                                                                                                                    |
| SPI_SO/SIO1 | 129     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip output pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is MSB first.</i> |
| SPI_SI/SIO0 | 128     | I/O <sub>PD</sub> | 12         | In Serial Mode: This is a flash chip input pin<br>In Dual Mode: This is a flash chip bi-directional pin<br><i>Note: This is LSB first.</i>  |
| SPI_CS#0    | 127     | O                 | 12         | Chip Select Output Pin.<br>Slave Transmit Enable and active low.                                                                            |

## 7.5.6. UART Interface Pins

**Table 36. UART Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                    |
|----------|---------|-------------------|------------|--------------------------------|
| UART0_RX | 125     | I <sub>PD</sub>   | 4          | UART0 Interface Receive Data.  |
| UART0_TX | 124     | I/O <sub>PD</sub> | 4          | UART0 Interface Transmit Data. |
| UART1_RX | 116     | I <sub>PU</sub>   | 4          | UART1 Interface Receive Data.  |
| UART1_TX | 117     | I/O <sub>PD</sub> | 4          | UART1 Interface Transmit Data. |

## 7.5.7. LED Interface Pins

**Table 37. LED Interface Pins**

| Pin Name | Pin No. | Type              | Drive (mA) | Description                                                                                                                                                                                         |
|----------|---------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LED_CLK  | 122     | O <sub>PU</sub>   | 12         | (1) In Serial LED Mode<br>Reference output clock for serial LED interface and Data is latched on the rising of LEDCK.<br>(2) In SMI-like LED Mode<br>Reference output clock for I2C-like interface. |
| LED_DAT  | 123     | I/O <sub>PU</sub> | 12         | (1) In Serial LED Mode<br>Serial bit stream of link status information.<br>(2) In I2C-like LED Mode<br>The data written to the LED IC.                                                              |

## 7.5.8. GPIO Interface Pins

**Table 38. GPIO Interface Pins**

| Pin Name  | Pin No.       | Type              | Drive (mA) | Description                                                                                   |
|-----------|---------------|-------------------|------------|-----------------------------------------------------------------------------------------------|
| GPIO0     | 113           | I/O <sub>PD</sub> | 4          | This pin default set as system LED.<br>Can be configured as General Purpose Input/Output Pin. |
| GPIO[3:1] | 110, 111, 112 | I/O <sub>PD</sub> | 4          | General Purpose Input/Output Pins.                                                            |

## 7.5.9. Configuration Strapping Pins

**Table 39. Configuration Strapping Pins**

| Pin Name       | Pin No.  | Default | Description                                                                                                          |
|----------------|----------|---------|----------------------------------------------------------------------------------------------------------------------|
| EEPROMTYPE     | 30       | 0b0     | Select EEPROM Address Byte Size.<br>0b0: 1-byte<br>0b1: 2-byte                                                       |
| REG_IF_SEL     | 124      | 0b0     | Select Switch Core Register Access Interface.<br>0b0: I2C<br>0b1: SPI slave                                          |
| DIS_PHYAUTO_UP | 117      | 0b0     | Disable ASIC Auto Power Up PHY.<br>0b0: Enable ASIC auto power up PHY<br>0b1: Disable ASIC auto power up PHY         |
| DIS_EEE        | 150      | 0b0     | Disable 1000M EEE and 100M EEE Function.<br>0b0: Enable<br>0b1: Disable                                              |
| PWRBLINK[1:0]  | 152, 151 | 0b00    | Select LED Power On Blinking Timer.<br>0b00: Disable<br>0b01: 800ms<br>0b10: 1.6s<br>0b11: 3.2s                      |
| SEL_XTAL_CLK   | 153      | 0b0     | Select XTAL Input is 25M or 125M.<br>0b0: 25M<br>0b1: 125M<br><i>Note: This option is only for sync Ethernet.</i>    |
| SDS_PDOWN_EN   | 154      | 0b0     | Enable SerDes Power Down Mode.<br>0b0: SerDes4/5 operate in normal mode<br>0b1: SerDes4/5 operate in power down mode |

| Pin Name      | Pin No.  | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPI_ADDR_SEL  | 155      | 0b0     | Select Address Mode for SPI Flash.<br>0b0: 3-byte address<br>0b1: 4-byte address                                                                                                                                                                                                                                                                                                                                                                                                         |
| LED_MODE[1:0] | 156, 157 | 0b0     | Select LED Mode.<br>0b00: Serial LED mode<br>0b10: Scan Bicolor mode<br>0b01: Scan Single mode<br>0b11: Disable LED                                                                                                                                                                                                                                                                                                                                                                      |
| CPU_SLEEP     | 166      | 0b0     | Enable CPU Function.<br>0b0: CPU is always under reset state<br>0b1: CPU is enabled                                                                                                                                                                                                                                                                                                                                                                                                      |
| MEM_TYPE[1:0] | 169, 170 | 0b00    | Select Memory Type for SOC.<br>0b00: Select SPI flash<br>0b10: Select SPI flash<br>0b01: Reserved<br>0b11: Select EEPROM                                                                                                                                                                                                                                                                                                                                                                 |
| CLK_M_EE[1:0] | 171, 172 | 0b00    | When MEM_TYPE Select is SPI Flash:<br>This Strapping Pin Selects the Initial Clock for The Memory Controller.<br>0b00: Reserved for test;<br>0b10: 100MHz<br>0b01: Reserved for test;<br>0b11: Reserved for test;<br><i>Note: The initial value for this strapping pin must be set as recommended in the reference design guide.</i><br><br>When MEM_TYPE Select is EEPROM:<br>CLK_M_EE[0] is used to select SOC EEPROM address byte size.<br>0b0: 1-byte address<br>0b1: 2-byte address |
| EN_DECRYPT    | 173      | 0b0     | Enable or Disable Decrypt for Flash.<br>0b0: Disable decrypt<br>0b1: Enable decrypt                                                                                                                                                                                                                                                                                                                                                                                                      |

## 7.5.10. Miscellaneous Interface Pins

**Table 40. Miscellaneous Interface Pins**

| Pin Name         | Pin No.                                                                                                                                          | Type              | Drive (mA) | Description                                                                                                                                                     |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDC              | 120                                                                                                                                              | O <sub>PU</sub>   | 12         | MII Management Interface Clock Pin.                                                                                                                             |
| MDIO             | 121                                                                                                                                              | I/O <sub>PU</sub> | 12         | MII Management Interface Data Pin.                                                                                                                              |
| SSPI_CLK/I2C_CLK | 119                                                                                                                                              | I/O <sub>PU</sub> | 4          | SPI Serial Clock Input (Slave Mode).<br>I2C Interface Clock Input (Slave Mode).<br>I2C Interface Clock Output (Master Mode).                                    |
| SSPI_SI/I2C_DAT  | 118                                                                                                                                              | I/O <sub>PU</sub> | 4          | SPI Serial Data Input (Slave Mode).<br>I2C Interface Bi-Directional data (Slave Mode).                                                                          |
| SSPI_SO          | 117                                                                                                                                              | I/O <sub>PD</sub> | 4          | SPI Serial Data Output (Slave Mode).                                                                                                                            |
| SSPI_CS#         | 116                                                                                                                                              | O <sub>UP</sub>   | 4          | SPI Serial Chip Select (Slave Mode).                                                                                                                            |
| RESET#           | 114                                                                                                                                              | AI                | -          | System Pin Reset Input (Low Active).<br>To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled up for normal operation. |
| XI               | 106                                                                                                                                              | AI                | -          | 25MHz Crystal Clock Input and Feedback Pin.                                                                                                                     |
| XO               | 105                                                                                                                                              | AO                | -          | 25MHz Crystal Clock Output Pin.                                                                                                                                 |
| MDIREF           | 21                                                                                                                                               | AO                | -          | MDI Bias Resistor.<br>Adjust the reference current for all PHYs. This pin must connect to AGND via a 2.49k ohm resistor.                                        |
| RTT1             | 23                                                                                                                                               | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| RTT2             | 24                                                                                                                                               | AI/O              | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| VX               | 179                                                                                                                                              | A                 | -          | Low Voltage Power Control Resistor.                                                                                                                             |
| CKOUT0           | 180                                                                                                                                              | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |
| CKOUT2           | 80                                                                                                                                               | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |
| CKOUT4           | 92                                                                                                                                               | AO                | 8          | 25MHz Clock Output.                                                                                                                                             |
| ATESTCK[1:0]     | 58, 214                                                                                                                                          | AO                | -          | Reserved for Internal Use (Must be Left Floating).                                                                                                              |
| RESERVED         | 28, 29, 31, 32, 133, 134, 135, 136, 137, 138, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 158, 159, 161, 164, 165, 167, 168, 174, 175, 176 | -                 | -          | Reserved (Must be Left Floating).                                                                                                                               |

## 7.5.11. Power and Ground Pins

**Table 41. Power and Ground Pins**

| Pin Name  | Pin No.                                           | Type | Description                     |
|-----------|---------------------------------------------------|------|---------------------------------|
| AVDDL     | 3, 13, 22, 42, 52, 63, 73, 198, 208               | AP   | Analog Low Voltage Power.       |
| PLLVDL    | 57, 213                                           | AP   | Analog PLL Low Voltage Power.   |
| AVDDH     | 8, 14, 19, 25, 36, 41, 47, 68, 78, 193, 203       | AP   | Analog High Voltage Power.      |
| DVDDL     | 26, 33, 34, 79, 108, 109, 126, 139, 160, 178, 192 | P    | Digital Low Voltage Power.      |
| DVDDH     | 27, 35, 115, 131                                  | P    | Digital High Voltage Power.     |
| SVDDL     | 81, 86, 93, 98, 103, 181, 191                     | AP   | SerDes Low Voltage Power.       |
| AVDDL_PLL | 107                                               | AP   | PLL Low Voltage Power.          |
| SVDDH     | 91, 186                                           | AP   | SerDes High Voltage Power.      |
| AVDDH_PLL | 104                                               | AP   | PLL High Voltage Power.         |
| VDDIO     | 132, 162, 163, 177                                | P    | Strapping pin IO Voltage Power. |
| AGND      | 20                                                | AG   | Analog Ground.                  |
| DGND      | E-PAD                                             | G    | Digital Ground.                 |

## **8. Switch Function Description**

### **8.1. *Hardware Reset and Software Reset***

#### **8.1.1. Hardware Reset**

A hardware reset forces the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB to start the initial power-on sequence. First hardware will strap pins to give all default values when the 'RESET' signal terminates. Next the complete SRAM BIST (Built-In Self Test) process is run. Finally the packet buffer descriptors are initialized and internal registers and external CPU will access them.

#### **8.1.2. Software Reset**

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports software queue resets, CPU&Memory reset, and Switch NIC reset. Reset sources are the signals that will trigger the reset command to the chip.

- CPU&Memory Reset: Resets MIPS 4KEc + Memory Controller + Peripheral + NIC
- Switch NIC Reset: Resets the NIC interface between the CPU and Switch

### **8.2. *Crystal***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB clock input frequency is 25MHz. When using a crystal, connect a loading capacitor from XI and XO to ground. The maximum Frequency Tolerance is +/-50ppm. Duty cycle should range from 40%~60%.

### **8.3. *IEEE 802.3az Energy Efficient Ethernet (EEE)***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports IEEE 802.3az Energy Efficient Ethernet (EEE) for 1000Base-T, 100Base-TX in full duplex operation, and supports 10Base-T for 10Base-T in full/half duplex. The Energy Efficient Ethernet (EEE) operational mode combines the IEEE 802.3 Media Access Control (MAC) Sub-layer with a family of Physical Layers defined to support operation in Low Power Idle (LPI) Mode. When Low Power Idle Mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB EEE operational mode supports IEEE 802.3 MAC operation at 1000Mbps/100Mbps. For 1000Mbps/100Mbps operation, the 1000Base-T/ 100Base-TX PHY is supported. In addition, the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports a 10Mbps PHY with reduced transmit amplitude requirements in EEE operational mode. This new PHY is fully interoperable with legacy 10Base-T PHYs over 100m of Class-D (Category 5) or better cabling.

## 8.4. Layer 2 Learning and Forwarding

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB has a 4K-entry VLAN table and provides a 64-entry filtering database.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports IVL (Individual VLAN Learning) and SVL (Shared VLAN learning) mode. The mode used depends on the FID (Filtering Identifier) setting.

### 8.4.1. Forwarding

IP multicast data packets involve multicast group table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to all member ports and router ports. If the multicast address is not stored in the address table (i.e., lookup miss), the packet is broadcast to all ports of the broadcast domain. The VLAN Frame Forwarding Rules are defined as follows:

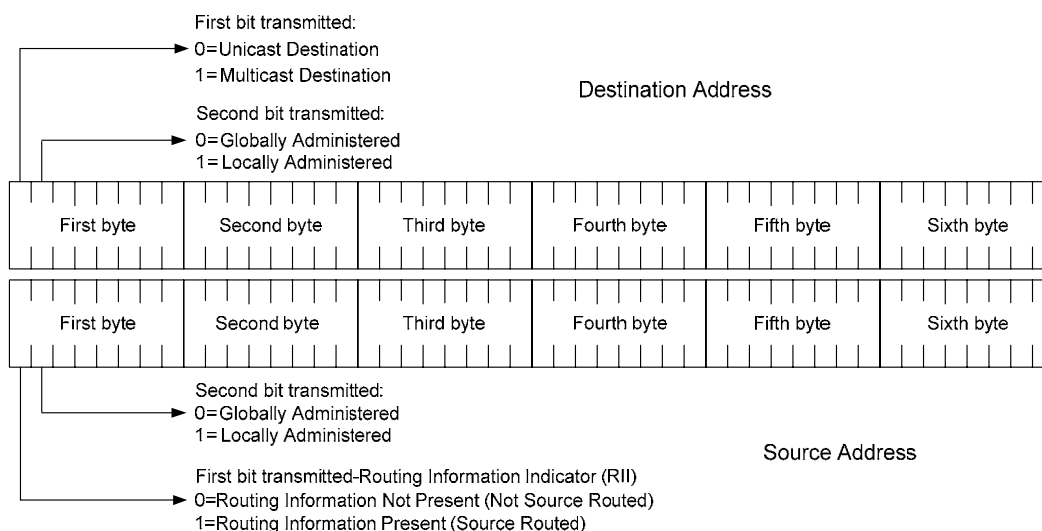
- The received broadcast/multicast frame will flood to VLAN member ports only, except for the source port
- The received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded

### 8.4.2. Learning

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB features a Layer 2 table (8K entries) that uses a 4-way hash structure to store L2 entries. Each entry can be recorded in three formats, L2 Unicast, L2 Multicast, and IP Multicast.

The L2 Unicast hash key is {MAC(48bits), FID/VID(12bits)}; the Multicast hash key is {MAC(48bits), FID/VID(12bits)}; the IP Multicast hash key is {MAC(48bits), FID/VID(12bits)}, {GIP(32bits), SIP(32bits)} or {0(16bits)+GIP(32bits), FID/VID(12bits)}.

### 8.4.3. DA/SA Block



**Figure 11. DA/SA Block**

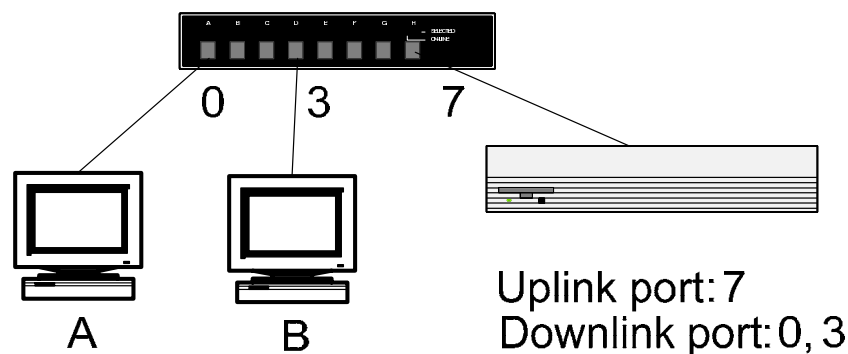
While a frame may be sent to either a unicast or a multicast destination, frames are always sent from an individual station. The first bit of the Destination Address shows unicast or multicast. When used in its originally intended manner, the first bit of a Source Address should always be 0, indicating an individual sending station.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB features DA blocking, SA blocking, or DA and SA blocking function through the Address Hash Table setting.

## 8.5. Port Isolation

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports the Port Isolation feature. We can control whether the hosts communicate with each other or not by controlling a register value.

If we set the register to cut the connection between hosts, all packets from a host cannot be transmitted to another host directly. These packets can only be transmitted by passing through the router. This feature is called ‘Port Isolation’. In Figure 12, Host A and host B connect to the port0 and port3 of the switch, respectively, and port7 is a router. If we set the port isolation enable bit of port0 and port3 to 1, all packets between A and B need to pass through the router (in both directions, A to B and B to A).



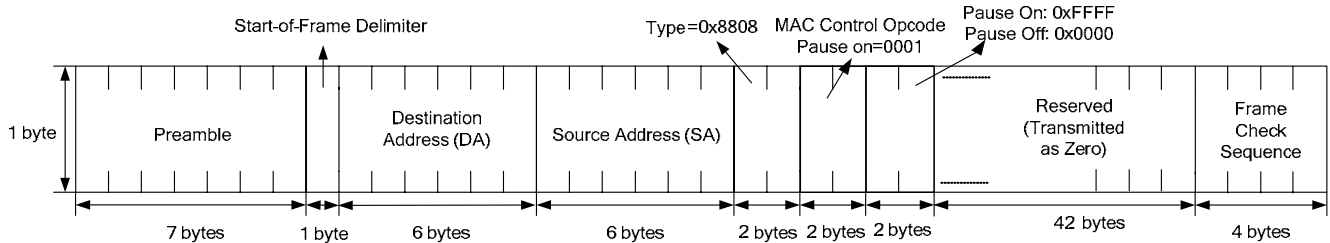
**Figure 12. Port Isolation Example**

Each port has its own port mask configuration (11 bits in total for the RTL8380M-VB, 29 bits for the RTL8382M-VB/RTL8382L-VB). These bits and the TX port list will be mixed to a list. We call this mixed list the final TX port list.

Port isolation port mask settings will affect received packets; however, the Mirroring function is not affected by the port isolation port mask.

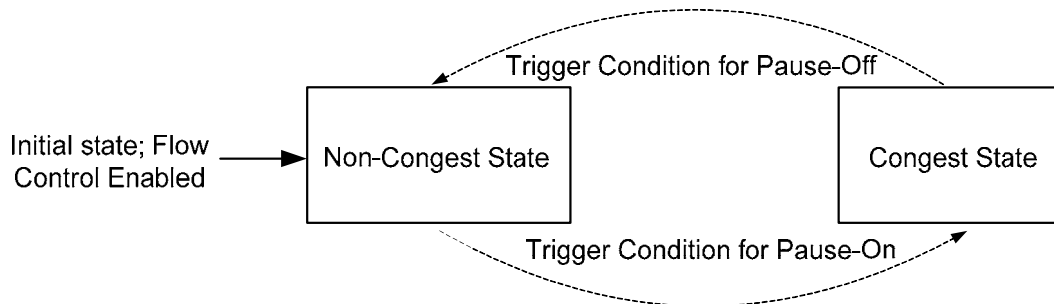
## 8.6. IEEE 802.3x Flow Control

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports IEEE 802.3x full duplex flow control. If one port's received frame buffer is over the pause threshold, a pause-on frame is sent to indicate to the link partner to stop the transmission. When the port's received frame buffer drops below the pause threshold, it sends a pause-off frame. The TX pause frame format is shown in Figure 13.



**Figure 13. TX Pause Frame Format**

The flow control mechanism of the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB is implemented on the RX side. It counts the received pages on the RX side in order to determine on which port it should send out Pause On/Off packets.



**Figure 14. Flow Control State Machine**

When RTL8380M-VB/RTL8382M-VB/RTL8382L-VB flow control is enabled, the initial state is 'Non\_Congest'. The state is monitored continuously. If a pause-on trigger condition occurs, it enters the 'Congest' state. When in the 'congest' state, it is also continuously monitored. When a pause-off trigger condition occurs it re-enters the 'Non\_Congest' state. Figure 14 shows the flow control state machine.

## 8.7. Half Duplex Backpressure

There are two mechanisms for half duplex backpressure (Backpressure is for input buffer overflow).

### 8.7.1. Collision-Based Backpressure (Jam Mode)

If the input buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- When the link partner detects the collision, it waits for a random backoff time. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will handle packets that are in the input packet buffer during this time
- RXDV and TXEN will be driven high. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will send a 12-byte Jam signal (pattern is preamble (7bytes) + SFD (1byte) + 0xAA (4bytes)). The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will then drive TXEN low
- When the link partner (which could be another RTL8380M-VB/RTL8382M-VB/RTL8382L-VB) receives the Jam signal, it will feedback a 4-byte signal (pattern is derived from the CRC of all transmitted bytes)
- After the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB receives this jamming signal, it drives RXDV low. The link partner waits for a random backoff time then re-sends the packet. The timing is shown in Figure 15

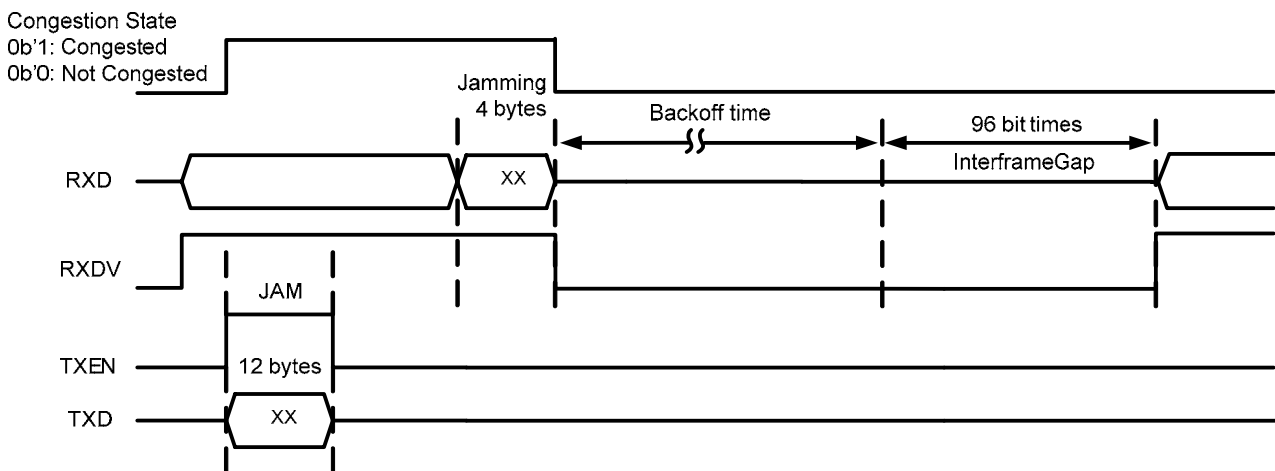


Figure 15. Signal Timing for Collision-Based Backpressure

### 8.7.2. Carrier-Based Backpressure (I.e., Defer Mode)

If the input buffer is about to overflow, this mechanism will send a fix pattern to defer the other station's transmission. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will continuously send the defer signal until the input buffer overflow is resolved.

## 8.8. Layer 2 Multicast and IP Multicast

There are two RTL8380M-VB/RTL8382M-VB/RTL8382L-VB IP multicast frame types: IPv4 multicast and IPv6 multicast.

An IPv4 multicast frame must satisfy two conditions:

- The type must be IPv4
- DMAC should=01-00-5E-XX-XX-XX

An IPv6 multicast frame must satisfy two conditions:

- The type must be IPv6
- DMAC should=0x33-33-XX-XX-XX-XX

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB definition of a L2 multicast packet is that the packet is not an IP multicast packet, and the I/G bit of the MAC address is 1.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports IGMPv1/2/3. IGMP and MLDv1/2 packets can be trapped to the CPU to allow software to insert an IP multicast entry into the L2 table.

## 8.9. IEEE 802.1d/1w/1s (STP/RSTP/MSTP)

There are 64 spanning tree instances for the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB. The CPU will create a different Port State for different spanning tree instances at each port.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will assign a VID for a received packet, and will look up the VLAN table to check for Multiple Spanning Tree Instances (MSTI).

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB will follow the ports MSTI state to complete its corresponding ingress/egress check. The Spanning Tree and Rapid Spanning Tree port states are shown in Figure 16.

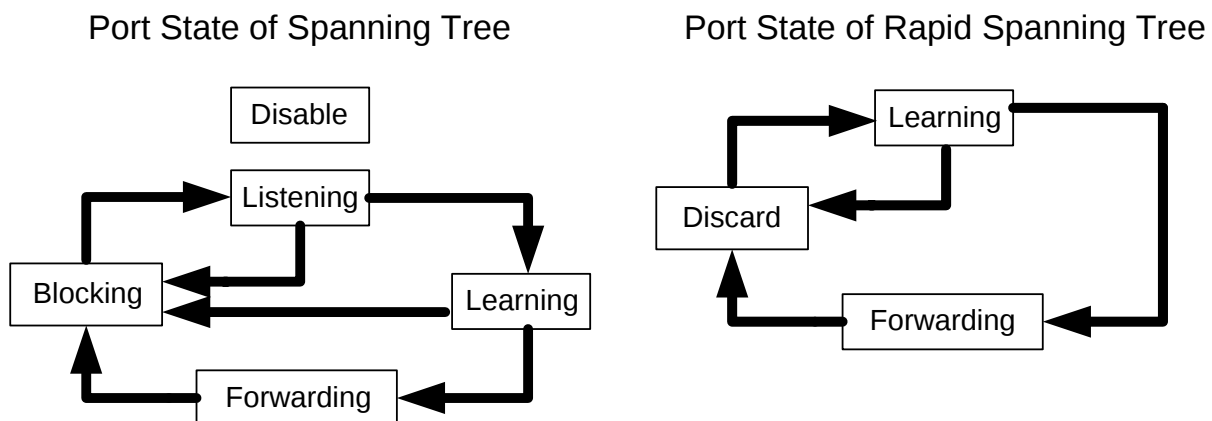


Figure 16. Spanning Tree and Rapid Spanning Tree Port States

When using IEEE 802.1D, the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports four status' for each port:

### Disabled

Except for software forwarding, the port will not transmit/receive packets, and will not perform learning.

### Blocking/Listening

Except for software forwarding, the port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

### Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

### Forwarding

The port will transmit/receive all packets, and will perform learning.

There are five Spanning Tree port states, and four Rapid Spanning Tree port states. Their mapping relations are Discarding→Blocking, Learning→Learning, and Forwarding→Forwarding (see Table 42).

**Table 42. Spanning Tree and Rapid Spanning Tree Action**

|                | Spanning Tree |          |           |          |            | Rapid Spanning Tree |          |            |
|----------------|---------------|----------|-----------|----------|------------|---------------------|----------|------------|
|                | Disable       | Blocking | Listening | Learning | Forwarding | Discard             | Learning | Forwarding |
| Receive BPDUs  | No            | Yes      | Yes       | Yes      | Yes        | Yes                 | Yes      | Yes        |
| Transmit BPDUs | No            | No       | Yes       | Yes      | Yes        | No                  | Yes      | Yes        |
| Learn Address  | No            | No       | No        | Yes      | Yes        | No                  | Yes      | Yes        |
| Forward Frame  | No            | No       | No        | No       | Yes        | No                  | No       | Yes        |

## 8.10. IEEE 802.1p and IEEE 802.1Q (VLAN)

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports IEEE 802.1Q tag-based, protocol-and-port-based, port-based, MAC-based, IP-subnet-based, and application-based VLANs. It supports a 4K-entry VLAN table, supporting C-VID (Customer VLAN ID) and FID (Filtering Identifier) entries. There are 6 fields in the VLAN table, and their definitions are as below.

- MBR: Determines whether the packets belong to the same VLAN
- UNTAG: Determines whether Egress packets have a VLAN tag
- FID\_MSTI: Gets different FIDs (Filtering Identifier) or determines the index of multiple spanning tree instances from different VLANs
- L2\_HKEY\_UBCAST: Determines the hash key (VID or FID) for L2 unicast and broadcast traffic
- L2\_HKEY\_MCAST: Determines the hash key (VID or FID) for L2 multicast and IP multicast traffic
- VLAN\_PROFILE: Determines the index of the VLAN profile

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports eight global VLAN profiles. Each VLAN profile has the following configurations:

- L2\_LRN\_EN: Enable L2 SA learning
- L2\_UNKN\_MC\_FLD\_PMSK: Unknown L2 multicast flooding port mask
- IP4\_UNKN\_MC\_FLD\_PMSK: Unknown IPv4 multicast flooding port mask
- IP6\_UNKN\_MC\_FLD\_PMSK: Unknown IPv6 multicast flooding port mask

For un-managed switches, there is a register setting to disable tag-based VLANs and force ‘no check’ for any VLAN settings. If a packet is tagged in, then it is tagged out. If untagged in, then it is untagged out.

- The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports ingress and egress VLAN filtering functions
- Ingress VLAN filtering: Packets from an input port that is not in the VLAN member set will be dropped, trapped, or forwarded depending on register configuration
- Egress VLAN filtering: Packets to an output port that is not in the VLAN member set will be dropped, trapped, or forwarded depending on register configuration

## ***8.11. IEEE 802.1X (Network Access Control)***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provides a software solution for 802.1X.

When a host connects to a switch, the switch will transfer the host information to an authentication server:

- If authentication is successful, the switch will set the control bit of this port to ‘TRUE’ (i.e., the host will be allowed the service)
- If authentication is not successful, the switch will deny the host access to the network

The CPU port can be regarded as a special port where transmit and receive packets are unrestricted for 802.1X.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports two types of 802.1X; Port-Based Network Access Control, and MAC-Based Network Access Control.

- Port-Based Network Access Control: For each port, there is a bit to check whether this port has passed authentication or not. A direction control register decides whether this port needs pass-through authentication for both (IN/OUT) directions or only for receive (IN)
- MAC-Based Access Control: Provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. There is a register that enables/disables each logical port MAC-based network access control function. Another register controls transmit/receive direction authentication for each port (IN/OUT) or only receive direction (IN)

Table 43 illustrates the forwarding of host n.

**Table 43. Forwarding of Host n**

| Authentication of Host n | Direction of Whole Chip | Fwd Frames to Host n | Fwd Frames from Host n |
|--------------------------|-------------------------|----------------------|------------------------|
| 0 (Unauthorized)         | 0 (BOTH)                | No                   | No                     |
| 0 (Unauthorized)         | 1 (IN)                  | Yes                  | No                     |
| 1 (Authorized)           | 0 (BOTH)                | Yes                  | Yes                    |
| 1 (Authorized)           | 1 (IN)                  | Yes                  | Yes                    |

## 8.12. *Reserved Multicast Address Handling*

There are some Reserved Multicast Address (RMA) definitions in the IEEE 802.1 standard. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB includes 01-80-C2-00-00-00 to 01-80-C2-00-00-2F RMA support and provides user defined RMA settings. For each RMA, the actions include: Table lookup, Drop, Trap to CPU, and always Flood. The action priority is higher than the results of a L2 Table lookup. Default actions are shown in Table 44.

**Table 44. Reserved Multicast Address Default Actions**

| Name                                                                  | Address                                                      | Default |
|-----------------------------------------------------------------------|--------------------------------------------------------------|---------|
| Bridge Group Address                                                  | 01-80-C2-00-00-00                                            | Forward |
| IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation             | 01-80-C2-00-00-01                                            | Drop    |
| IEEE Std 802.3ad Slow Protocols-Multicast Address                     | 01-80-C2-00-00-02                                            | Drop    |
| IEEE Std 802.1X PAE Address                                           | 01-80-C2-00-00-03                                            | Forward |
| Reserved for future protocol standards                                | 01-80-C2-00-00-04 to 01-80-C2-00-00-0D,<br>01-80-C2-00-00-0F | Drop    |
| LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address | 01-80-C2-00-00-0E                                            | Forward |
| All LANs Bridge Management Group Address                              | 01-80-C2-00-00-10                                            | Drop    |
| GMRP                                                                  | 01-80-C2-00-00-20                                            | Drop    |
| GVRP                                                                  | 01-80-C2-00-00-21                                            | Forward |
| Reserved for use by Multiple Registration Protocol (MRP) applications | 01-80-C2-00-00-22 to 01-80-C2-00-00-2F                       | Drop    |

### ***8.13. Layer 2 Traffic Suppression (Storm Control)***

The per-port L2 storm filtering control mechanism suppresses the flow rate of some specific packets. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports five control types: Unknown Unicast Storm, Unicast Storm, Unknown Multicast Storm, Multicast Storm, and Broadcast Storm. Each port has control registers to enable or disable the storm filtering function. These five traffic type definitions are:

- Unknown Unicast: If the I/G bit of the packet's destination address is 0, it is a unicast packet and its DA look-up in the L2 unicast table failed. I.e., the packet's destination address is unknown
- Unicast: The unicast storm filtering control includes unknown and known unicast for RTL8380M-VB/RTL8382M-VB/RTL8382L-VB
- Unknown Multicast: If the I/G bit of the packet's destination address is 1, it is a multicast packet and its DA look-up in the L2 unicast table failed, i.e., the packet's destination address is unknown
- Multicast: The multicast storm filtering control includes unknown and known multicast for RTL8380M-VB/RTL8382M-VB/RTL8382L-VB
- Broadcast: DMAC = FF-FF-FF-FF-FF-FF indicates this is a broadcast packet

Unknown Unicast and Unicast use the same traffic counter, and Unknown Multicast and Multicast use the same traffic counter. The user should set the Unicast and Multicast storm type as unknown or both known and unknown in the storm filter setting.

The traffic rate for these five types can be set on a per-port basis. The priority sequence of L2 filtering control is:

1. Input bandwidth control
2. ACL policy
3. Storm-filtering control

### ***8.14. PIE (Packet Inspection Engine)***

PIE is a 1.5K-entry search engine that is divided into 12 blocks (block numbers are 0~11). Each block size is 128-entries. Every entry has 216-bit data, and a 216-bit mask. There is an extra bit to indicate whether this entry is valid or not. Each block can be disabled for power saving when it is not used. All the entries are prepared for ingress ACL.

#### **8.14.1. Ingress ACL**

The Ingress ACL (Access Control List) perform actions such as packet drop, forwarding, ingress I-VID Assignment, Ingress O-VID Assignment, filter, log, remarking, meter, mirror etc. When a packet hits one entry it will execute the corresponding action mapped to this entry. Each PIE memory entry corresponds to one action entry. The packet can match to multi-actions. When a multi-match occurs (i.e., there are several ACL entries that match) in one block, it will execute the lowest address entry corresponding action.

## ***8.15. Input Bandwidth Control and ACL Traffic Meter***

### **8.15.1. Input Bandwidth Control**

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB has input bandwidth control for each port (excluding the CPU port). The bandwidth setting range is 16Kbps~1Gbps. The granularity is 16Kbps, and each port has a 16-bit register to control the bandwidth. If the speed of received packets is faster than the bandwidth setting, it will send a 'Pause ON' packet to slow the link partner transmissions when the flow control function is enabled, and drop packets when the flow control function is disabled. When normal transmissions become possible and the flow control function is enabled, the switch will send a 'Pause OFF' packet.

### **8.15.2. ACL Traffic Meter**

For Ingress ACL entry, there is an index to point to 256 ACL rate-limited entries. The rate limit is flow controlled via leaky bucket. The rate range is 16Kbps~1Gbps, the granularity is 16Kbps, and each rate-limited entry has a 16-bit register to control the rate value.

## ***8.16. IEEE 802.3ad Link Aggregation Protocol***

To ensure correct frame ordering when changing the hash algorithm, the marker protocol mechanism must be started. Software will wait for the aggregation port queues to empty, and then send a marker message to all aggregation ports. After receiving a marker reply packet, software can change the hash algorithm.

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports 802.3ad (Link Aggregation) for 8 groups of link aggregators with up to 8 ports per-group (based on DMAC/SMAC/SPA/SIP/DIP/SPORT/DPORT). The CPU port cannot be aggregated to an aggregation port. As the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB does not check CPU port aggregation, software should check this to avoid frame transmit errors.

### **Frame Distribution**

Link aggregation group frames are sent to an aggregation port of the link aggregation group according to a hash algorithm. There are seven parameters (DMAC, SMAC, SPA, SIP, DIP, SPORT, DPROT). To prevent assigning the same hash value when hash keys simultaneously change to another value, we stagger the least significant bit of all hash keys.

### **Mapping a Physical Port to a Logical Port**

No matter how many physical aggregation port members are in a link aggregation group, it is regarded as one logical port. Each link aggregation has an ID (the lowest number of the physical aggregation port members is used as its ID). Once the ID is chosen, even if the logical port ID's corresponding physical port is link down, the ID and setting of the link aggregation group will not change. However, it will change when this corresponding port is removed or a lower-numbered port is added.

## Hash Algorithm Change

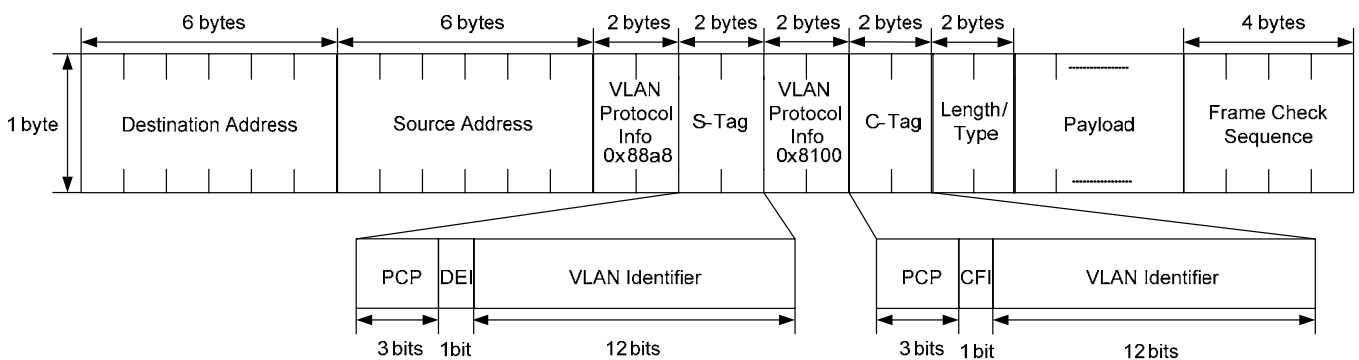
The algorithm will change when the following conditions occur:

- The link aggregation group member port changes to link-down or link-up
- The user/LACP (i.e., Link Aggregation Control Protocol) changes the link aggregation group member port or register setting

## 8.17. IEEE 802.1ad VLAN Stacking

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports multi-layered VLANs and can have Outer-VLAN and Inner-VLAN tagging. Standard 802.1ad takes the S-tag (Service VLAN tag) as the relay VID. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB uses the Outer-tag as S-tag, and the Inner-tag as C-tag to support 802.1ad applications.

The IEEE 802.1ad frame format is shown in Figure 17.



**Figure 17. IEEE 802.1ad Frame Format**

## 8.18. *Quality of Service (QoS)*

There are 5 types of Priority Assignment for the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB:

- Port-based Inner-tag Priority
- Port-based Outer-tag Priority
- Inner-tag-based Priority
- Outer-tag-based Priority
- DSCP-based Priority

These priority assignments will pass through the whole system priority selection table to decide the packets internal priority. Afterwards the internal priority will point to the adaptive output queue ID table.

### Priority Selection Tables

A received packet may be assigned up to five different priorities. These priorities are coordinated into a final priority according to the priority selection table Figure 18. Each priority assignment has a control register. The corresponding bit set to 1, sets the priority from high bit to low bit.

Inner-tag-based priority, Outer-tag-based priority, and DSCP-based priority may be NULL.

The priority arbiter should check whether the item is NULL or not. The NULL item priority corresponds to the lowest priority arbitration value; the bigger the corresponding priority arbitration value, the higher the priority assignment.

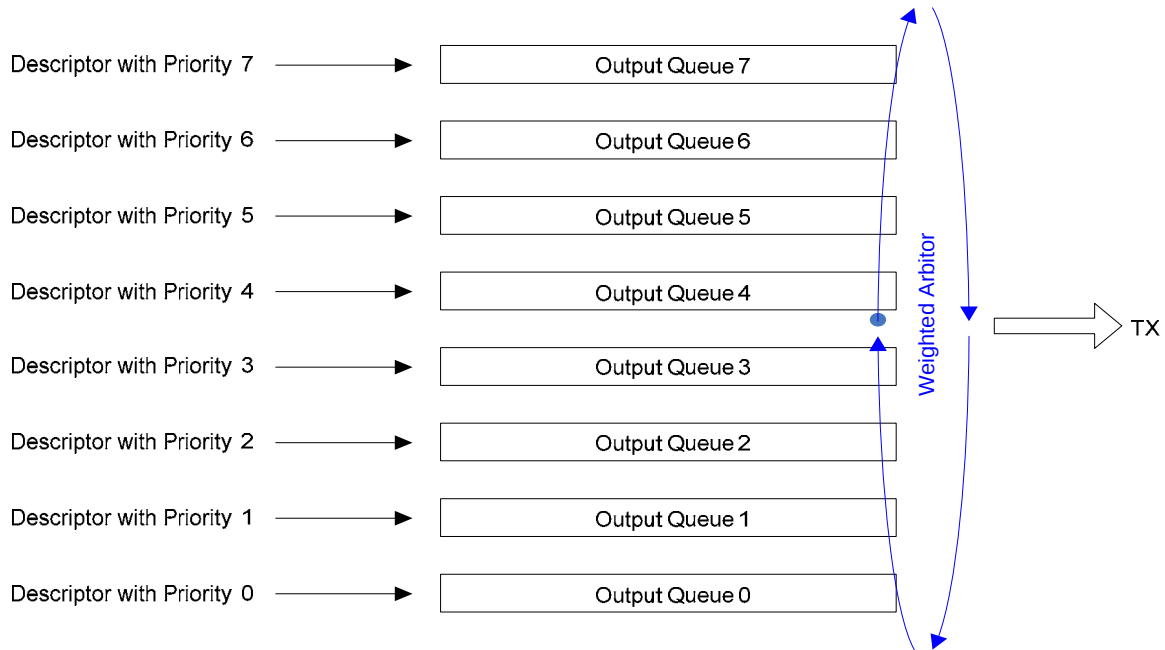
We can take an example to describe the priority order. The order is Inner-tag-based priority assignment > DSCP-based priority assignment > Outer-tag based priority assignment > Port-based Inner-tag Priority assignment = Port-based Outer-tag Priority assignment.

|                                                 | <i>Priority weight</i> |
|-------------------------------------------------|------------------------|
| <i>Port-based Inner-tag Priority Assignment</i> | 1                      |
| <i>Port-based Outer-tag Priority Assignment</i> | 1                      |
| <i>DSCP-based Priority Assignment</i>           | 6                      |
| <i>Inner-tag-based Priority Assignment</i>      | 7                      |
| <i>Outer-tag-based Priority Assignment</i>      | 5                      |

**Figure 18. Priority Selection Table Weight Rules Example**

### Internal Priority to Queue ID Table

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB can transfer its internal priority setting (see Figure 19) to the output queue ID. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB can configure each port's output queue level (including the CPU port). Each port has eight output queues.



**Figure 19. Per-Port Queue Management**

## 8.19. Packet Scheduling (WRR and WFQ)

The Packet Scheduler controls the various traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB scheduling algorithm is divided into Weighted Fair-Queuing (WFQ) and Weighted Round-Robin (WRR). Note that the Strict Priority queue is the highest priority of all queues, and overrides WFQ & WRR. A larger strict priority queue ID indicates the priority is higher.

The Scheduler operates as follows:

- Weighted Fair-Queuing (WFQ): Byte-count
- Weighted Round-Robin (WRR): Packet-count

WFQ and WRR cannot exist at the same time. WFQ or WRR can co-exist with Strict Priority Schedule. Both WFQ and WRR are round robin, from large queue ID to small.

## ***8.20. Packet Drop Algorithm (TD)***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports Tail Drop (TD).

- Tail Drop (TD): For a drop threshold value, if a packet meets queue overflow conditions before entering the output queue, the switch will drop this packet

## ***8.21. Egress Packet Remarking***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB Remarking can be divided into Inner-tag remarking, Outer-tag remarking, and DSCP remarking.

- For Inner-tag remarking, there is an internal priority to inner-tag priority remarking table that is used to configure the final user inner-tag priority value for per-port egress of a packet
- For Outer-tag remarking, there is an internal priority to outer-tag priority remarking table that is used to configure the final Outer-tag priority value for per-port egress of a packet
- DSCP remarking also has an internal priority to DSCP priority table for per-port egress of a packet

## ***8.22. Ingress and Egress Port Mirror***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB has four mirror sets (set0~3), and the Mirroring port can monitor several mirrored ports simultaneously. RX mirror and TX mirror function is supported by setting a source port mask, destination port mask. The mirror function can be configured across VLANs. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports a mirror filtering function to filter forwarded traffic. Only mirrored traffic can egress through a mirroring port.

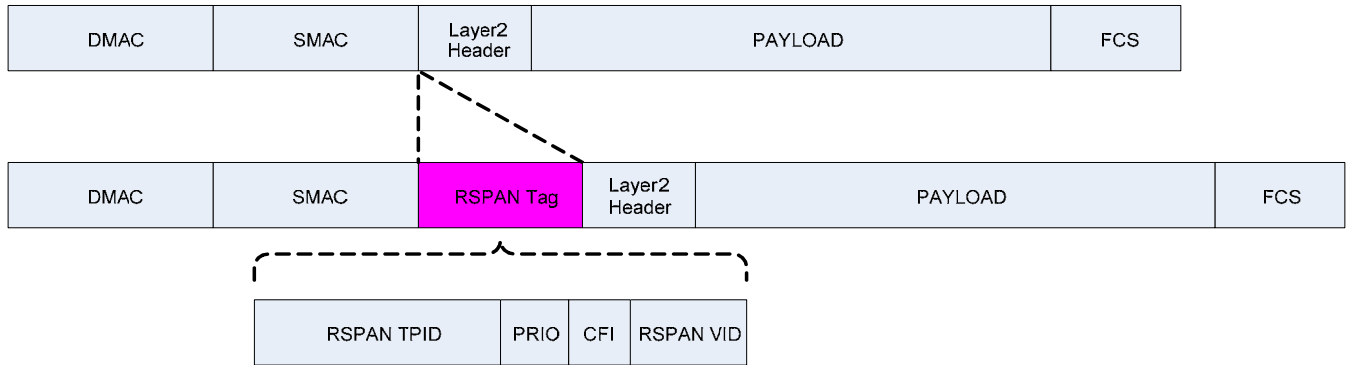
The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provide a flexible flow-based mirror function. In a flow-based mirror, only specified packets will be mirrored through a configured ACL action and fill a corresponding traffic mirror table entry.

For flow control, the mirroring port will drop the mirrored packets and send PAUSE frames or backpressure signals to the mirrored port for normal packets. It will resume mirror function when flow control is back to normal status. The design limitations for mirroring settings are as below.

- Each mirror entry can only set one mirroring port
- A mirroring port cannot be a member of a trunk group
- The mirroring port is not limited by port isolation for mirrored packets

### 8.22.1. Remote Mirror (RSPAN)

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB support Remote Switched Port Analyzer (RSPAN) to analyze a remote device's traffic flow. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB defined RSPAN VLAN tag is illustrated in Figure 20. Users can configure the RSPAN tag's TPID/VID/Priority/CFI at each port. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB can parse for the RSPAN tag in RX and add or remove RSPAN tags in TX.

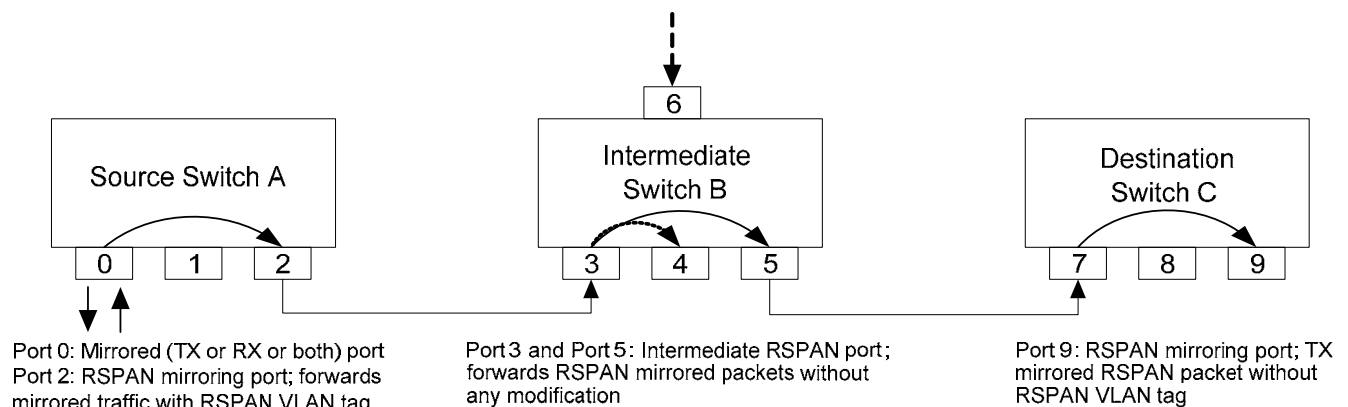


**Figure 20. RSPAN Encapsulation**

Figure 21 shows an example of an RSPAN application. In Source Switch A, Port0 is configured as a mirrored port, and Port2 as a mirroring port with setting 'TX added RSPAN tag'.

In Intermediate Switch B, Port3 and Port5 are added as RSPAN VLAN members. RSPAN mirrored packets will be forwarded without any modification.

In Destination Switch C, Port7 and Port9 join as RSPAN VLAN members, with Port9 configured to 'Remove RSPAN tag in TX'. This means packets are mirrored from Source Switch A Port0 to Destination Switch C Port9 without modification.



**Figure 21. RSPAN Illustration**

### 8.23. Management Information Base (MIB)

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB MIB (Management Information Base) counters include:

- Ethernet-like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (Remote Network Monitoring) MIB (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

### 8.24. NIC and CPU Tag Forwarding

NIC interface: This is used for receiving packets from the CPU, or transmitting packets to the CPU. The architecture is shown in Figure 22.

When a packet is sent from the switch core to the CPU port, the CPU tag can carry status information. The CPU tag can be divided into a transmit CPU tag, and a receive CPU tag.

- Transmit CPU Tag: Forces TX port mask. Indicates which ports the packet will NOT be sent to. For example, if we set port1, port2, and port5 mask bits, then the packet will not be sent to these ports
- Receive CPU Tag: Indicates which RX port the packet came from

If no CPU tag is attached, the normal process will be followed to perform a look-up in the L2 table.

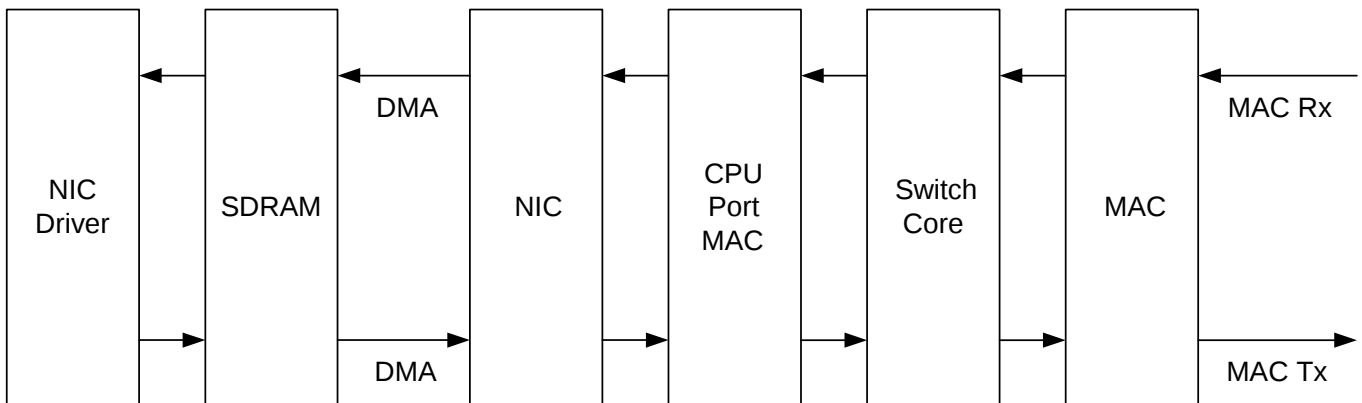


Figure 22. NIC Architecture

## ***8.25. Indirect Table Access***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB employs an indirect method to set the control register and the data register to complete a VLAN/L2 Lookup/ Forwarding/SPT/ACL Table Access:

1. Sets the register to determine which table and which entry is to be accessed
2. Determines the read or write action
3. Hardware executes table access

Read: After the control register setup has been completed by software, hardware access then puts this data into the data register. Software then reads this data from the data register.

Write: The data is placed in the data register by software and the control register is set. Hardware writes this data to the table.

## ***8.26. External PHY Register Access***

After the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB powers on and initializes, it will set the PHY MII register via MDC/MDIO. The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports three access control registers to indirectly access an external PHY via the MDC/MDIO interface.

## ***8.27. Switch Interrupt Indication***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provides one global interrupt function: switch interrupt. Interrupt sources are listed below:

- Port Link Change interrupt
- Port SA learning constraint interrupt
- SerDes interrupt

## **9. CPU Function Description**

### **9.1. *MIPS-4KEc***

- MIPS 4KEc CPU Core (Targeted at 500MHz): 5-stage pipeline, MIPS32 instruction set, additional MIPS16e instruction set support, 2 GPR sets (one shadow set), and vectored/Non-Maskable Interrupts (NMI) support
- Cache Configuration: I-Cache is 16KB, 4-way set associative, and 16-byte line size. D-Cache is 16KB, 4-way set associative, 16-byte line size, and write-back policy. It also has virtually indexed, physically tagged, and Prefetch instructions
- MMU Configuration: 4-entry ITLB, 4-entry DTLB, and 32-entry JTLB
- Misc.: Power-down mode, EJTAG support, internal BIST, internal real-time timer interrupts (Count/Compare registers), and CPU breakpoints

### **9.2. *SPI Flash***

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB support 32M-Byte (max) serial I/O, dual I/O SPI Flash.

### **9.3. *SDRAM Interface Configuration (RTL8380M-VB/RTL8382M-VB Only)***

Only the RTL8380M-VB/RTL8382M-VB support 8-bit data bus DDR1/DDR2/DDR3 SDRAM.

## 10. Interface Descriptions

### 10.1. QSGMII

QSGMII-plus (Quad Serial Gigabit Media Independent Interface) reduces PCB complexity and IC pin count. This innovative 5Gbps serial interface provides an up to 10 inch MAC to PHY communication path. QSGMII can carry the full duplex gigabit Ethernet data streams of four ports simultaneously, using only 4 pins.

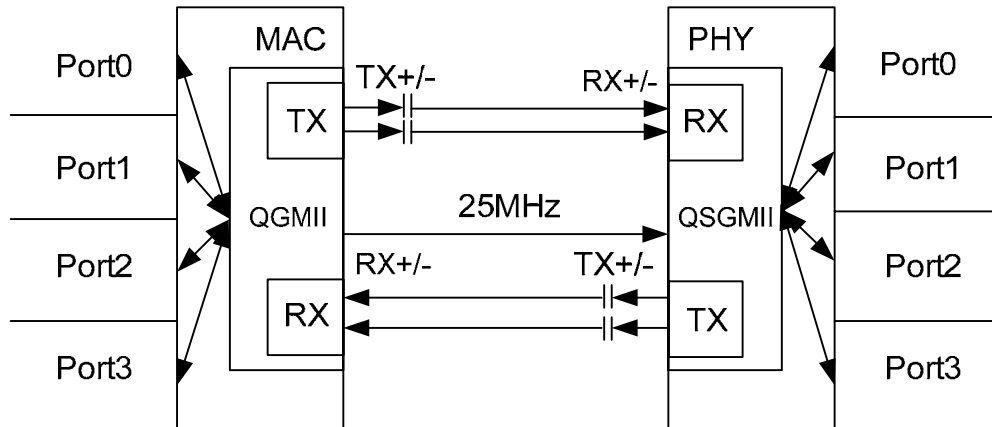


Figure 23. QSGMII Interconnection

### 10.2. SGMII

SGMII (Serial Gigabit Media Independent Interface) conveys PHY and MAC data with significantly less pins than required for GMII. It operates in both half and full duplex, and at all port speeds. It includes 4 data signals and 2 CLK signals to convey frame data and link rate information between the PHY and MAC. The data signals operate at 1.25Gbaud, and the CLK operates at 625MHz. Each of these signals is carried as a differential pair, thus providing signal integrity while minimizing system noise.

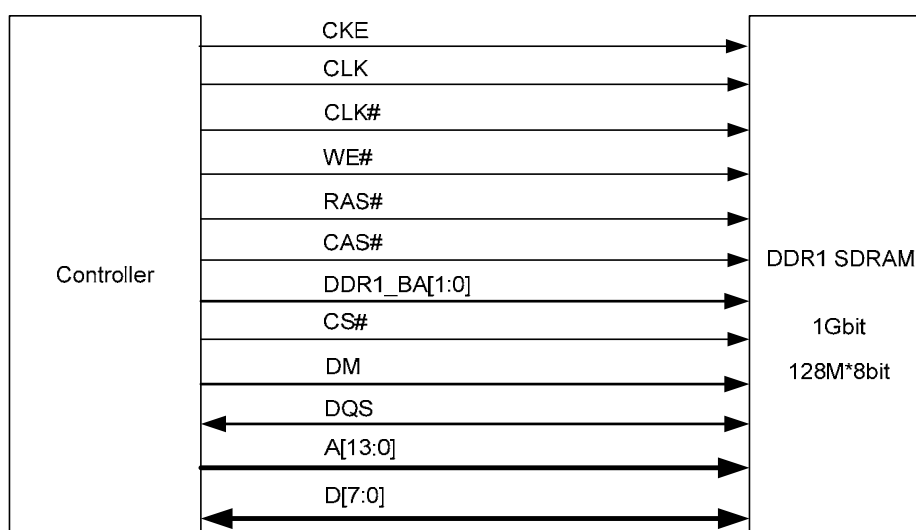


Figure 24. SGMII Signal

### 10.3. *DDR1 SDRAM (RTL8380M-VB/RTL8382M-VB Only)*

The RTL8380M-VB/RTL8382M-VB support DDR1 SDRAM with the following features:

- Bus width is 8 bits
- One chip selection
- Supports 4 banks
- Row count range is 4~16K, and column count range is 512~4K
- Supports maximum 128M Bytes DDR1 SDRAM

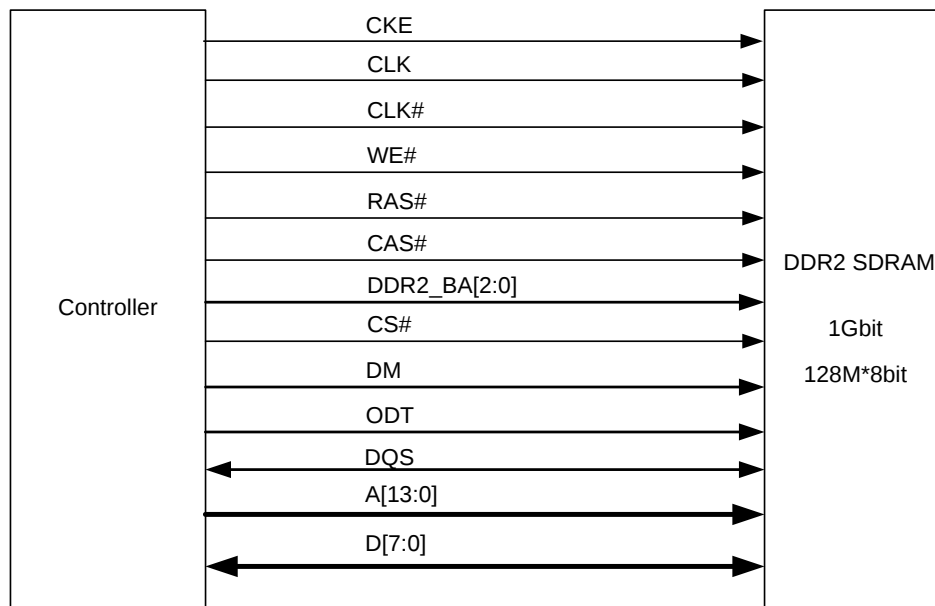


**Figure 25. DDR1 SDRAM Configuration**

### 10.4. *DDR2 SDRAM (RTL8380M-VB/RTL8382M-VB Only)*

The RTL8380M-VB/RTL8382M-VB support DDR2 SDRAM with the following features:

- Bus width is 8 bits
- One chip selection
- Supports 4 banks or 8 banks
- Row count range is 4~16K, and column count range is 512~4K
- Supports maximum 128M Bytes DDR2 SDRAM

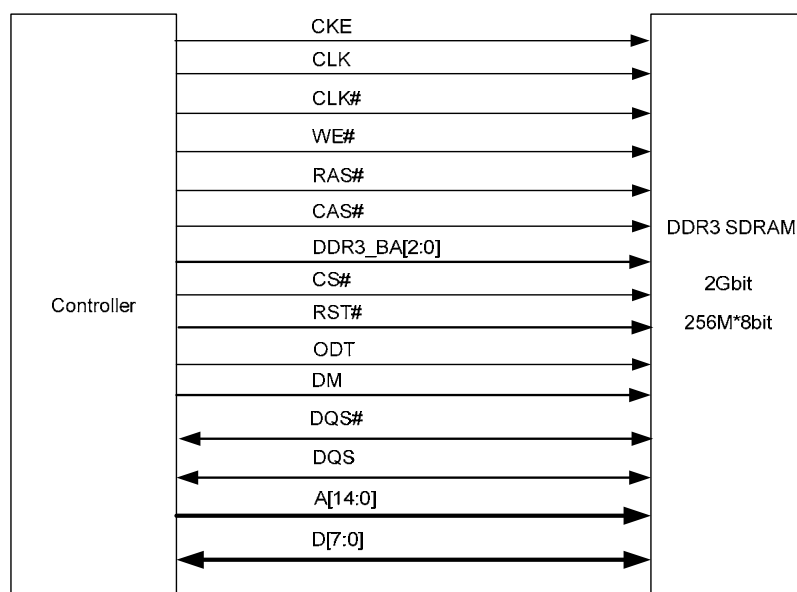


**Figure 26. DDR2 SDRAM Configuration**

## 10.5. *DDR3 SDRAM (RTL8380M-VB/RTL8382M-VB Only)*

The RTL8380M-VB/RTL8382M-VB support DDR3 SDRAM with the following features:

- Bus width is 8 bits
- One chip selection
- Supports 8 banks
- Supports maximum 256M Bytes DDR3 SDRAM

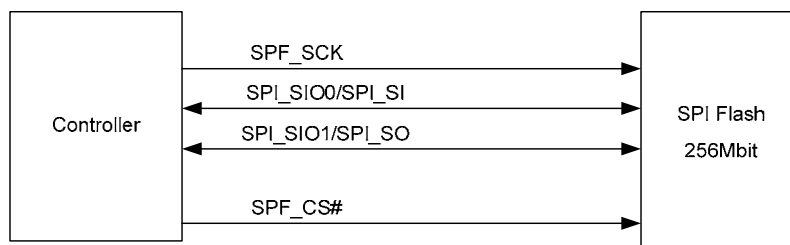


**Figure 27. DDR3 SDRAM Configuration**

## 10.6. *SPI Flash Interface*

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB support SPI Flash with the following features:

- Supports serial I/O, dual I/O SPI Flash (max)
- Supports both MMIO (Memory Mapped I/O) and PIO (Programmed I/O) mode
- One chip selection
- Supports maximum 32M Bytes SPI Flash in PIO mode and 16M Bytes in MMIO mode



**Figure 28. SPI Flash Configuration**

## 10.7. UART

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provides two UARTs, and each contains a 16-byte FIFO buffer. The baud rate can be up to 1Mbps and a programmable baud rate generator allows division of any input reference clock by 1 to 65535, and generates an internal 16x clock. The RTL8380M-VB/RTL8382M-VB provides a fully programmable serial interface.

In addition to the above functions, the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB provides fully prioritized interrupt control and loopback functionality for diagnostic capabilities.

The UART interface pins are shown in the following table.

**Table 45. UART Control Interface Pins**

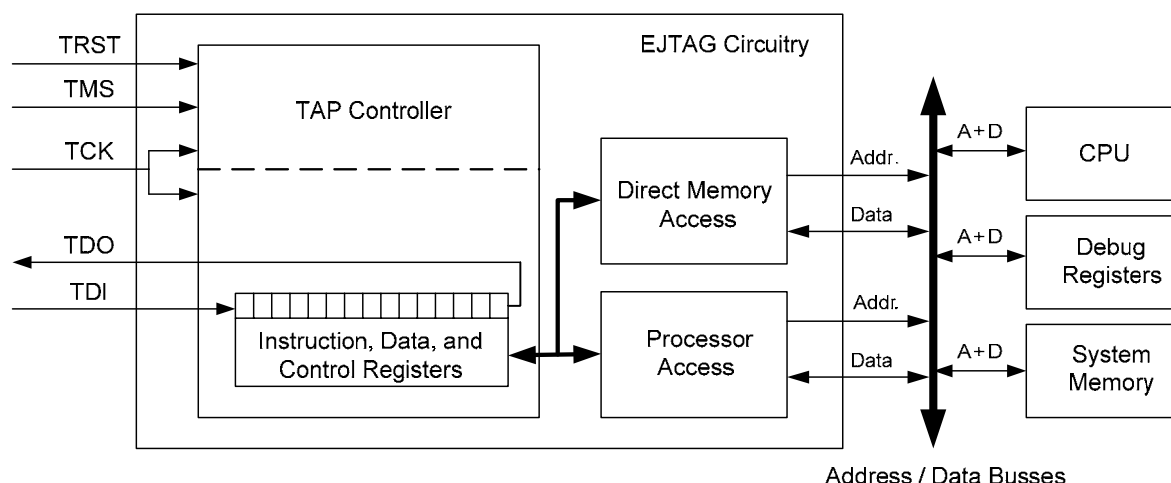
| Signal Name | Type   | Description    |
|-------------|--------|----------------|
| TXD#        | Output | Transmit Data. |
| RXD#        | Input  | Receive Data.  |

## 10.8. EJTAG

EJTAG is inexpensive, and easy to implement. EJTAG utilizes the 5-pin IEEE 1149.1 JTAG (Joint Test Action Group) specification for off-chip communication. The interface pins are shown in Table 46.

**Table 46. EJTAG Interface Pins**

| Signal Name | Type              | Description       |
|-------------|-------------------|-------------------|
| TDI         | Input             | Test Data In.     |
| TDO         | Output            | Test Data Out.    |
| TCK         | Output            | Test Clock.       |
| TMS         | Output            | Test Mode Select. |
| TRST        | Output (Optional) | Test Reset.       |



**Figure 29. EJTAG Using a 5-Pin JTAG Interface to Access Data Block**

EJTAG provides a path to access internal debug registers and circuitry that monitor and control the address and data busses of the processor. The DMA and Processor circuit blocks are used to setup and monitor the processor's internal busses and to execute the code from the EJTAG interface.

When an access is detected, the EJTAG circuitry makes the transaction address available in the EJTAG Address Register, and the appropriate data available in the EJTAG Data Register. It takes about 200 TCK periods to access 32-bit address and data registers in this fashion, so with a 40MHz TCK frequency, the access time is in the range of 5 $\mu$ s.

## 10.9. I2C Master for EEPROM

The EEPROM can be divided into two sizes: 2Kb~8Kb and 32Kb~512Kb. The address of the small size EEPROM is 8-bits, however the larger EEPROM has word-high addressing and word-low addressing, and it is 16-bits (two bytes).

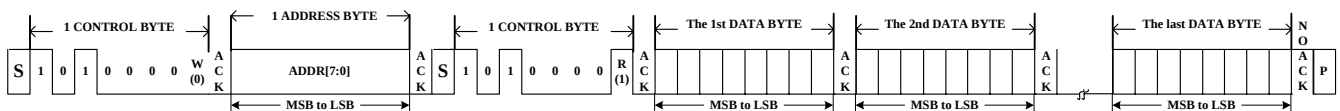


Figure 30. 8-Bit EEPROM Sequential Read

## 10.10. I2C Slave Interface

The RTL8380M-VB/RTL8382M-VB supports an I2C slave interface (Slave mode) for an external CPU to access the internal register. The RTL8382L-VB only supports an I2C slave interface to access some registers for debug purposes.

The interface has two I/O pins (i.e., SDA and SCL). SDA is the access data signal, and SCL is the clock signal (typical clock is 1~2MHz). The read/write data sequence is shown below.

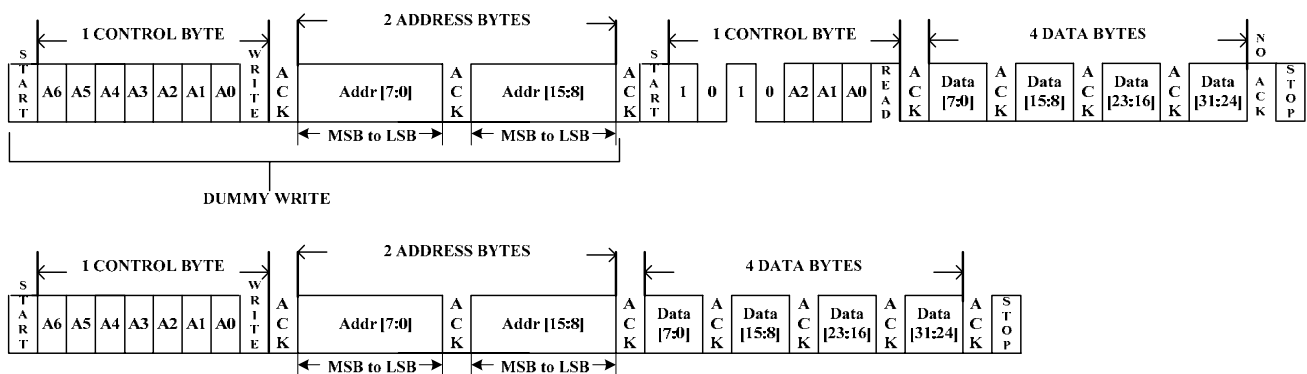


Figure 31. I2C Slave Interface Access Data Sequence

## 10.11. SPI Slave Interface

The RTL8380M-VB/RTL8382M-VB supports SPI slave interface (Slave mode) for an external CPU to access the internal register. The RTL8382L-VB only supports SPI slave interface to access some registers for debug purposes.

The interface has four I/O pins (SI, SO, SCK, and CS#). The instruction sets are as shown in the following table.

**Table 47. SPI Slave Interface**

| Instruction Name | Byte 1<br>(Code) | Byte 2  | Byte 3 | Byte 4 | Byte 5  | Byte 6  | Byte 7 | Byte 8 |
|------------------|------------------|---------|--------|--------|---------|---------|--------|--------|
| Write Data       | 02h              | A23~A16 | A15~A8 | A7~A0  | D31~D24 | D23~D16 | D15~D8 | D7~D0  |
| Read Data        | 03h              | A23~A16 | A15~A8 | A7~A0  | D31~D24 | D23~D16 | D15~D8 | D7~D0  |

*Note:*

*A23~A8: Maps to the switch's 16-bits register address.*

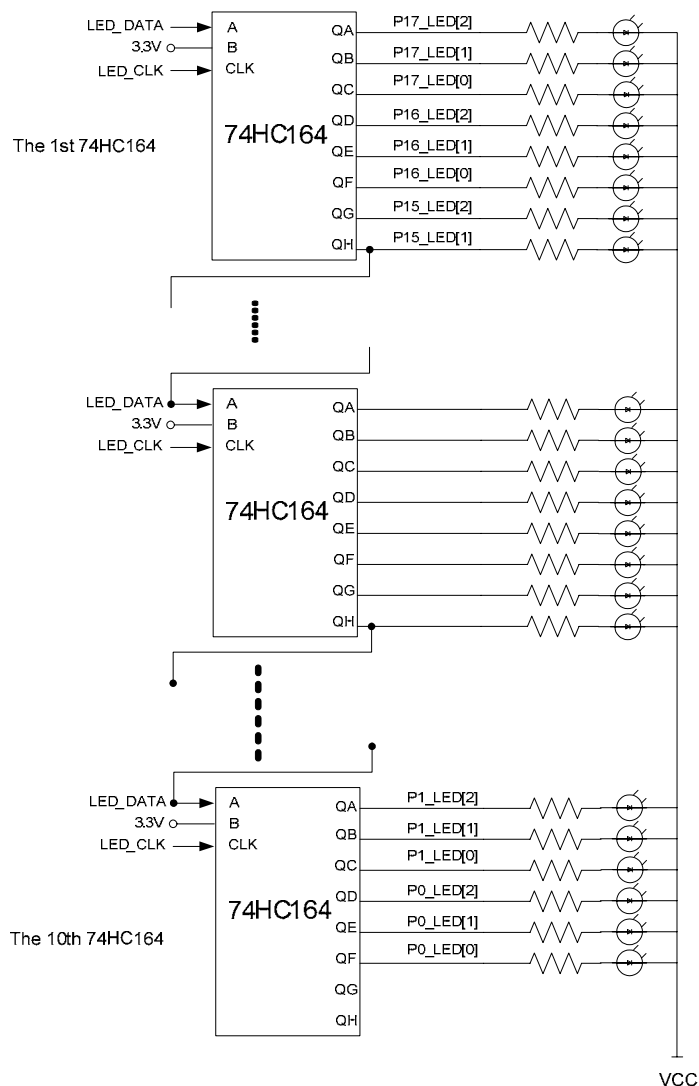
*A7~A0 in Write Data Instruction: Dummy byte for switch and conforms to standard SPI 24-bits address format.*

*A7~A0 in Read Data Instruction: Dummy byte waits for the switch to prepare the register data and conforms to standard SPI 24-bits address format.*

*D31~D0: 32-bits Register Data.*

## 10.12. Serial LED

The RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports a serial LED interface to display the link status. The serial LED interface, LED\_CLK and LED\_DA provide clock and data to enable/disable the external shift registers. A 74HC164 8-Bit Serial-In, Parallel-Out Shift Register captures the per-port link status and diagnostic information. In serial shift LED mode, the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB supports per-port one/two/three single-color LED to show the speed, link status, and other information.



**Figure 32. Serial LED Connection**

The default LED status for the RTL8380M-VB/RTL8382M-VB/RTL8382L-VB is as follows:

| LED Number      | 3-LEDs     |
|-----------------|------------|
| LED0 Definition | 1000M Link |
| LED1 Definition | 100M Link  |
| LED2 Definition | Link/Act   |

## 11. Electrical AC/DC Characteristics

### 11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified referenced to GND unless otherwise specified.

**Table 48. Absolute Maximum Ratings**

| Parameter                                                                  | Min        | Max        | Units |
|----------------------------------------------------------------------------|------------|------------|-------|
| Junction Temperature (Tj)                                                  | -          | +125       | °C    |
| Storage Temperature                                                        | -45        | +125       | °C    |
| DVDDH, AVDDH, SVDDH, AVDDH_PLL Supply Referenced to DGND and AGND          | 2.97       | 3.63       | V     |
| DVDDL, AVDDL, SVDDL, AVDDL_PLL, PLLVDDL Supply Referenced to DGND and AGND | 0.90       | 1.18       | V     |
| MVDDH Supply Referenced to DGND (for DDR1)                                 | 2.375      | 2.625      | V     |
| MVDDH Supply Referenced to DGND (for DDR2)                                 | 1.71       | 1.89       | V     |
| MVDDH Supply Referenced to DGND (for DDR3)                                 | 1.425      | 1.575      | V     |
| VDDIO                                                                      | 1.875(2.5) | 2.625(2.5) | V     |
|                                                                            | 1.350(1.5) | 1.732(1.5) | V     |

### 11.2. Operating Range

**Table 49. Recommended Operating Range**

| Parameter                                             | Min   | Typical | Max   | Units |
|-------------------------------------------------------|-------|---------|-------|-------|
| Ambient Operating Temperature (Ta)                    | 0     | -       | 55    | °C    |
| DVDDH, AVDDH, SVDDH, AVDDH_PLL Supply Voltage Range   | 3.135 | 3.3     | 3.465 | V     |
| DVDDL, AVDDL, AVDDL_PLL, PLLVDDL Supply Voltage Range | 0.95  | 1.1     | 1.15  | V     |
| SVDDL Supply Voltage Range                            | 1.05  | 1.1     | 1.15  | V     |
| MVDDH Supply Voltage Range(for DDR1)                  | 2.375 | 2.5     | 2.625 | V     |
| MVDDH Supply Voltage Range(for DDR2)                  | 1.71  | 1.8     | 1.89  | V     |
| MVDDH Supply Voltage Range(for DDR3)                  | 1.425 | 1.5     | 1.575 | V     |
| VDDIO                                                 | 1.875 | 2.5     | 2.625 | V     |
|                                                       | 1.350 | 1.5     | 1.732 | V     |

### 11.3. DC Characteristics

**Table 50. DC Characteristics (IO Power =3.3V)**

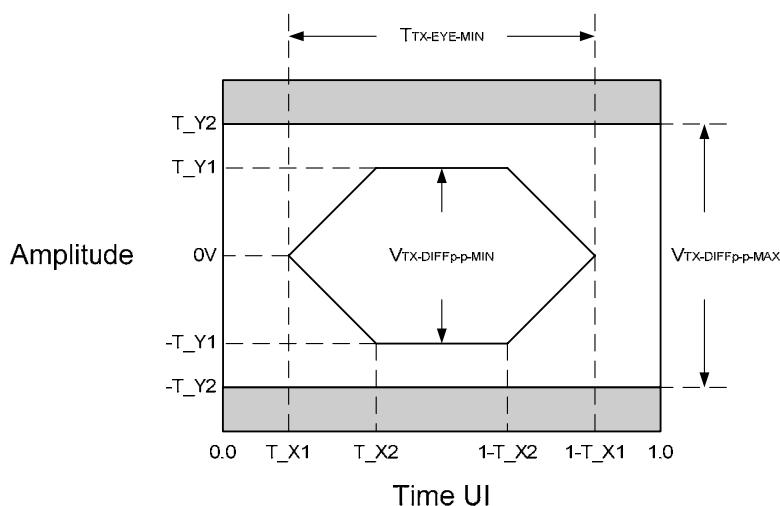
| Symbol   | Parameter              | Min | Typical | Max | Units |
|----------|------------------------|-----|---------|-----|-------|
| $V_{IH}$ | TTL Input High Voltage | 2.0 | -       | -   | V     |
| $V_{IL}$ | TTL Input Low Voltage  | -   | -       | 0.8 | V     |
| $V_{OH}$ | Output High Voltage    | 2.4 | -       | -   | V     |
| $V_{OL}$ | Output Low Voltage     | -   | -       | 0.4 | V     |

### 11.4. AC Characteristics

#### 11.4.1. QSGMII Differential Transmitter Characteristics

**Table 51. QSGMII Differential Transmitter Characteristics**

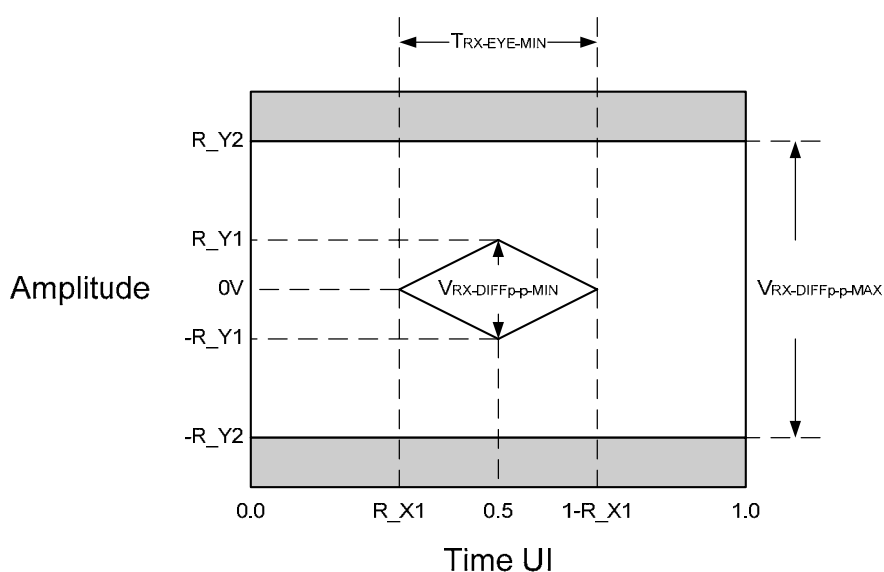
| Symbol           | Parameter                   | Min    | Typical | Max    | Units | Notes        |
|------------------|-----------------------------|--------|---------|--------|-------|--------------|
| UI               | Unit Interval               | 199.94 | 200     | 200.06 | ps    | 200ps±300ppm |
| $T_{X1}$         | Eye Mask                    | -      | -       | 0.2    | UI    | -            |
| $T_{X2}$         | Eye Mask                    | -      | -       | 0.4    | UI    | -            |
| $T_{Y1}$         | Eye Mask                    | 150    | -       | -      | mV    | -            |
| $T_{Y2}$         | Eye Mask                    | -      | -       | 650    | mV    | -            |
| $V_{TX-DIFFp-p}$ | Output Differential Voltage | 600    | 900     | 1300   | mV    | -            |
| $T_{TX-EYE}$     | Minimum TX Eye Width        | 0.6    | -       | -      | UI    | -            |
| $T_{TX-JITTER}$  | Output Jitter               | -      | -       | 0.4    | UI    | -            |
| $T_{TX-RISE}$    | Output Rise Time            | 0.15   | -       | -      | UI    | -            |
| $T_{TX-FALL}$    | Output Fall Time            | 0.15   | -       | -      | UI    | -            |
| $R_{TX}$         | Differential Resistance     | 80     | 100     | 120    | ohm   | -            |
| $C_{TX}$         | AC Coupling capacitor       | 75     | 100     | 200    | nF    | -            |
| $L_{TX}$         | Transmit Length in PCB      | -      | -       | 10     | inch  | -            |


**Figure 33. QSGMII Differential Transmitter Eye Diagram**

## 11.4.2. QSGMII Differential Receiver Characteristics

**Table 52. QSGMII Differential Receiver Characteristics**

| Symbol                  | Parameter                  | Min    | Typical | Max    | Units | Notes        |
|-------------------------|----------------------------|--------|---------|--------|-------|--------------|
| UI                      | Unit Interval              | 199.94 | 200     | 200.06 | ps    | 200ps±300ppm |
| R_X1                    | Eye Mask                   | -      | -       | 0.3    | UI    | -            |
| R_Y1                    | Eye Mask                   | 100    | -       | -      | mV    | -            |
| R_Y2                    | Eye Mask                   | -      | -       | 650    | mV    | -            |
| V <sub>RX-DIFFp-p</sub> | Input Differential Voltage | 200    | -       | 1300   | mV    | -            |
| T <sub>RX-EYE</sub>     | Minimum RX Eye Width       | 0.4    | -       | -      | UI    | -            |
| T <sub>RX-JITTER</sub>  | Input Jitter Tolerance     | -      | -       | 0.6    | UI    | -            |
| R <sub>RX</sub>         | Differential Resistance    | 80     | 100     | 120    | ohm   | -            |

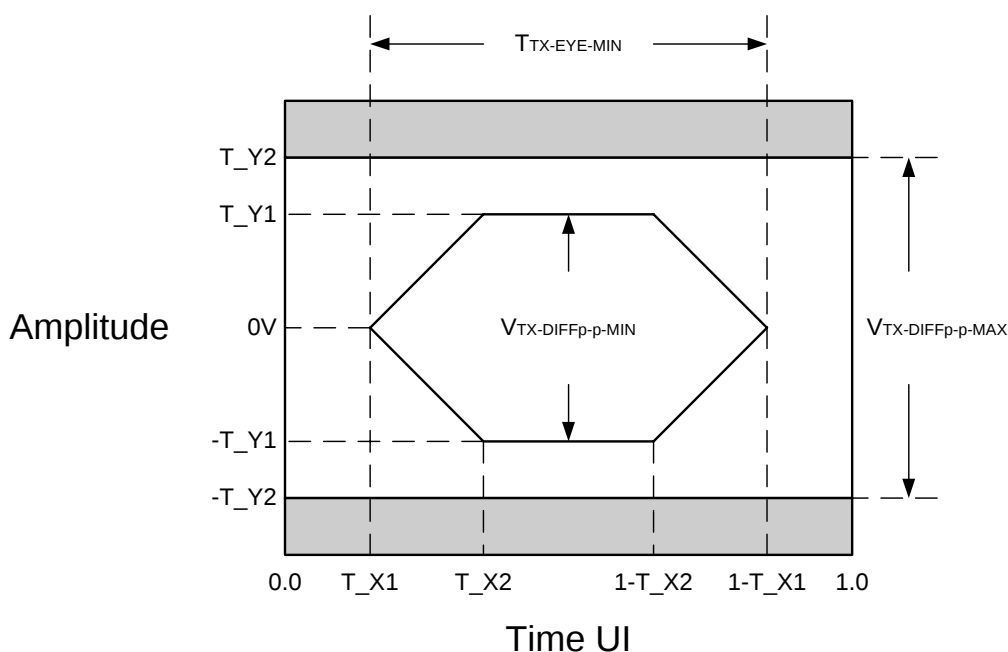


**Figure 34. QSGMII Differential Receiver Eye Diagram**

### 11.4.3. SGMII Differential Transmitter Characteristics

**Table 53. SGMII Differential Transmitter Characteristics**

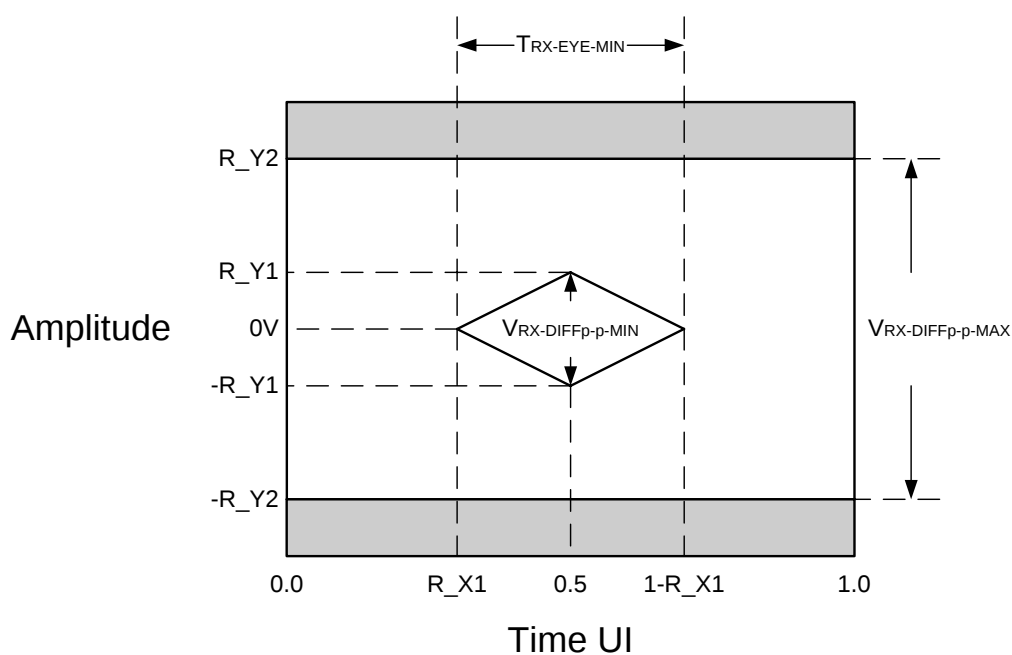
| Symbol                  | Parameter                   | Min    | Typical | Max    | Units | Notes        |
|-------------------------|-----------------------------|--------|---------|--------|-------|--------------|
| UI                      | Unit Interval               | 799.76 | 800     | 800.24 | ps    | 800ps±300ppm |
| T_X1                    | Eye Mask                    | -      | -       | 0.1875 | UI    | -            |
| T_X2                    | Eye Mask                    | -      | -       | 0.4    | UI    | -            |
| T_Y1                    | Eye Mask                    | 125    | -       | -      | mV    | -            |
| T_Y2                    | Eye Mask                    | -      | -       | 500    | mV    | -            |
| V <sub>TX-DIFFp-p</sub> | Output Differential Voltage | 400    | 700     | 900    | mV    |              |
| T <sub>TX-EYE</sub>     | Minimum TX Eye Width        | 0.625  | -       | -      | UI    | -            |
| T <sub>TX-JITTER</sub>  | Output Jitter               | -      | -       | 0.375  | UI    | -            |
| R <sub>TX</sub>         | Differential Resistance     | 80     | 100     | 120    | ohm   | -            |
| C <sub>TX</sub>         | AC Coupling capacitor       | 75     | 100     | 200    | nF    | -            |
| L <sub>TX</sub>         | Transmit Length in PCB      | -      | -       | 10     | inch  | -            |


**Figure 35. SGMII Differential Transmitter Eye Diagram**

### 11.4.4. SGMII Differential Receiver Characteristics

**Table 54. SGMII Differential Receiver Characteristics**

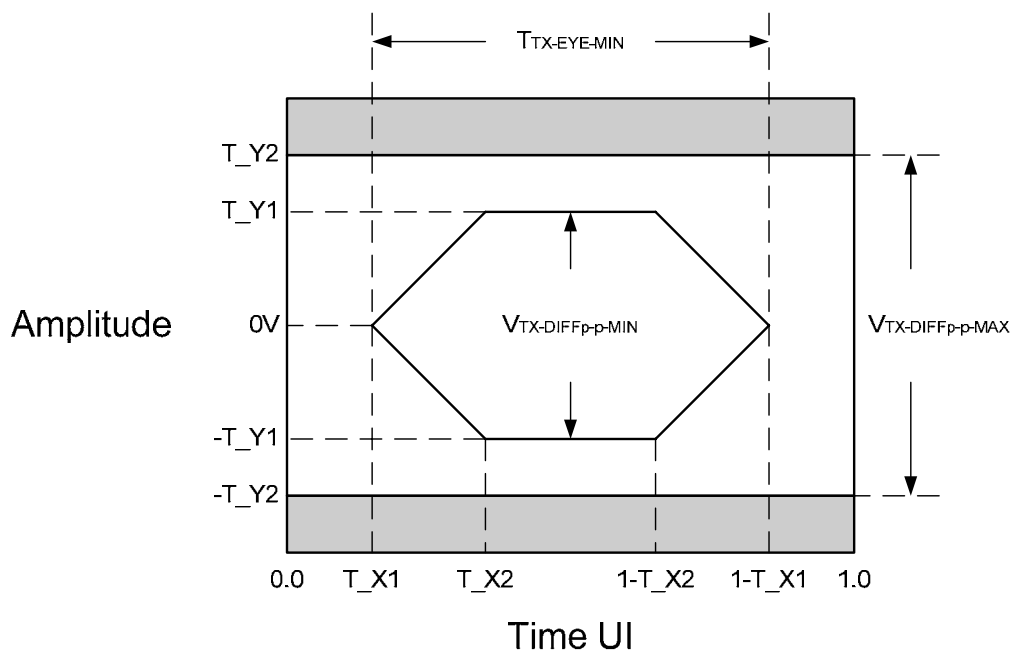
| Symbol                  | Parameter                  | Min    | Typical | Max    | Units | Notes        |
|-------------------------|----------------------------|--------|---------|--------|-------|--------------|
| UI                      | Unit Interval              | 799.76 | 800     | 800.24 | ps    | 800ps±300ppm |
| R_X1                    | Eye Mask                   | -      | -       | 0.3125 | UI    | -            |
| R_Y1                    | Eye Mask                   | 50     | -       | -      | mV    | -            |
| R_Y2                    | Eye Mask                   | -      | -       | 600    | mV    | -            |
| V <sub>RX-DIFFp-p</sub> | Input Differential Voltage | 100    | -       | 1200   | mV    | -            |
| T <sub>RX-EYE</sub>     | Minimum RX Eye Width       | 0.375  | -       | -      | UI    | -            |
| T <sub>RX-JITTER</sub>  | Input Jitter Tolerance     | -      | -       | 0.625  | UI    | -            |
| R <sub>RX</sub>         | Differential Resistance    | 80     | 100     | 120    | ohm   | -            |


**Figure 36. SGMII Differential Receiver Eye Diagram**

### 11.4.5. 1000Base-X/100Base-FX Differential Transmitter Characteristics

**Table 55. 1000Base-X/100Base-FX Differential Transmitter Characteristics**

| Symbol                  | Parameter                   | Min    | Typical | Max    | Units | Notes        |
|-------------------------|-----------------------------|--------|---------|--------|-------|--------------|
| UI                      | Unit Interval (1000Base-X)  | 799.76 | 800     | 800.24 | ps    | 800ps±300ppm |
|                         | Unit Interval (100Base-FX)  | 7.9976 | 8.0     | 8.0024 | ns    | 8ns±300ppm   |
| T_X1                    | Eye Mask                    | -      | -       | 0.1875 | UI    | -            |
| T_X2                    | Eye Mask                    | -      | -       | 0.4    | UI    | -            |
| T_Y1                    | Eye Mask                    | 125    | -       | -      | mV    | -            |
| T_Y2                    | Eye Mask                    | -      | -       | 650    | mV    | -            |
| V <sub>TX-DIFFp-p</sub> | Output Differential Voltage | 400    | 800     | 1300   | mV    | -            |
| T <sub>TX-EYE</sub>     | Minimum TX Eye Width        | 0.625  | -       | -      | UI    | -            |
| T <sub>TX-JITTER</sub>  | Output Jitter               | -      | -       | 0.375  | UI    | -            |
| R <sub>TX</sub>         | Differential Resistance     | 80     | 100     | 120    | ohm   | -            |
| C <sub>TX</sub>         | AC Coupling capacitor       | 75     | 100     | 200    | nF    | -            |
| L <sub>TX</sub>         | Transmit Length in PCB      | -      | -       | 10     | inch  | -            |

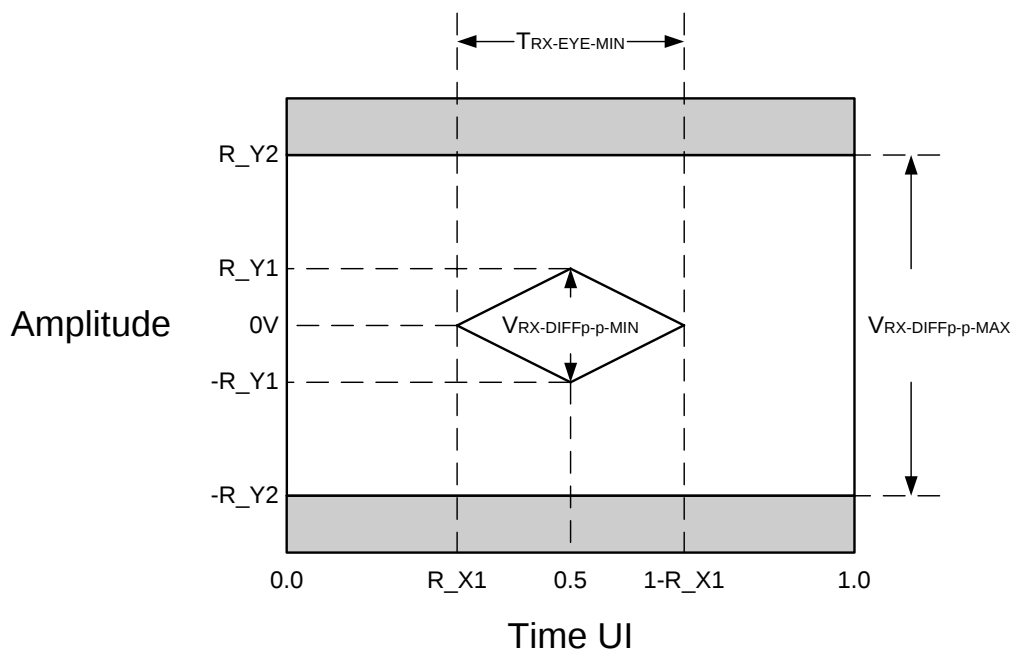


**Figure 37. 1000Base-X/100Base-FX Differential Transmitter Eye Diagram**

### 11.4.6. 1000Base-X/100Base-FX Differential Receiver Characteristics

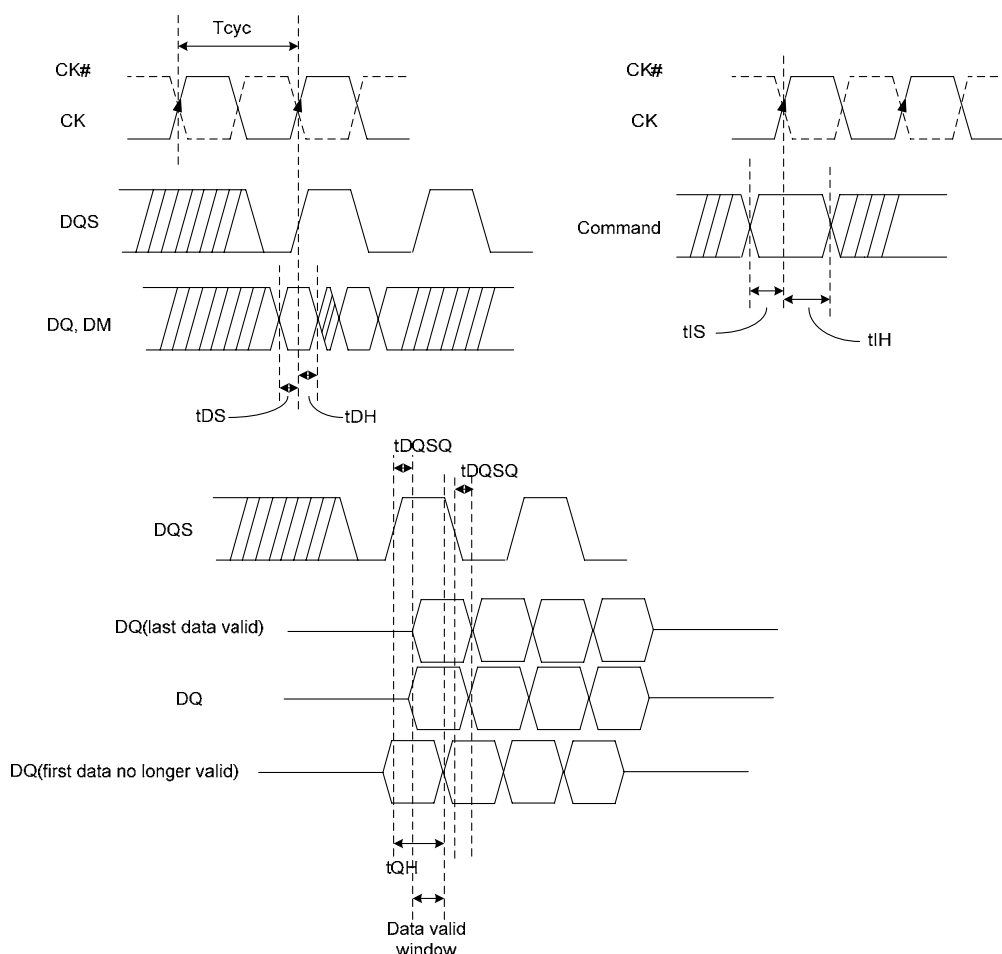
**Table 56. 1000Base-X/100Base-FX Differential Receiver Characteristics**

| Symbol                  | Parameter                  | Min    | Typical | Max    | Units | Notes        |
|-------------------------|----------------------------|--------|---------|--------|-------|--------------|
| UI                      | Unit Interval (1000Base-X) | 799.76 | 800     | 800.24 | ps    | 800ps±300ppm |
|                         | Unit Interval (100Base-FX) | 7.9976 | 8.0     | 8.0024 | ns    | 8ns±300ppm   |
| R_X1                    | Eye Mask                   | -      | -       | 0.3125 | UI    | -            |
| R_Y1                    | Eye Mask                   | 100    | -       | -      | mV    | -            |
| R_Y2                    | Eye Mask                   | -      | -       | 1000   | mV    | -            |
| V <sub>RX-DIFFp-p</sub> | Input Differential Voltage | 200    | -       | 2000   | mV    | -            |
| T <sub>RX-EYE</sub>     | Minimum RX Eye Width       | 0.375  | -       | -      | UI    | -            |
| T <sub>RX-JITTER</sub>  | Input Jitter Tolerance     | -      | -       | 0.625  | UI    | -            |
| R <sub>RX</sub>         | Differential Resistance    | 80     | 100     | 120    | ohm   | -            |



**Figure 38. 1000Base-X/100Base-FX Differential Receiver Eye Diagram**

### 11.4.7. DDR2 Characteristics



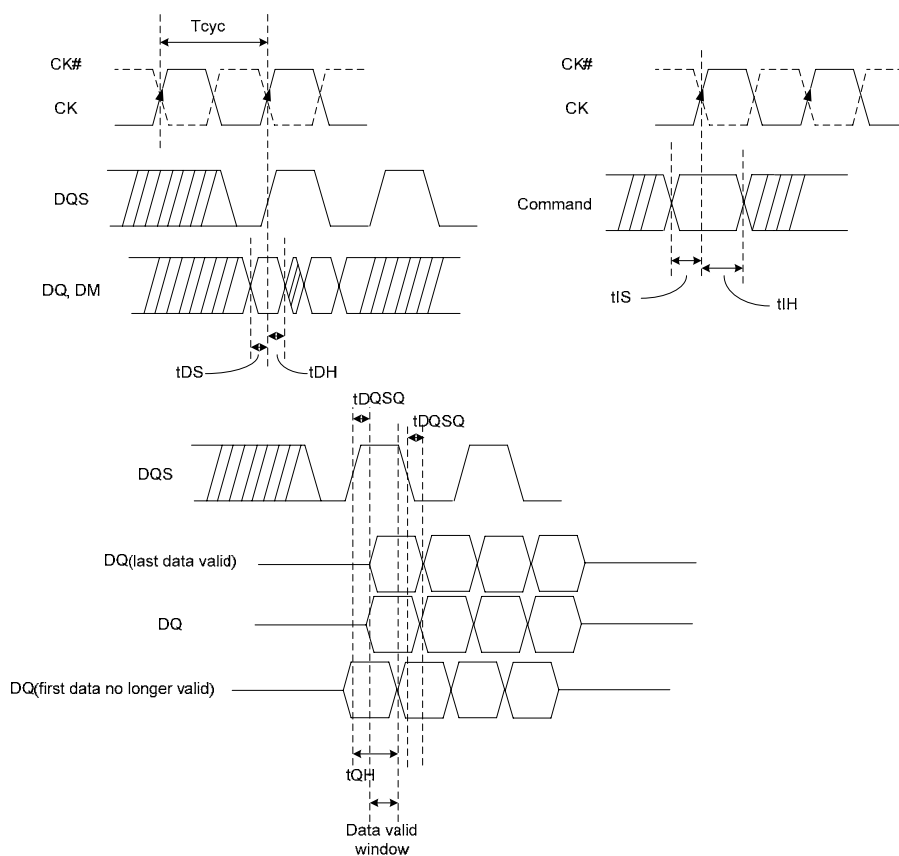
**Figure 39. DDR2 Timing Characteristics**

**Table 57. DDR2 SDRAM Timing Characteristics**

| Symbol             | Description                                        | Min  | Typical | Max | Units |
|--------------------|----------------------------------------------------|------|---------|-----|-------|
| $f_{CK}, f_{CK\#}$ | Clock Frequency of the CK and CK#                  | -    | 300     | -   | MHz   |
| Duty               | Duty Cycle of the CK and CK#                       | 48   | 50      | 52  | %     |
| $t_{JITper}$       | Clock period jitter                                | -110 | -       | 110 | ps    |
| $t_{JITec}$        | Cycle-to-cycle jitter                              | -220 | -       | 220 | ps    |
| $t_{DS}$           | DQ and DM Output Setup Time                        | 450  | -       | -   | ps    |
| $t_{DH}$           | DQ and DM Output Hold Time                         | 450  | -       | -   | ps    |
| $t_{IS}$           | Address and Control Output Setup Time              | 600  | -       | -   | ps    |
| $t_{IH}$           | Address and Control Output Hold Time               | 600  | -       | -   | ps    |
| $t_{DQSQ}$         | Input DQS-DQ Skew, DQS to Last DQ Valid            | -    | -       | 300 | ps    |
| $t_{QH}$           | Input DQ-DQS Hold, DQS to First DQ to Go Non-Valid | 0.3  | -       | -   | CK    |

Note: Test Condition,  $f_{DDR\_CK}=300MHz$ .

## 11.4.8. DDR3 Characteristics



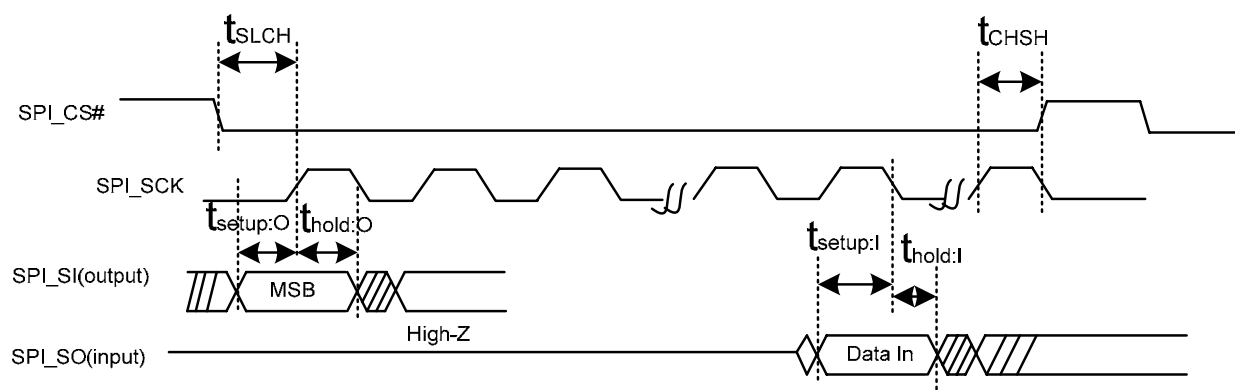
**Figure 40. DDR3 Timing Characteristics**

**Table 58. DDR3 SDRAM Timing Characteristics**

| Symbol             | Description                                        | Min  | Typical | Max | Units |
|--------------------|----------------------------------------------------|------|---------|-----|-------|
| $f_{CK}, f_{CK\#}$ | Clock Frequency of the CK and CK#                  | -    | 300     | -   | MHz   |
| Duty               | Duty Cycle of the CK and CK#                       | 47   | 50      | 53  | %     |
| $t_{JITper}$       | Clock period jitter                                | -90  | -       | 90  | ps    |
| $t_{JITcc}$        | Cycle-to-cycle jitter                              | -165 | -       | 165 | ps    |
| $t_{DS}$           | DQ and DM Output Setup Time                        | 450  | -       | -   | ps    |
| $t_{DH}$           | DQ and DM Output Hold Time                         | 400  | -       | -   | ps    |
| $t_{IS}$           | Address and Control Output Setup Time              | 750  | -       | -   | ps    |
| $t_{IH}$           | Address and Control Output Hold Time               | 550  | -       | -   | ps    |
| $t_{DQSQ}$         | Input DQS-DQ Skew, DQS to Last DQ Valid            | -    | -       | 300 | ps    |
| $t_{QH}$           | Input DQ-DQS Hold, DQS to First DQ to Go Non-Valid | 0.3  | -       | -   | CK    |

Note: Test Condition,  $f_{DDR\_CK}=300MHz$ .

### 11.4.9. SPI Interface Characteristics



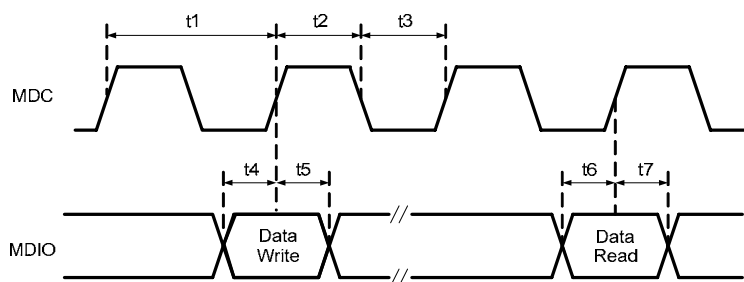
**Figure 41. SPI Interface Timing**

**Table 59. SPI Interface Timing Characteristics**

| Symbol         | Description                    | Min  | Typical | Max  | Units |
|----------------|--------------------------------|------|---------|------|-------|
| $f_{SPI\_SCK}$ | Clock Frequency of the SPI_SCK | 49.5 | 50      | 50.5 | MHz   |
| Duty           | Duty Cycle of the SPI_SCK      | 45   | 50      | 55   | %     |
| $t_{SLCH}$     | CS# Active Setup Time          | 7    | 8.1     | -    | ns    |
| $t_{CHSH}$     | CS# Active Hold Time           | 8    | 9.65    | -    | ns    |
| $t_{setup:O}$  | Data Output Setup Time         | 4    | 8.3     | -    | ns    |
| $t_{hold:O}$   | Data Output Hold Time          | 6    | 9.65    | -    | ns    |
| $t_{setup:I}$  | Data Input Setup Time          | 4    | -       | -    | ns    |
| $t_{hold:I}$   | Data Input Hold Time           | 0    | -       | -    | ns    |

Note: Test Condition,  $f_{SPI\_SCK}=50MHz$ .

### 11.4.10. SMI (MDC/MDIO) Interface Characteristics

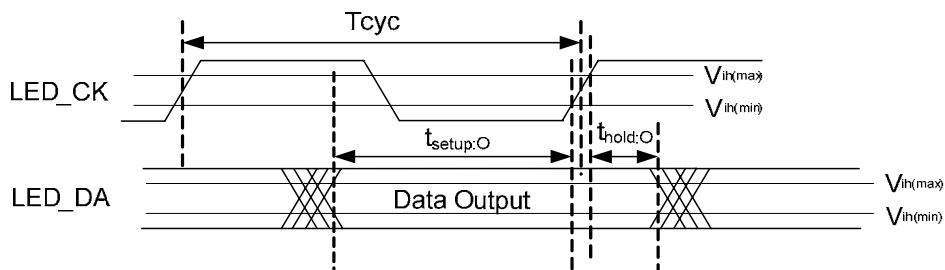


**Figure 42. SMI (MDC/MDIO) Timing**

**Table 60. SMI (MDC/MDIO) Timing Characteristics**

| Symbol | Description                                | Min | Typ | Max | Units |
|--------|--------------------------------------------|-----|-----|-----|-------|
| t1     | MDC Clock Period                           | 380 | -   | -   | ns    |
| t2     | MDC High Time                              | -   | 190 | -   | ns    |
| t3     | MDC Low Time                               | -   | 190 | -   | ns    |
| t4     | MDIO to MDC Rising Setup Time (Write Data) | -   | 190 | -   | ns    |
| t5     | MDIO to MDC Rising Hold Time (Write Data)  | -   | 190 | -   | ns    |
| t6     | MDIO to MDC Rising Setup Time (Read Data)  | 40  | -   | -   | ns    |
| t7     | MDIO to MDC rising hold time (Read Data)   | 2   | -   | -   | ns    |

### 11.4.11. Serial Mode LED



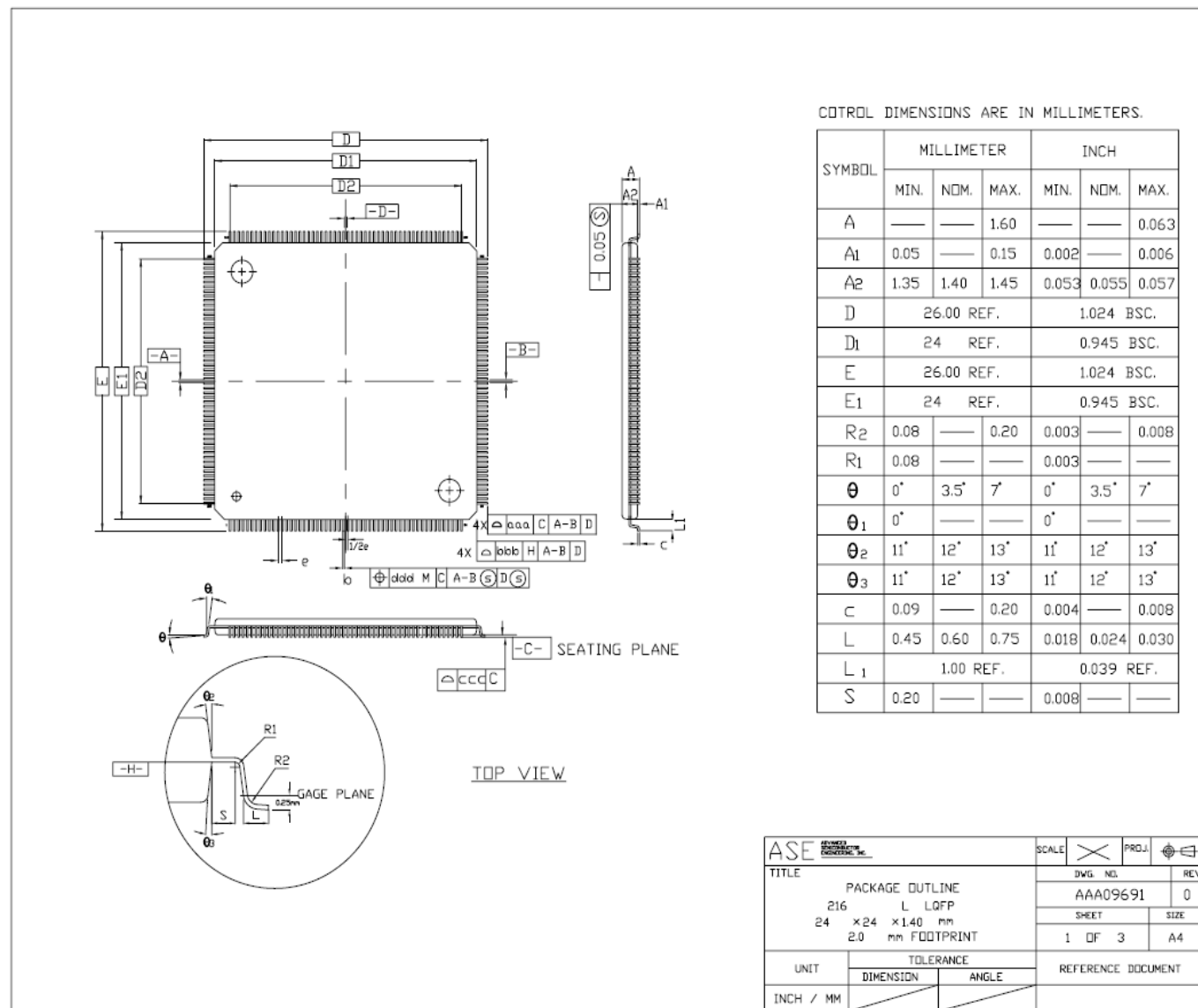
**Figure 43. Serial Mode LED AC Timing Parameters**

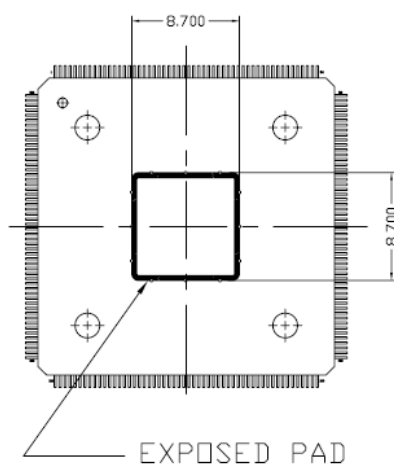
**Table 61. Serial Mode LED AC Timing**

| Mode and Description |                                    | Symbol               | Min | Typical | Max | Units |
|----------------------|------------------------------------|----------------------|-----|---------|-----|-------|
| Serial LED           | Input High Voltage                 | Vih                  | 2.0 | -       | -   | V     |
|                      | Input Low Voltage                  | Vil                  | -   | -       | 0.8 | V     |
|                      | LED_CK Clock Cycle                 | Tcyc                 | -   | 600     | -   | ns    |
|                      | Duty Cycle of the LED_CK           | Duty                 | 45  | 50      | 55  | %     |
|                      | LED_DA to LED_CK Output Setup Time | t <sub>setup:O</sub> | -   | 314     | -   | ns    |
|                      | LED_DA to LED_CK Output Hold Time  | t <sub>hold:O</sub>  | -   | 285     | -   | ns    |

## 12. Package Information

### 12.1. LQFP216-E-PAD (24\*24mm)





BOTTOM VIEW

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. DIMENSION  $b$  DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM  $b$  DIMENSION BY MORE THAN 0.08mm.  
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. THE MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
3. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

| SYMBOL                          | 216L       |      |      |            |       |       |
|---------------------------------|------------|------|------|------------|-------|-------|
|                                 | MILLIMETER |      |      | INCH       |       |       |
|                                 | MIN.       | NOM. | MAX. | MIN.       | NOM.  | MAX.  |
| b                               | 0.13       | 0.16 | 0.23 | 0.005      | 0.006 | 0.009 |
| e                               | 0.40 BSC.  |      |      | 0.016 BSC. |       |       |
| D2                              | 21.20      |      |      | 0.835      |       |       |
| E2                              | 21.20      |      |      | 0.835      |       |       |
| TOLERANCES OF FORM AND POSITION |            |      |      |            |       |       |
| aaa                             | 0.20       |      |      | 0.008      |       |       |
| bbb                             | 0.20       |      |      | 0.008      |       |       |
| ccc                             | 0.08       |      |      | 0.003      |       |       |
| ddd                             | 0.07       |      |      | 0.003      |       |       |

|                             |           |                    |                                                                                       |       |                                                                                       |  |  |
|-----------------------------|-----------|--------------------|---------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------------------------|--|--|
| ASE <small>ASSEMBLY</small> |           | SCALE              |  | PROJ. |  |  |  |
| TITLE                       |           | DWG. NO.           |                                                                                       | REV.  |                                                                                       |  |  |
| PACKAGE OUTLINE             |           | AAA09691           |                                                                                       | 0     |                                                                                       |  |  |
| 216 L LQFP                  |           | SHEET              |                                                                                       | SIZE  |                                                                                       |  |  |
| 24 x 24 x 1.40 mm           |           | 2 OF 3             |                                                                                       | A4    |                                                                                       |  |  |
| 2.0 mm FOOTPRINT            |           | REFERENCE DOCUMENT |                                                                                       |       |                                                                                       |  |  |
| UNIT                        | TOLERANCE |                    |                                                                                       |       |                                                                                       |  |  |
|                             | DIMENSION | ANGLE              |                                                                                       |       |                                                                                       |  |  |
| INCH / MM                   |           |                    |                                                                                       |       |                                                                                       |  |  |

## 13. Ordering Information

**Table 62. Ordering Information**

| Part Number    | Package                                                   | Status |
|----------------|-----------------------------------------------------------|--------|
| RTL8380M-VB-CG | LQFP 216-Pin E-PAD (24*24mm) 'Green' Package (Managed)    | MP     |
| RTL8382M-VB-CG | LQFP 216-Pin E-PAD (24*24mm) 'Green' Package (Managed)    | MP     |
| RTL8382L-VB-CG | LQFP 216-Pin E-PAD (24*24mm) 'Green' Package (Un-Managed) | MP     |

*Note: See page 11 (RTL8380M-VB), page 25 (RTL8382M-VB), and page 39 (RTL8382L-VB) for package identification.*

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