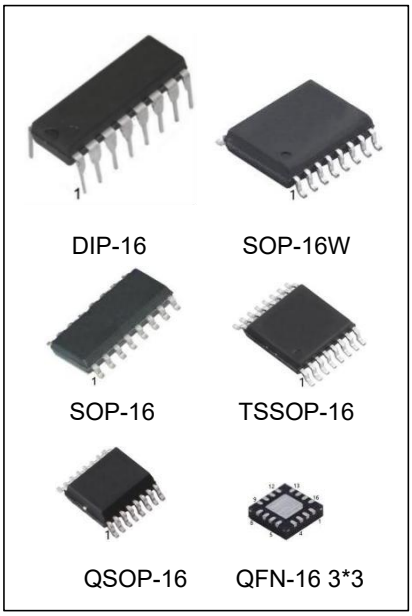
Remote 8-bit I/O expander for I²C-bus

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- Available in 16-Pin DIP, 16-Pin SOP, 16-Pin QSOP, 16-Pin TSSOP and QFN-16 packages .



ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
PCF8574AP	DIP-16	PCF8574A	TUBE	1000pcs/Box
PCF8574AT/TR	SOP-16W	PCF8574A	REEL	2000pcs/Reel
PCF8574AM/TR	SOP-16	PCF8574A	REEL	2500pcs/Reel
PCF8574AMT/TR	TSSOP-16	PCF8574A	REEL	2500pcs/Reel
PCF8574AMS/TR	QSOP-16	PCF8574A	REEL	2500pcs/Reel
PCF8574ALQ/TR	QFN-16 3*3	8574A	REEL	5000pcs/Reel
PCF8574P	DIP-16	PCF8574	TUBE	1000pcs/Box
PCF8574T/TR	SOP-16W	PCF8574	REEL	2000pcs/Reel
PCF8574M/TR	SOP-16	PCF8574	REEL	2500pcs/Reel
PCF8574MT/TR	TSSOP-16	PCF8574	REEL	2500pcs/Reel
PCF8574MS/TR	QSOP-16	PCF8574	REEL	2500pcs/Reel
PCF8574LQ/TR	QFN-16 3*3	8574	REEL	5000pcs/Reel

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I^2C).

The device consists of an 8-bit quasi-bidirectional port and an I^2C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

BLOCK DIAGRAM

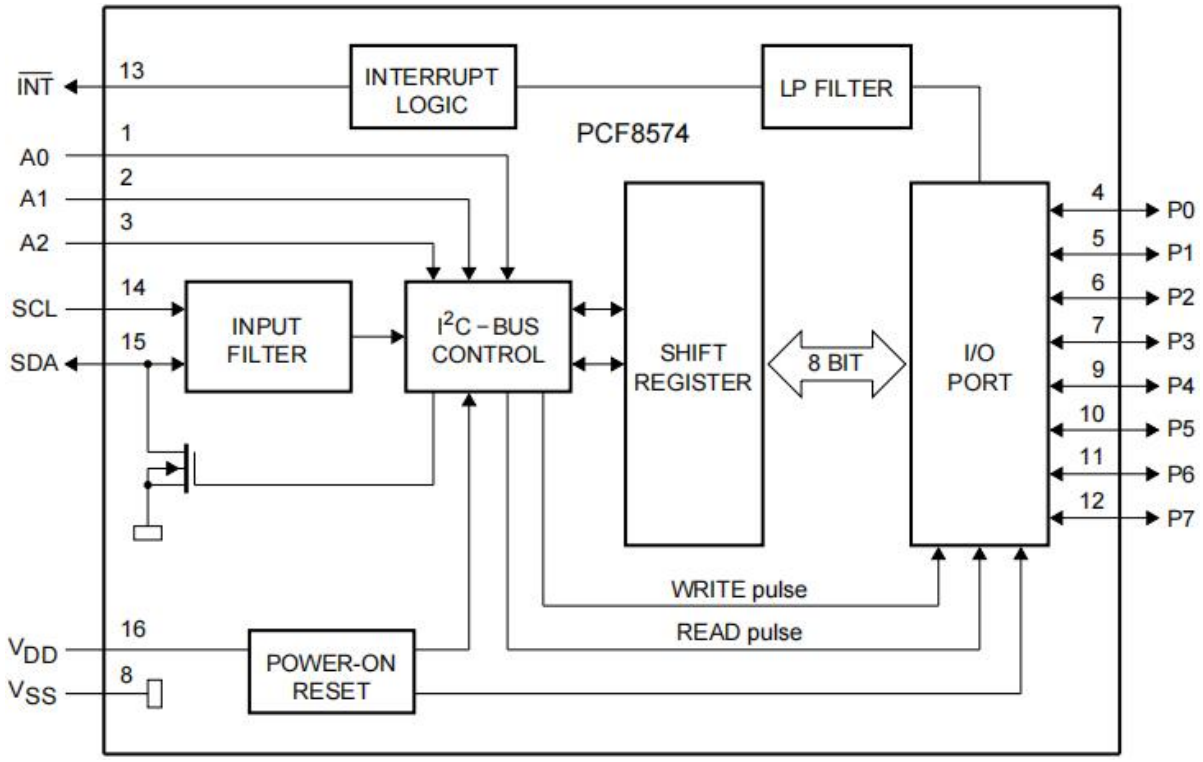
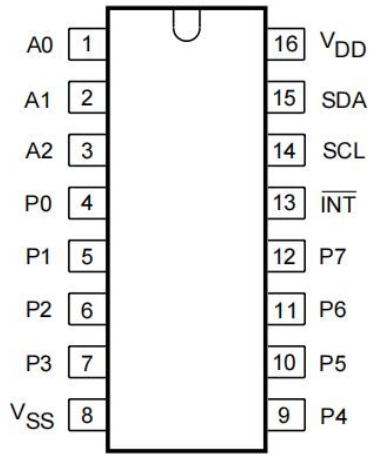


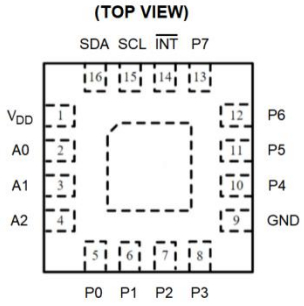
Fig.1 Block diagram

Connection Diagrams



DIP-16/SOP-16/SOP-16W/
QSOP-16/TSSOP-16

Fig.2 Pin configuration .



QFN-16 3*3

Fig.3 Pin configuration .

PIN DESCRIPTION

SYMBOL	Pin.		DESCRIPTION
	DIP-16/SOP-16/SOP-16W/ QSOP-16/TSSOP-16	QFN-16	
A0	1	2	address input 0
A1	2	3	address input 1
A2	3	4	address input 2
P0	4	5	quasi-bidirectional I/O 0
P1	5	6	quasi-bidirectional I/O 1
P2	6	7	quasi-bidirectional I/O 2
P3	7	8	quasi-bidirectional I/O 3
V_{SS}	8	9	supply ground
P4	9	10	quasi-bidirectional I/O 4
P5	10	11	quasi-bidirectional I/O 5
P6	11	12	quasi-bidirectional I/O 6
P7	12	13	quasi-bidirectional I/O 7
$\overline{INT}$	13	14	interrupt output (active LOW)
SCL	14	15	serial clock line
SDA	15	16	serial data line
V_{DD}	16	1	supply voltage

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.4).

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.5).

System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Fig.6).

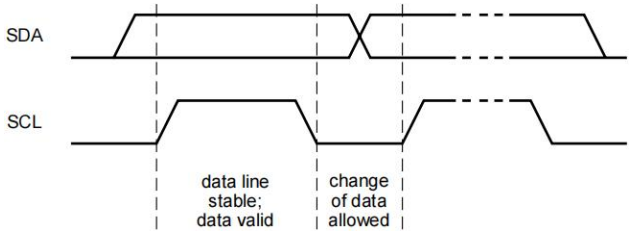


Fig.4 Bit transfer.

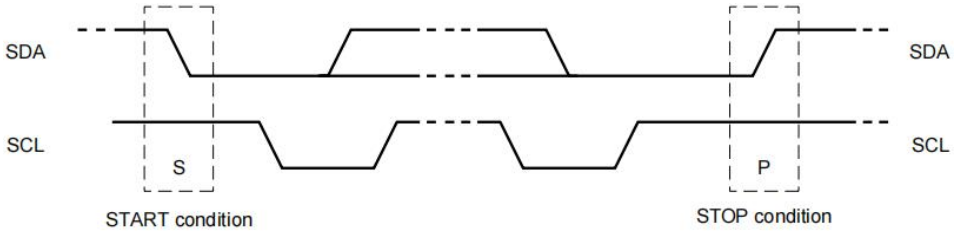


Fig.5 Definition of start and stop conditions.

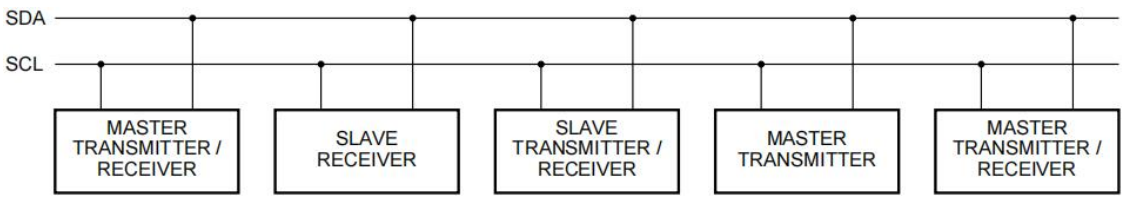


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

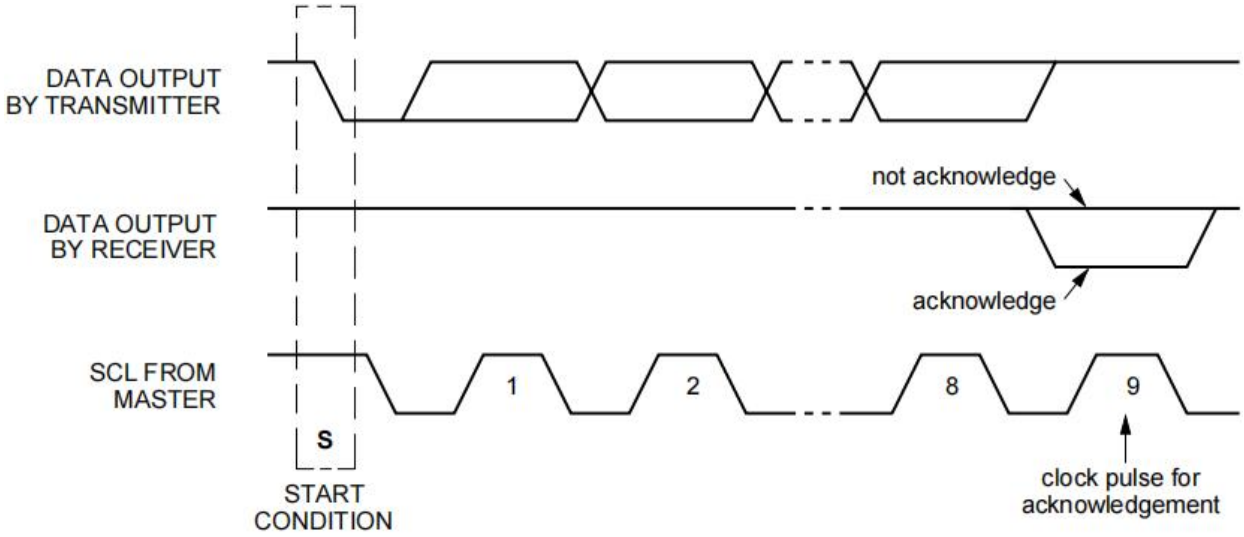


Fig.7 Acknowledgment on the I^2C-bus.

FUNCTIONAL DESCRIPTION

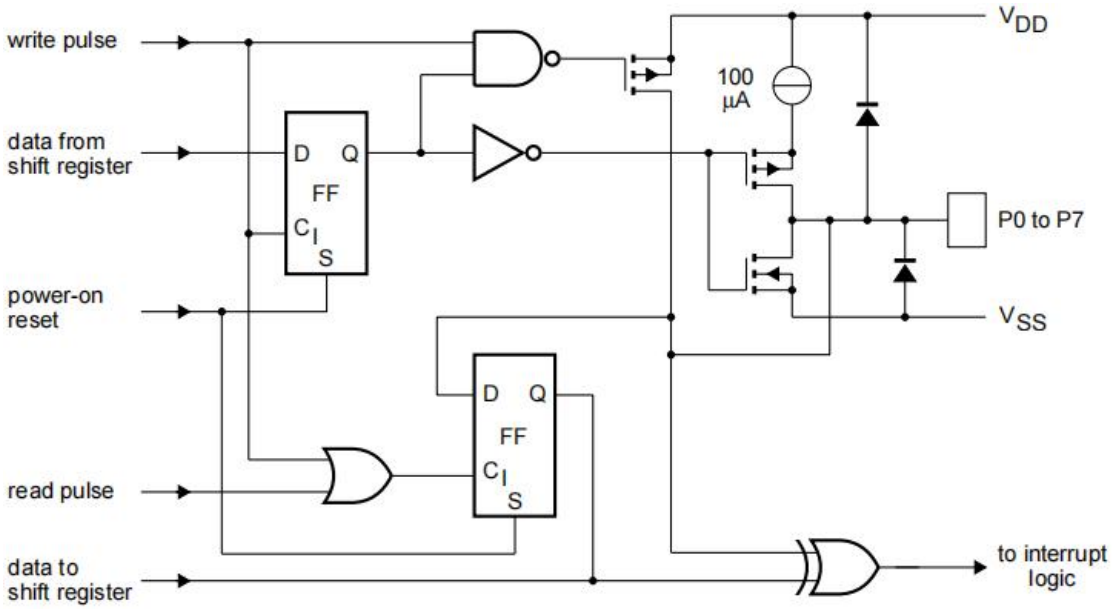
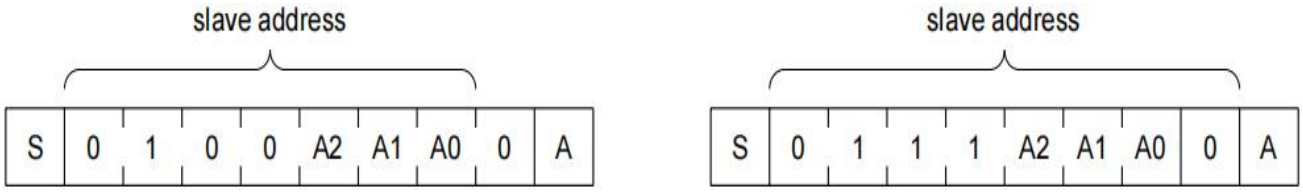


Fig.8 Simplified schematic diagram of each I/O.

Addressing

For addressing see Figs 9, 10 and 11.



a. **(a) PCF8574.**

b. **(b) PCF8574A.**

Fig.9 PCF8574 and PCF8574A slave addresses.

Each of the PCF8574's eight I/Os can be independently used as an input or output. Input data is transferred from the port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the port by the WRITE mode (see Fig.10).

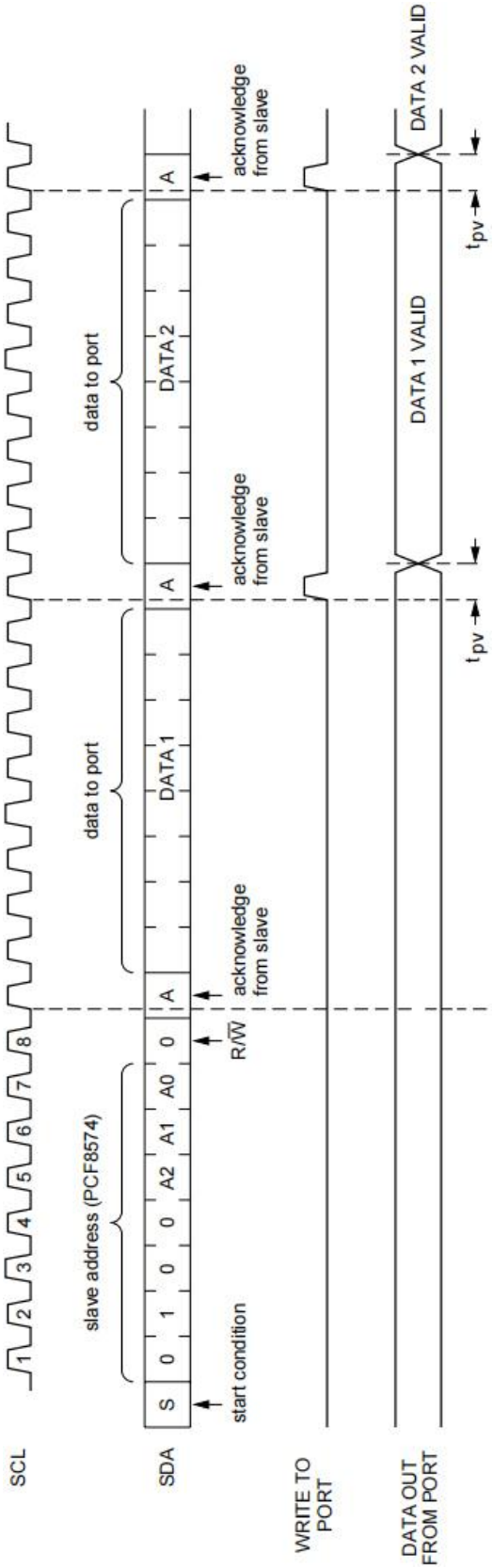


Fig.10 WRITE mode (output).

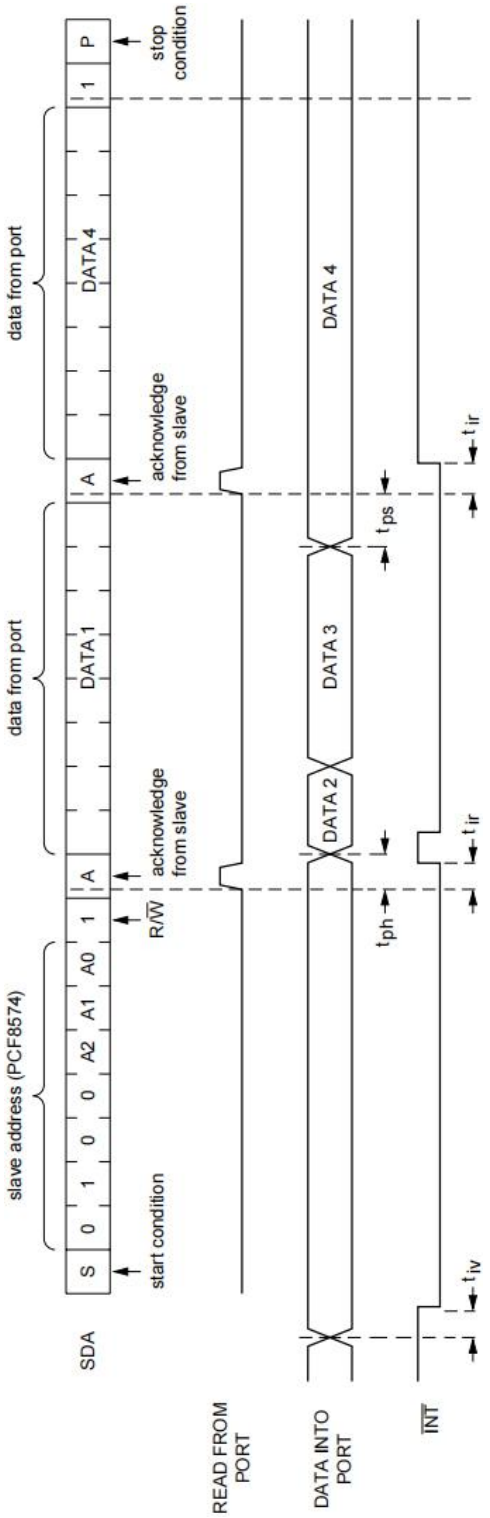


Fig.11 READ mode (input).

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time tiv the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the I/Os after resetting will be detected and, after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

Quasi-bidirectional I/Os (see Fig.14)

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

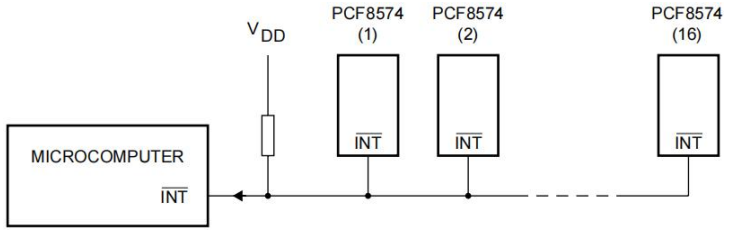


Fig.12 Application of multiple PCF8574s with interrupt.

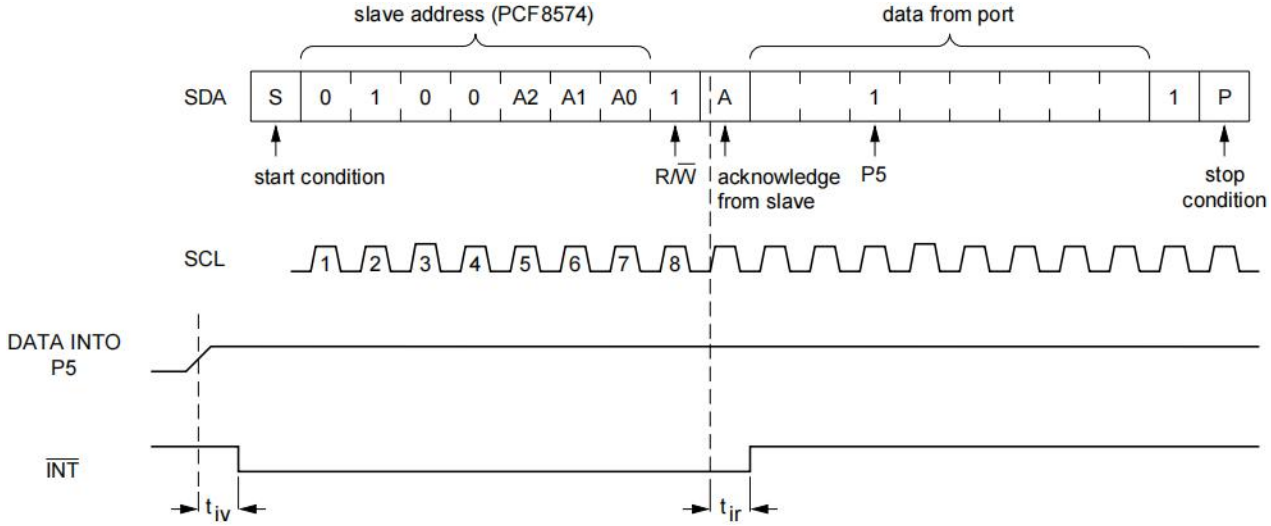


Fig.13 Interrupt generated by a change of input to I/O P5.

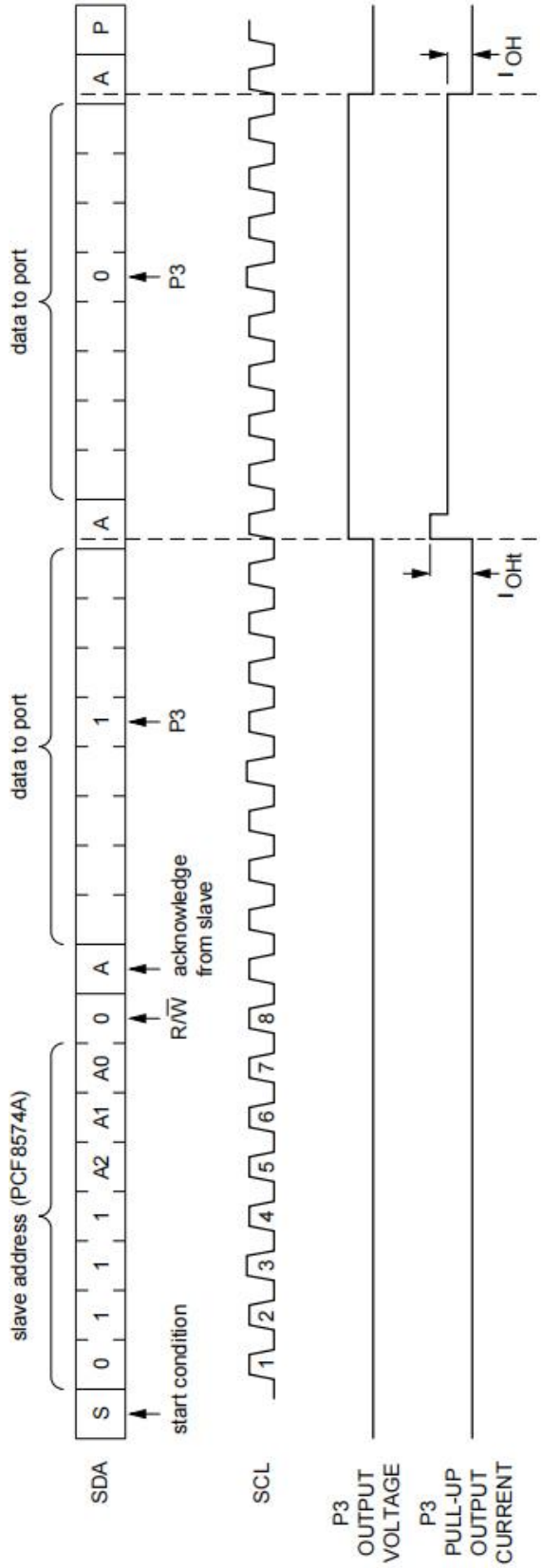


Fig.14 Transient pull-up current I while P3 changes from LOW-to-HIGH and back to LOW.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	-0.5	+7.0	V
V_I	input voltage	V_{SS} - 0.5	V_{DD} + 0.5	V
I_I	DC input current	-	20	mA
I_O	DC output current	-	25	mA
I_{DD}	supply current	-	100	mA
I_{SS}	supply current	-	100	mA
P_{tot}	total power dissipation	-	400	mW
P_O	power dissipation per output	-	100	mW
T_{stg}	storage temperature	-65	+150	℃
T_{amb}	operating ambient temperature	-40	+85	℃
T_L	Lead Temperature (Soldering, 10 seconds)	-	260	℃

Note:Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; Tamb = -40 to +85℃; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5		6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	-	40	100	μA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}	-	2.5	10	μA
V_{POR}	Power-on reset voltage	V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; note 1	-	1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage	-	-0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage	-	0.7V_{DD}	-	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}	-1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}	-	-	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
		I/Os				
V_{IL}	LOW level input voltage	-	-0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	-	$0.7V_{DD}$	-	V_{DD} + 0.5	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	-	-	400	μA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25		mA
I_{OH}	HIGH level output current	$V_{OH} = V_{SS}$	30	-	300	μA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.14); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	-	-1	-	mA
C_i	input capacitance	-	-	-	10	pF
C_o	output capacitance	-	-	-	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 10 and 11)						
t_{pv}	output data valid	-	-	-	4	μs
t_{su}	input data set-up time	-	0	-	-	μs
t_h	input data hold time	-	4	-	-	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
TIMING; $C_L \leq$ 100 pF						
t_{iv}	input data valid time	-	-	-	4	μs
t_{ir}	reset delay time	-	-	-	4	μs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage	-	-0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	-	$0.7V_{DD}$	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	-250	-	+250	nA

Note

1. The Power-on reset circuit resets the I2C-bus logic with $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-BUS TIMING (see Fig.15; note 1)					
f_{SCL}	SCL clock frequency	-	-	100	kHz
t_{SW}	tolerable spike width on bus	-	-	100	ns
t_{BUF}	bus free time	4.7	-	-	µs
$t_{SU;STA}$	START condition set-up time	4.7	-	-	µs
$t_{HD;STA}$	START condition hold time	4.0	-	-	µs
t_{LOW}	SCL LOW time	4.7	-	-	µs
t_{HIGH}	SCL HIGH time	4.0	-	-	µs
t_r	SCL and SDA rise time	-	-	1.0	µs
t_f	SCL and SDA fall time	-	-	0.3	µs
$t_{SU;DAT}$	data set-up time	250	-	-	ns
$t_{HD;DAT}$	data hold time	0	-	-	ns
$t_{VD;DAT}$	SCL LOW to data out valid	-	-	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	-	-	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

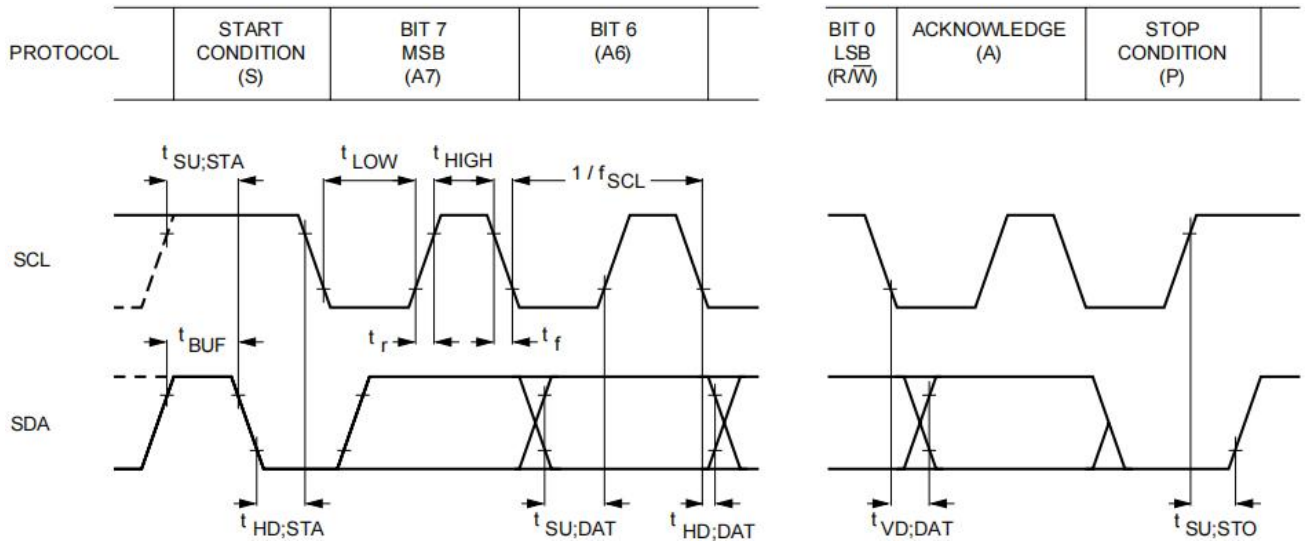
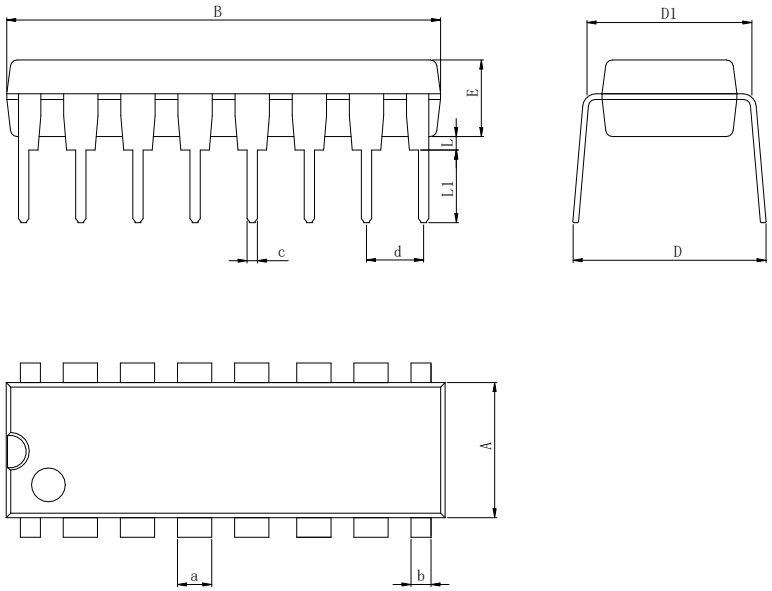


Fig.15 I²C-bus timing diagram.

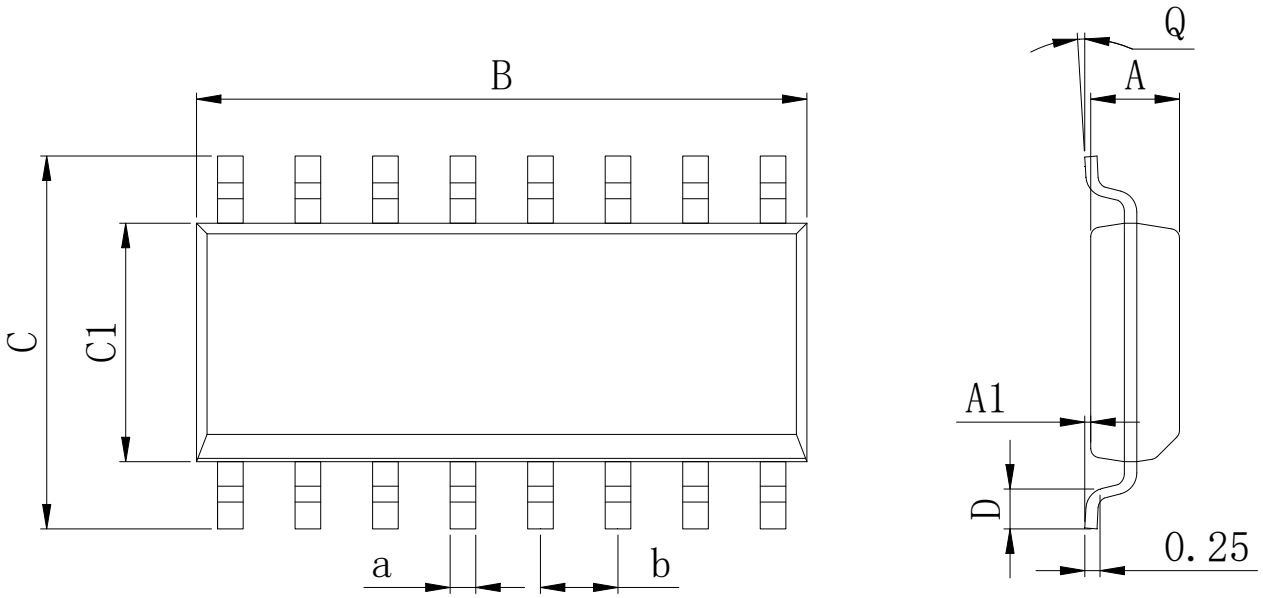
PHYSICAL DIMENSIONS

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

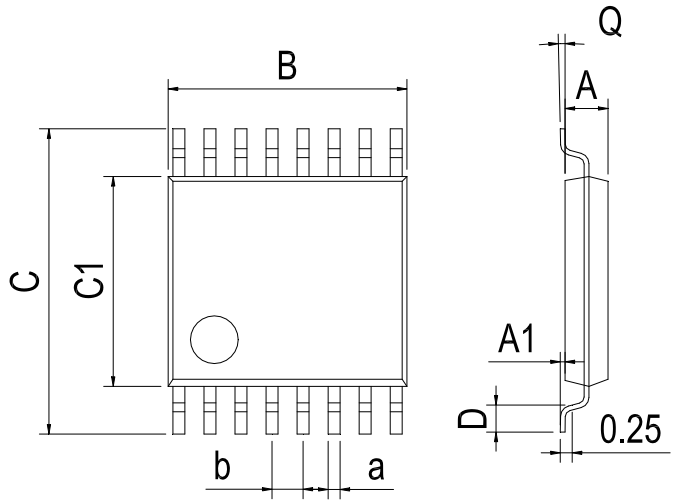
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

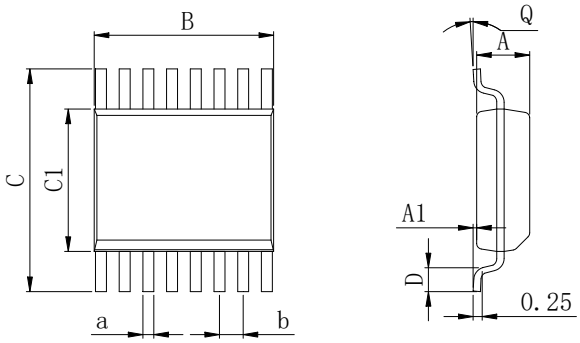
PHYSICAL DIMENSIONS

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

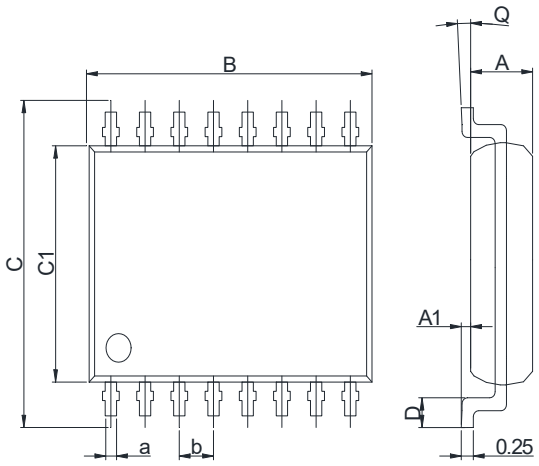
QSOP-16



Dimensions In Millimeters(QSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.80	5.80	3.80	0.40	0°	0.20	0.635 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.25	

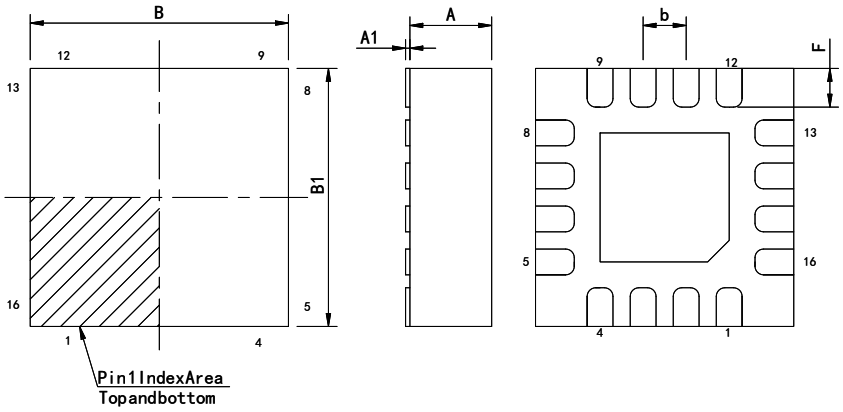
PHYSICAL DIMENSIONS

SOP-16W



Dimensions In Millimeters(SOP-16W)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.25	0.10	10.10	10.26	7.30	0.55	0°	0.35	1.27 BSC
Max:	2.35	0.30	10.50	10.60	7.70	0.85	8°	0.44	

QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	0.30	

REVISION HISTORY

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2018-8	New	1-17
V1.1	2020-10	Update encapsulation type 、 Update DIP-16 Physical dimensions 、 Add annotation for Maximum Ratings、Update Ordering Information.	1、11、14
V1.2	2024-10	Add New model TSSOP-16、QFN-16 and QSOP-16、Update Lead Temperature	1、11

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.