1. DESCRIPTION

The XL177 features one of the highest precision performance of any operational amplifier currently available. Offset voltage of the XL177 is only 50 µV maximum at room temperature. The ultralow V_{OS} of the XL177 combines with the exceptional offset voltage drift (TCV_{OS}) of 0.5 µV/°C maximum to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The XL177 open-loop gain of 12 V/µV is maintained over the full ±10 V output range. CMRR of 105 dB minimum, PSRR of 100 dB minimum, and maximum supply current of 3 mA are just a few examples of the excellent performance of this operational amplifier. The combination of outstanding specifications of the XL177 ensures accurate performance in high closed-loop gain applications.

This low noise, bipolar input operational amplifier is also a cost effective alternative to chopper-stabilized amplifiers. The XL177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The XL177 is offered in the −40°C to +85°C extended industrial temperature ranges. This product is available in 8-lead PDIP (XL177GP) , as well as the space saving 8-lead SOP (XL177GS).

2. FEATURES

- Ultralow offset voltage
  T_A = 25°C, 50 µV maximum
- Outstanding offset voltage drift 0.5 µV/°C maximum
- Excellent open-loop gain and gain linearity
  12 V/µV (typical)
- CMRR: 105 dB minimum
- PSRR: 100 dB minimum
- Low supply current 3.0 mA maximum

3. PIN CONFIGURATION

XL177GP
XL177GS

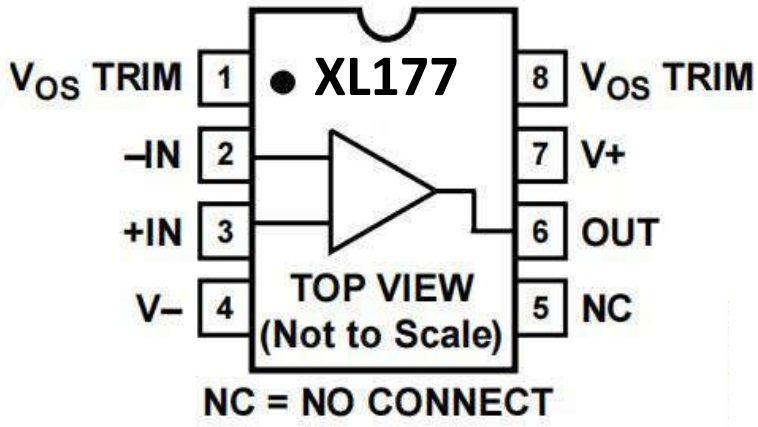
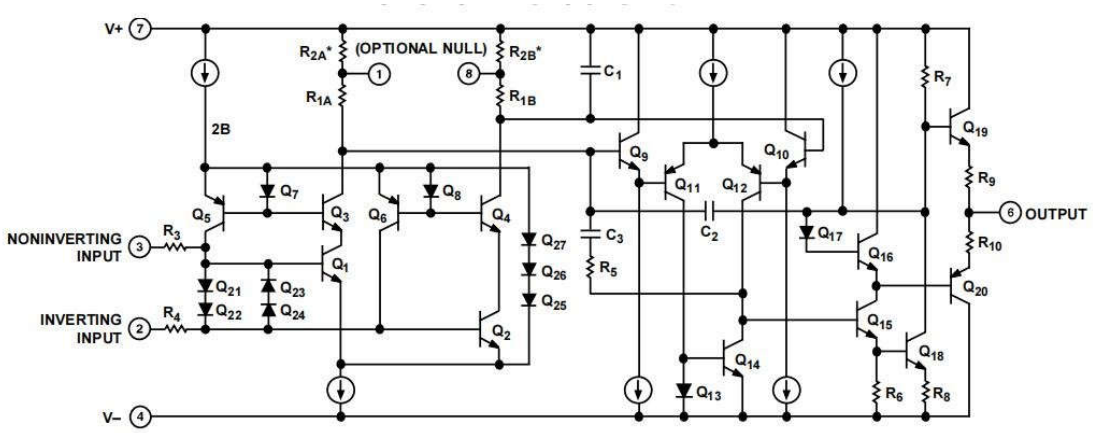


Figure 1.

4. FUNCTIONAL BLOCK DIAGRAM



*R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY

Figure 2. Simplified Schematic

5. ELECTRICAL CHARACTERISTICS

At VS = ±15 V, TA = 25°C, unless otherwise noted

Parameter	Symbol	Test Conditions/Comments	MIN	TYP	MAX	UNIT
INPUT OFFSET VOLTAGE	V_{OS}			50	100	µV
LONG-TERM INPUT OFFSET(1) Voltage Stability	ΔV_{OS}/ time			0.6		µV/mo
INPUT OFFSET CURRENT	I_{OS}			0.8	4.5	nA
INPUT BIAS CURRENT	I_B		-0.2	+1.9	+6.5	nA
INPUT NOISE VOLTAGE	e_n	fo = 1 Hz to 100 Hz(2)		125	200	nV rms
INPUT NOISE CURRENT	i_n	fo = 1 Hz to 100 Hz(2)		10	30	pA rms
INPUT RESISTANCE Differential Mode(3)	R_{in}		15	40		MΩ
INPUT RESISTANCE COMMON MODE	R_{INCM}			150		GΩ
INPUT VOLTAGE RANGE(4)	I_{VR}		±13	±14		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} =±13V	105	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	Vs=±3V to ±18V	100	120		dB
LARGE SIGNAL VOLTAGE GAIN	A_{VO}	R_L≥ 2 kQ,Vo =±10V(5)	2000	6000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 10 kQ R_L ≥2 kO R_L ≥1 kQ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5		V
SLEW RATE(2)	SR	R_L ≥2 kO	0.1	0.3		V/µs
CLOSED-LOOP BANDWIDTH(2)	BW	A_{VCL} = 1	0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O			60		Ω
POWER CONSUMPTION	P_D	Vs=±15V, no load Vs=±3V, no load		55 4.8	80 10	mW
SUPPLY CURRENT	I_{SY}	Vs =±15V, no load		1.9	3	mA
OFFSET ADJUSTMENT RANGE		R_P = 20 kO		±3		mV

(1) Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically less than 3.0 µV.
(2) Sample tested.
(3) Guaranteed by design.
(4) Guaranteed by CMRR test condition.
(5) To ensure high open-loop gain throughout the ±10 V output range,A_{VO} is tested at −10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and –10 V ≤ V_O ≤ +10 V.

At V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Parameter	Symbol	Test Conditions/Comments	MIN	TYP	MAX	UNIT
INPUT						
-Input Offset Voltage	V_{OS}			50	300	µV
-Average Input Offset Voltage Drift(1)	TCV_{OS}			0.9	2.8	µV/°C
-Input Offset Current	I_{OS}			0.5	4.5	nA
-Average Input Offset Current Drift(2)	TCL_{OS}			3.6	110	pA/°C
-Input Bias Current	L_B			+4.3	±15	nA
-Average Input Bias Current Drift(2)	TCI_B			20	95	pA/°C
-Input Voltage Range(3)	IVR		±13	±13.5		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	100	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V	95	110		dB
LARGE-SIGNAL VOLTAGE GAIN(4)	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	1000	4000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		V
POWER CONSUMPTION	P_D	V_S = ±15 V, no load		55	105	mW
SUPPLY CURRENT	I_{SY}	V_S = ±15 V, no load		1.9	3.8	mA

(1) TCV_{OS} is sample tested.
(2) Guaranteed by endpoint limits.
(3) Guaranteed by CMRR test condition.
(4) To ensure high open-loop gain throughout the ±10 V output range, AVO is tested at −10 V ≤ VO ≤ 0 V, 0 V ≤ VO ≤ +10 V, and −10 V ≤ VO ≤ +10 V.

6. TEST CORCIOTS

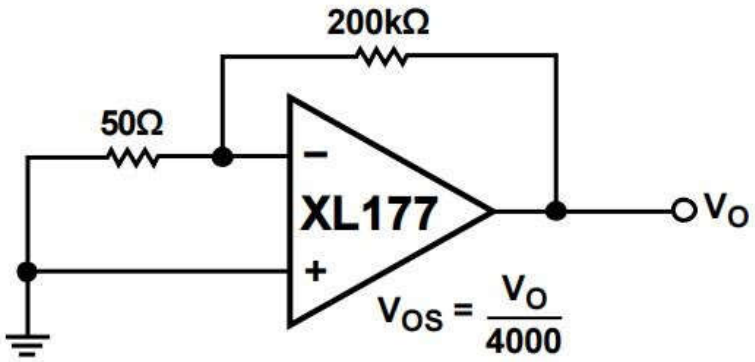


Figure 3. Typical Offset Voltage Test Circuit

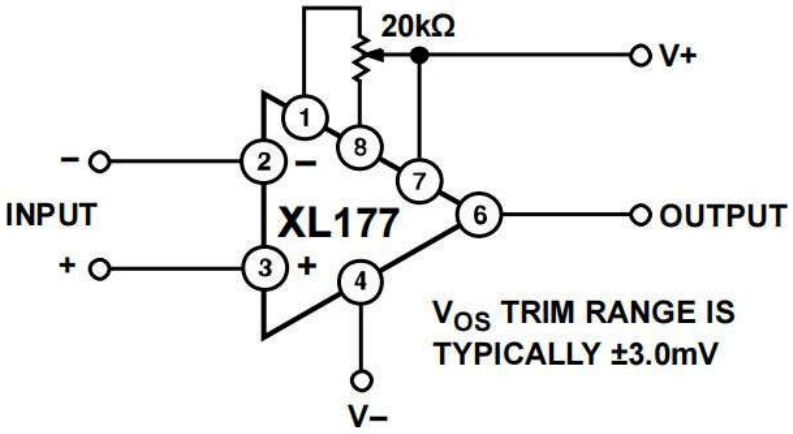


Figure 4. Optional Offset Nulling Circuit

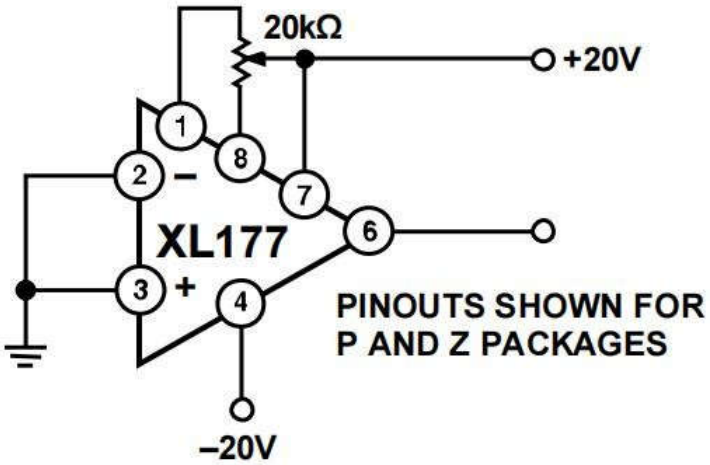


Figure 5. Burn-In Circuit

7. ABSOLUTE MAXIMUM RATINGS

Parameter	Ratings
Supply Voltage	±22 V
Internal Power Dissipation(1)	500 mW
Differential Input Voltage	±30 V
Input Voltage	±22 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (TJ)	−65°C to +150°C

(1) For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

(2) Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

8. THERMAL RESISTANCE

θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for PDIP; θ_{JA} is specified for device soldered to printed circuit board for SOP package.

Package Type	θJA	θJC	Unit
8-Lead PDIP	110	50	°C/W
8-Lead SOP	165	50	°C/W

9. ESD CAUTION

ESD (electrostatic discharge) sensitive device. charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD Precautions should be taken to avoid performance degradation or loss of functionality.

10. TYPICAL PERFORMANCE CHARACTERISTICS CURVE

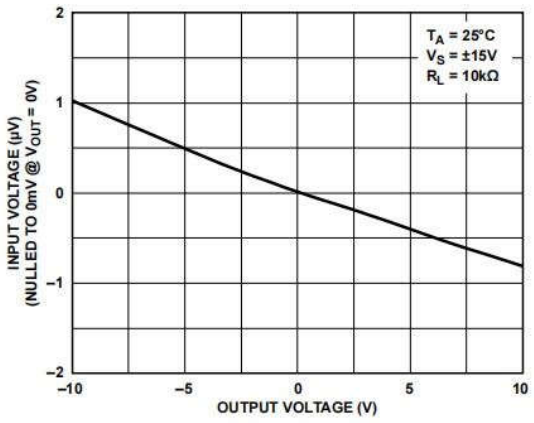


Figure6. Gain Linearity (Input Voltage vs. Output Voltage)

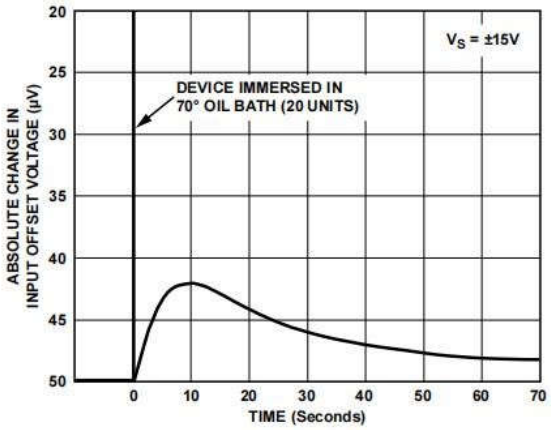


Figure 7. Offset Voltage Change Due to Thermal Shock

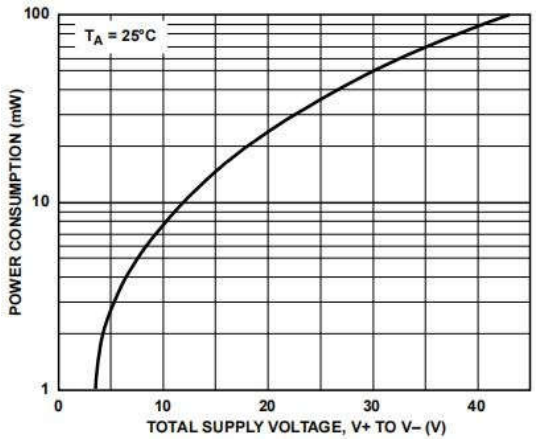


Figure 8. Power Consumption vs. Power Supply

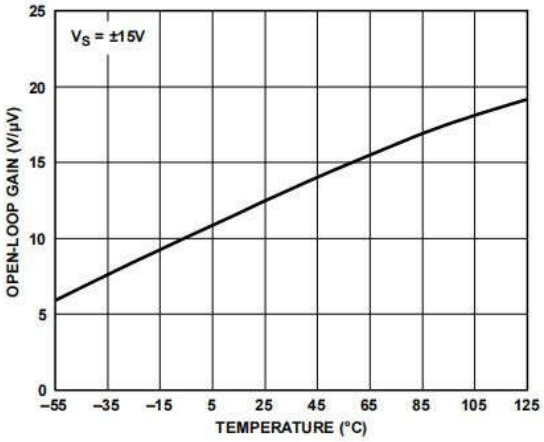


Figure 9. Open-Loop Gain vs. Temperature

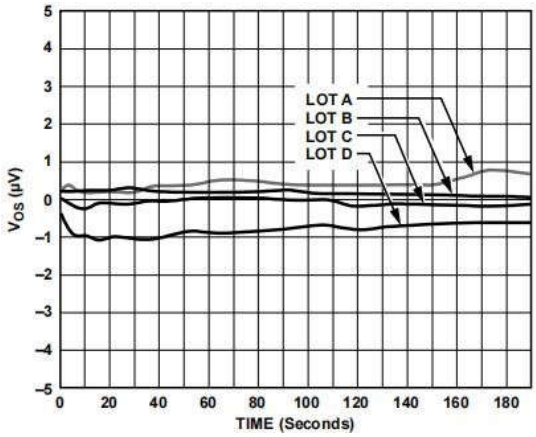


Figure 10. Warm-Up Vos Drift (Normalized) Z Package

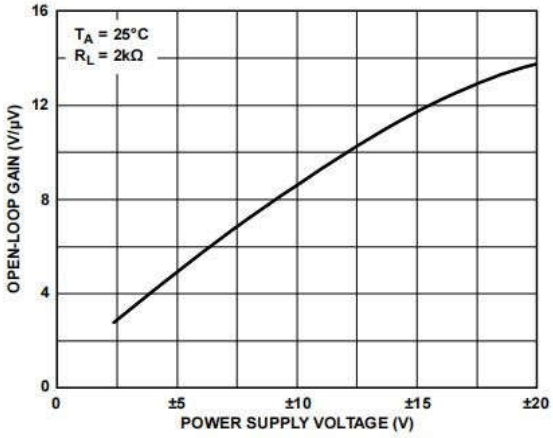


Figure 11. Open-Loop Gain vs. Power Supply Voltage

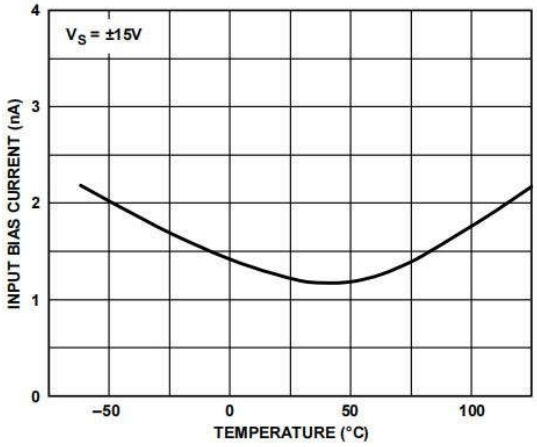


Figure 12. Input Bias Current vs. Temperature

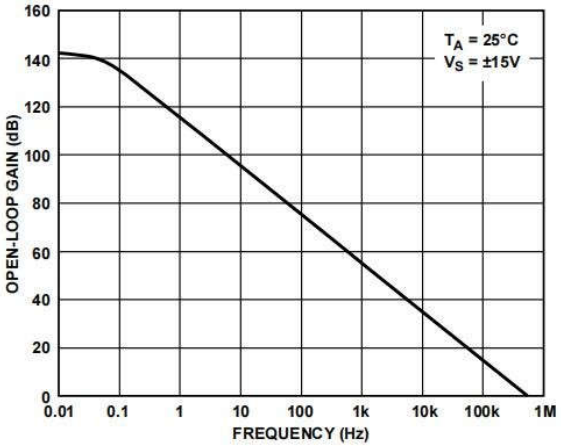


Figure 13. Open-Lpop Frequency Response

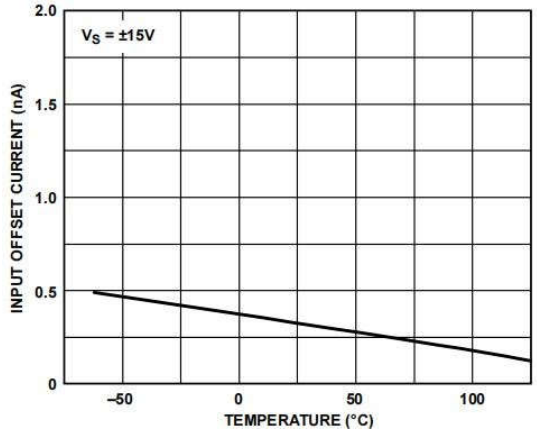


Figure 14. Input Offset Current vs. Temperature

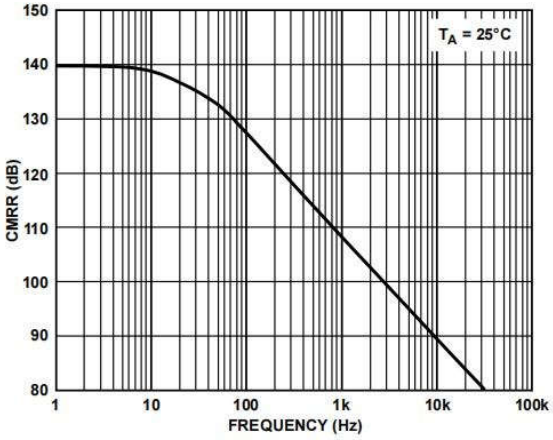


Figure 15. CMRR vs. Frequency

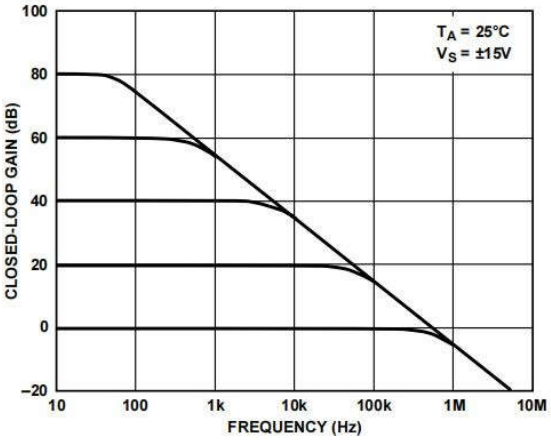


Figure 16. Closed-Loop Response for Various Gain Configurations

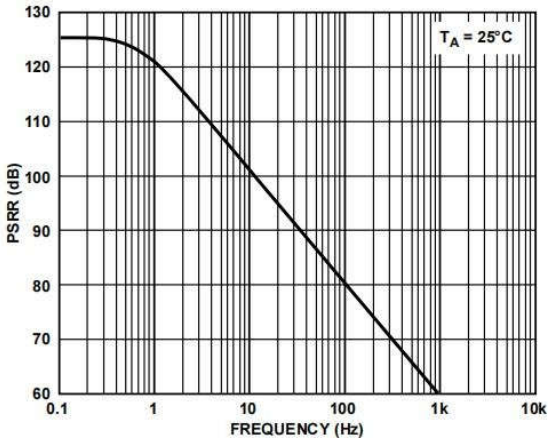


Figure 17. PSRR vs. Frequency

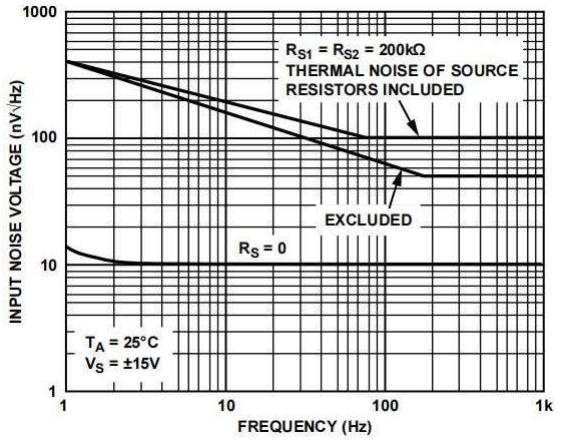


Figure 18. Total Input Noise Voltage vs. Frequency

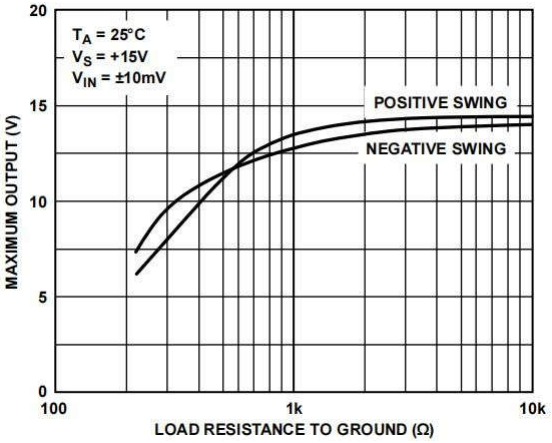


Figure 19. Maximum Output Voltage vs. Load Resistance

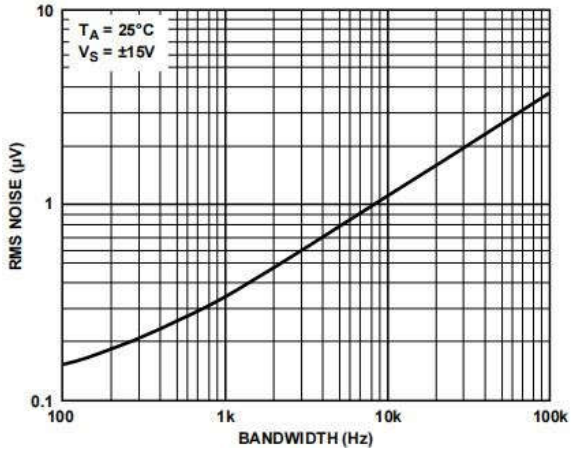


Figure 20. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

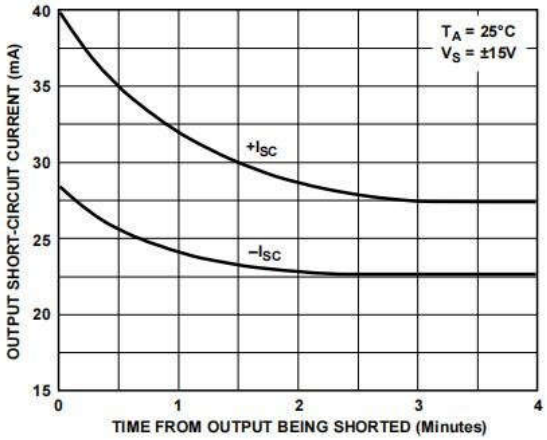


Figure 21. Output Short-Circuit Current vs. Time

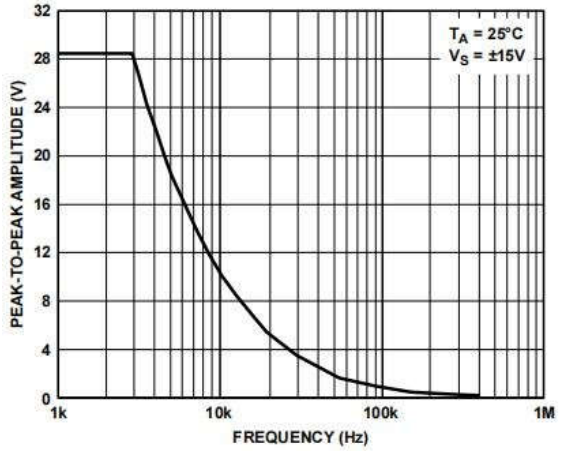


Figure 22. Maximum Output Swing vs. Frequency

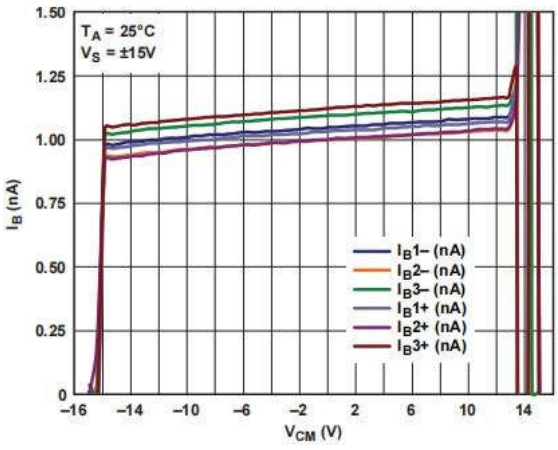


Figure 23. Input Bias (I_B) vs. Common-Mode Voltage (V_{CM})

11. APPLICATIONS INFORMATION

GAIN LINEARITY

The actual open-loop gain of most monolithic operational amplifiers varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

All automated testers use endpoint testing and, therefore, show only the average gain. For example, Figure 24 shows a typical precision operationalamplifier with a respectable open-loop gain of 650 V/ mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal operational amplifier shows a horizontal scope trace.

Figure 25 shows the XL177 output gain linearity trace with the truly impressive average AVO of 12,000 V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. Figure 26 is a simple open-loop gain test circuit.

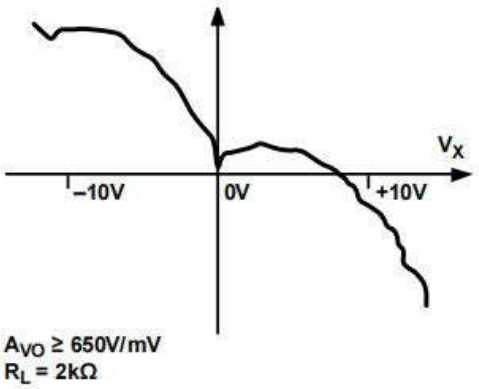


Figure24.Typical Precision Operational amplifier

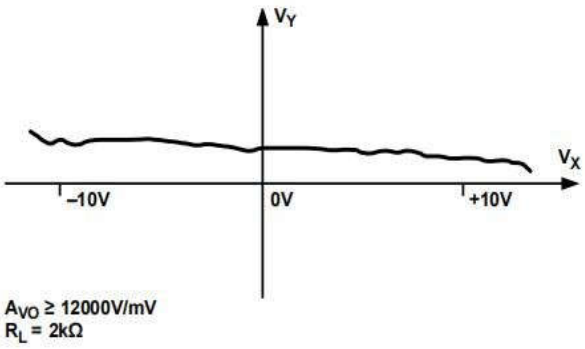


Figure25.Output Gain Linearity Trace

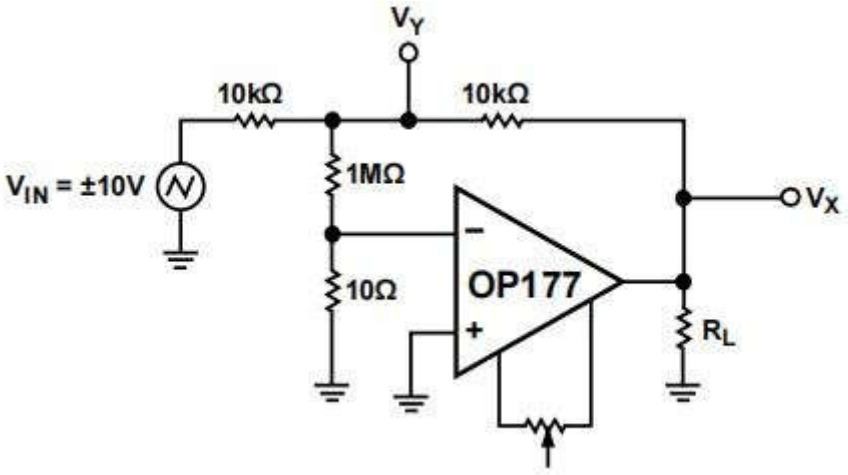


Figure 26. Open-Loop Gain Linearity Test Circuit

12. THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must accurately amplify very low level signals without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple with a Seebeck coefficient of 10.3 µV/°C produces 10.3 mV of output voltage at a temperature of 1000°C. The amplifier gain is set at 973.16, thus, it produces an output voltage of 10.024 V. Extended temperature ranges beyond 1500°C are accomplished by reducing the amplifier gain. The circuit uses a low cost diode to sense the temperature at the terminating junctions and, in turn, compensates for any ambient temperature change. The XL177, with the high open loop gain plus low offset voltage and drift, combines to yield a precise temperature sensing circuit. The table below lists the thermocouple types for other circuit values.

Thermocouple Type	Seebeck coefficient	R1	R2	R7	R9
K	39.2 µV/°C	100Ω	5.76kΩ	102kΩ	269kΩ
J	50.2 µV/°C	110Ω	4.02kΩ	80.6kΩ	200kΩ
S	10.3 µV/°C	110Ω	20.5kΩ	392kΩ	1.07MΩ

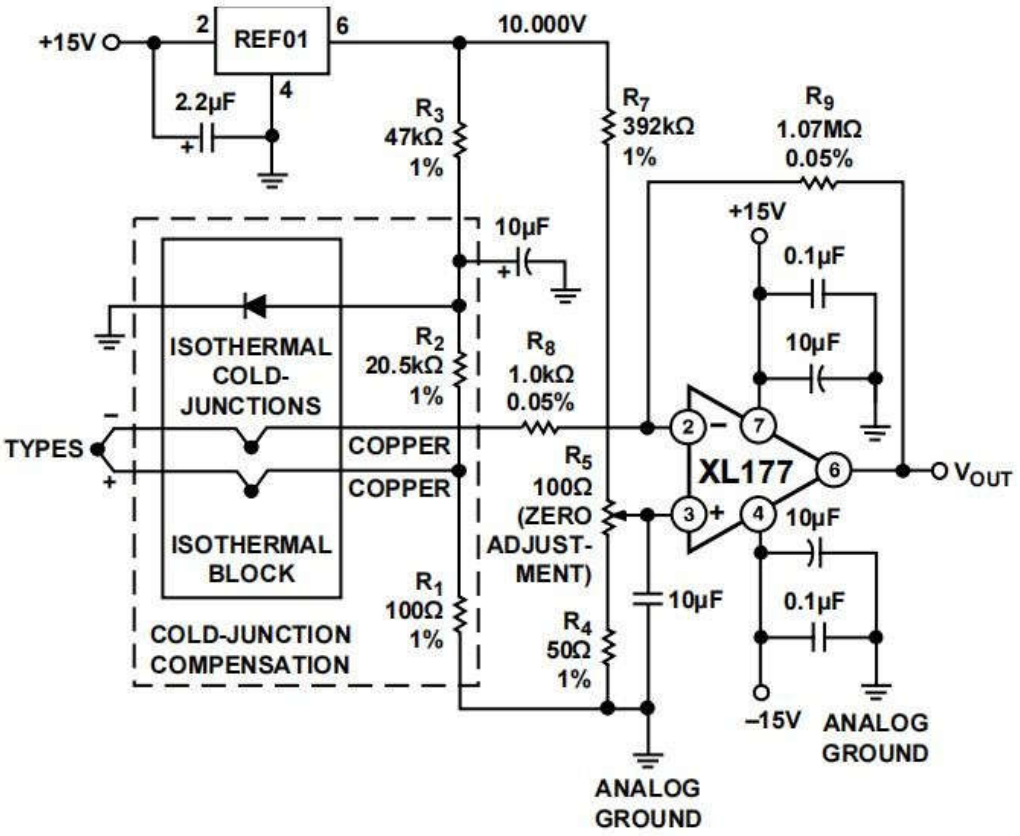


Figure 27. Thermocouple Amplifier with Cold Junction Compensation

13. PRECISION HIGH GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low TCV_{OS} of the XL177 make it possible to obtain performance not previously available in single stage, very high gain amplifier applications. See Figure 28.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$

In this example, with a 10 mV differential signal, the maximum errors are listed in Table .

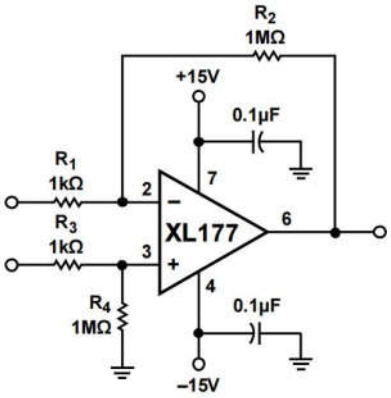


Figure 28. Precision High Gain Differential Amplifier

High Gain Differential Amplifier Performance	
Type	**Amount**
Common-Mode Voltage	0.15%/V
Gain Linearity, Worst Case	0.03%
TCV_{OS}	0.002%/°C
TCI_{OS}	0.01%/°C

14. ISOLATING LARGE CAPACITIVE LOADS

The circuit shown in Figure 29 reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the 100 Ω resistor is inside the feedback loop, the effect on output impedance is reduced to insignificance by the high open loop gain of the XL177.

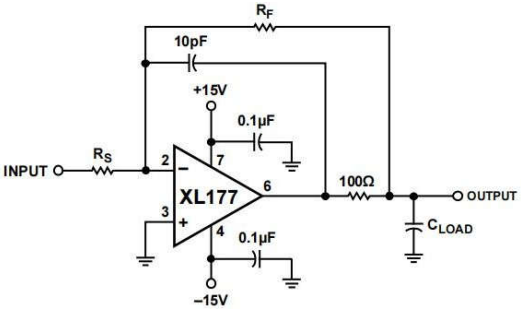


Figure 29. Isolating Capacitive Loads

15. BILATERAL CURRENT SOURCE

The current sources shown in Figure 30 supply both positive and negative currents into a grounded load. Note that:

$$Z_O = \frac{R5\left(\frac{R4}{R2}+4\right)}{\frac{R5+R4}{R2}-\frac{R3}{R1}}$$ and that for Z_O to be infinite $\frac{R5+R4}{R2}$ must $= \frac{R3}{R1}$

16. PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low TCVOS assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the operational amplifiers (for details, see Figure 31).

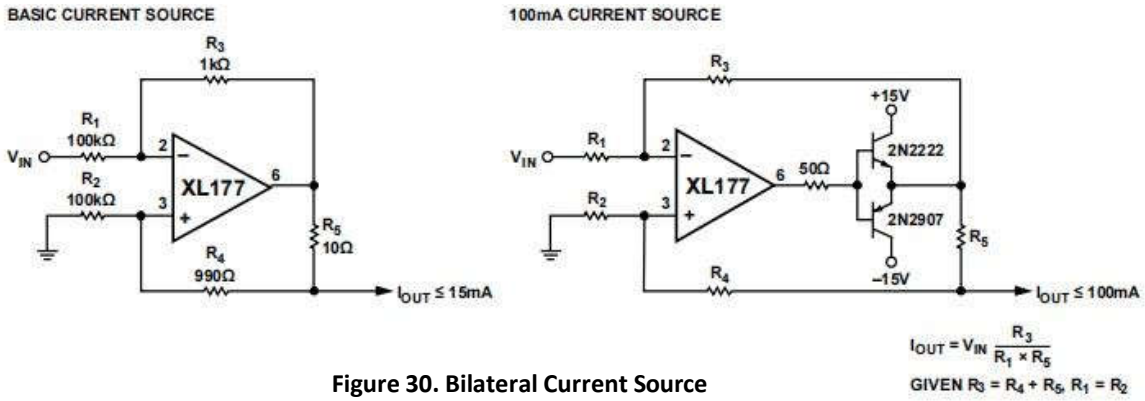


Figure 30. Bilateral Current Source

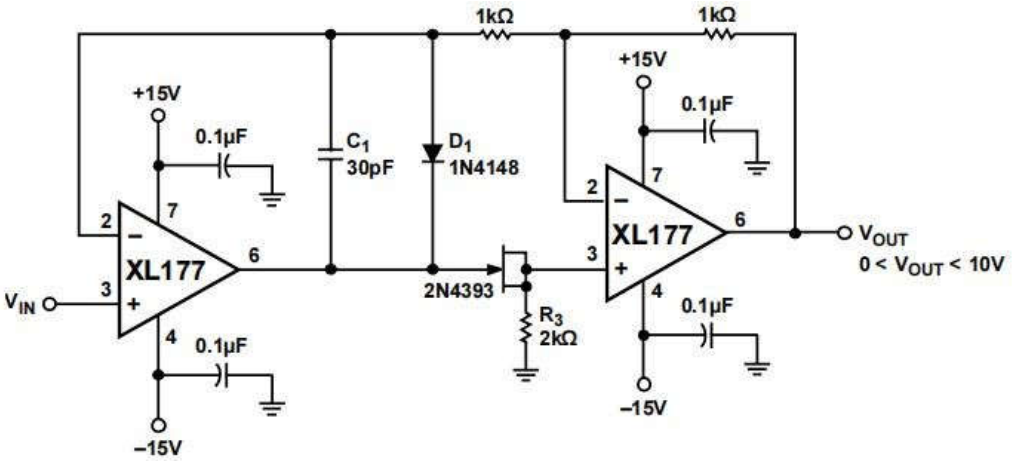


Figure 31. Precision Absolute Value Amplifier

17. PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 32, when VIN < VTH, amplifier output swings negative, reverse biasing diode D1. VOUT = VTH if RL = ∞. When $V_{IN} \geq V_{TH}$,the loop closes.

$$V_{OUT} = V_{TH} + \left(V_{IN} - V_{TH}\right)\left(1 + \frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

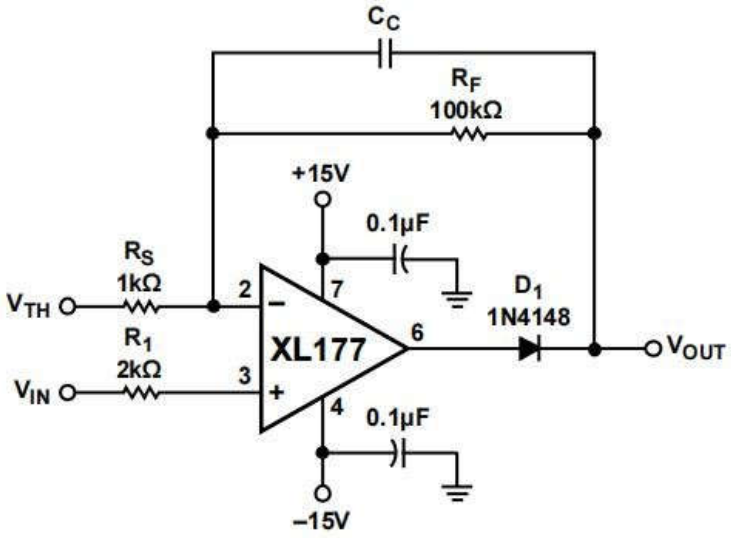


Figure 32. Precision Threshold Detector/Amplifier

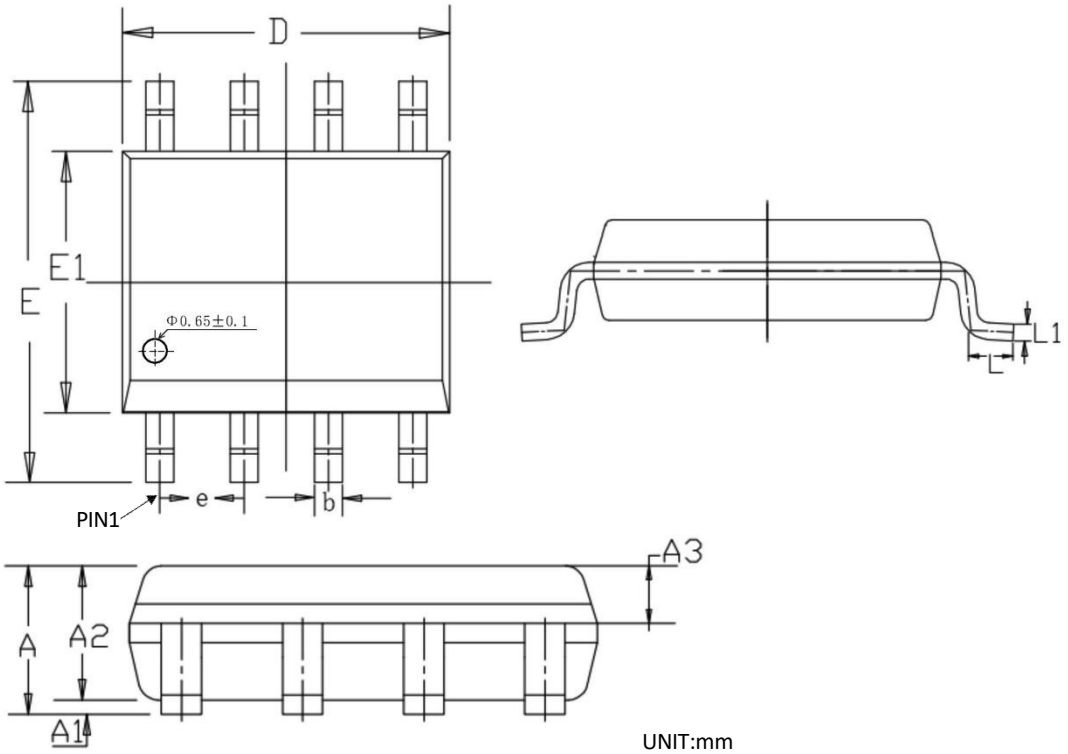
18. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL177GP	XL177P	DIP8	9.25 * 6.38	- 40 to 85	MSL3	Tube 50	2000
XL177GS	XL177G	SOP8	4.90 * 3.90	- 40 to 85	MSL3	T&R	2500

19. DIMENSIONAL DRAWINGS

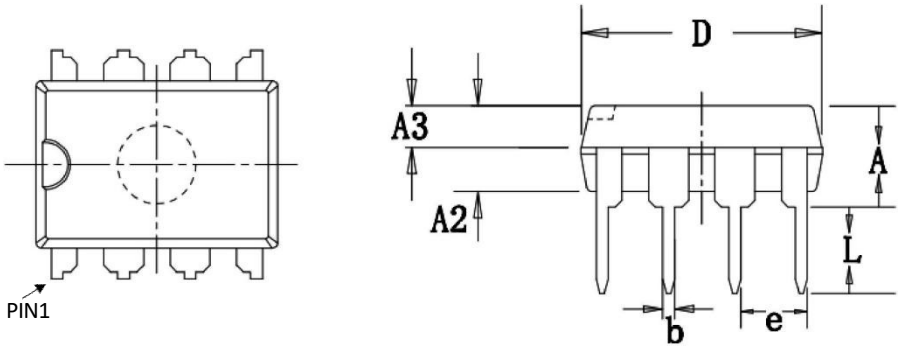
SOP8

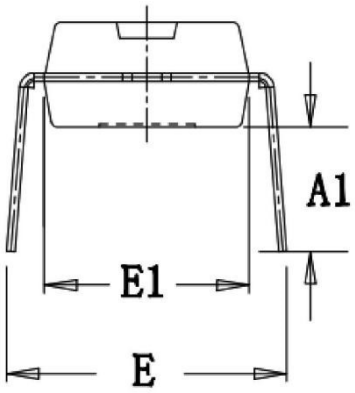


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	—	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	—	—