1. FEATURES

- HART-compliant fully integrated FSK modem
- 1200 Hz and 2200 Hz sinusoidal shift frequencies
- 112 µA maximum supply current in receive mode
- Suitable for intrinsically safe applications
- Integrated receive band-pass filter
  - Minimal external components required
- Clocking optimized for various system configurations
  - Ultralow power crystal oscillator (58 µA maximum)
  - External CMOS clock source
  - Precision internal oscillator
- Buffered HART output—extra drive capability
- 8 kV HBM ESD rating
- 2.7 V to 5.5 V power supply
- 1.71 V to 5.5 V interface
- −40°C to +125°C operation
- 4 mm × 4 mm QFN package
- HART physical layer compliant
- UART interface

2. APPLICATIONS

- Field transmitters
- HART multiplexers
- PLC and DCS analog I/O modules
- HART network connectivity

3. GENERAL DESCRIPTION

The LHE2700 are single-chip solutions, designed and specified to operate as a HART® FSK half-duplex modem, complying with the HART physical layer requirements. The LHE2700 integrate all of the necessary filtering, signal detection, modulating, demodulating and signal generation functions, thus requiring few external components. The precision internal oscillator on the LHE2700 greatly reduces the board space requirements, making it ideal for line-powered applications in both master and slave configurations. The maximum supply current consumption is 112 µA, making the LHE2700 an optimal choice for low power loop-powered applications. Transmit waveforms are phase continuous 1200 Hz and 2200 Hz sinusoids. The LHE2700 contain accurate carrier detect circuitry and use a standard UART interface.

FUNCTIONAL BLOCK DIAGRAM

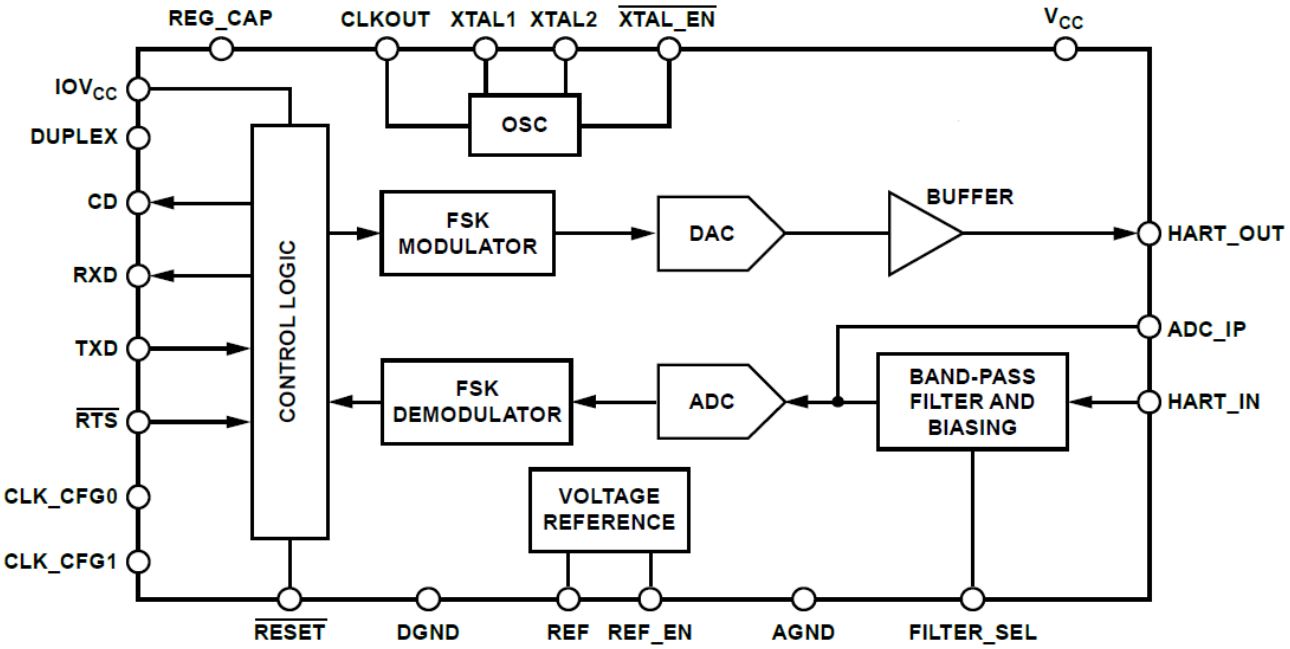

Figure 1.

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4. REVISION HISTORY

Version number	Date	Update the content
PreA	August 7, 2024	First edition
PreB	September 25, 2024	1. Remove LHE2700-1 2. Update TYPICAL PERFORMANCE CHARACTERISTICS
PreC	April 30, 2025	1.Update FEATURES 2.Update TYPICAL CONNECTION DIAGRAMS 3.Update TIMING CHARACTERISTICS
RevA	June.17, 2025	1.Update CD Assert 2.Update Transmit Impedance

5. SPECIFICATIONS

V_{CC} =2.7 V to 5.5 V, IOV_{CC} = 1.71 V to 5.5 V, AGND = DGND, CLKOUT disabled, HART_OUT with 5 nF load, internal and external receive filter, internal reference; all specifications are from −40°C to +125°C , unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS[2]					
V_{CC}	2.7		5.5	V	
IOV_{CC}	1.71		5.5	V	
V_{CC} and IOV_{CC} Current Consumption					
Demodulator		86	112	µA	external clock, −40°C to +85°C
			125	µA	external clock, −40°C to +125°C
		68	94	µA	external clock, −40°C to +85°C, external reference
			105	µA	external clock, −40°C to +125 °C, external reference
Modulator		113	150	µA	external clock, −40°C to +85°C
			170	µA	external clock, −40°C to +125°C
		72	107	µA	external clock, −40°C to +85°C, external reference
			120	µA	external clock, −40°C to +125°C, external reference
Crystal Oscillator [3]		38	58	µA	External crystal, 16 pF at XTAL1 and XTAL2
		45	65	µA	External crystal, 36 pF at XTAL1 and XTAL2
Internal Oscillator [4]		87	110	µA	External crystal not required
Power-Down Mode					$\overline{RESET}$ = REF_EN = DGND
		30	50	µA	Internal reference disabled, −40°C to +85°C
			60	µA	Internal reference disabled, −40°C to +125°C
INTERNAL VOLTAGE REFERENCE					
Internal Reference Voltage	1.49	1.5	1.51	V	REF_EN = IOV_{CC} to enable use of internal reference; V_{CC} = 2.7 V minimum
Load Regulation		22		ppm/µA	Tested with 50 µA load
OPTIONAL EXTERNAL VOLTAGE					
REFERENCE					
External Reference Input Voltage	2.47	2.5	2.53	V	REF_EN = DGND to enable use of external reference, V_{CC} = 2.7 V minimum
External Reference Input Current					
Demodulator		14	16	µA	Current required by external reference in receive mode
Modulator		37	40	µA	Current required by external reference in transmit mode
Internal Oscillator		14	16	µA	Current required by external reference if using internal oscillator
Power-Down		14	16	µA	
DIGITAL INPUTS					
V_{IH}, Input High Voltage	0.7 × IOV_{CC}			V	
V_{IL}, Input Low Voltage			0.3 × OV_{CC}	V	
Input Current	−0.1		+0.1	µA	
Input Capacitance [5]		5		pF	Per pin
DIGITAL OUTPUTS					
V_{OH}, Output High Voltage	IOV_{CC} − 0.5			V	
V_{OL}, Output Low Voltage			0.4	V	
CD Assert [6]	65	85	100	mV p-p	
HART_IN INPUT[5]					
Input Voltage range	0		REF	V	External reference source
	0		1.5	V	Internal reference enabled
HART_OUT OUTPUT					
Output Voltage	460	495	510	mV p-p	AC-coupled (2.2 µF), measured at HART_OUT pin with 160 Ω load (worst-case load)
Mark Frequency[7]		1200		Hz	Internal oscillator

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Space Frequency[7]		2200		Hz	Internal oscillator
Frequency Error	−0.8		+0.8	%	Internal oscillator, −40°C to +85°C
	−1		+1	%	Internal oscillator, −40°C to +125°C
Phase Continuity Error[5]			0	Degrees	
Maximum Load Current[5]		160		Ω	Worst-case load is 160 Ω, ac-coupled with 2.2 µF. for recommended configuration if driving a resistive load
Transmit Impedance		1.5		Ω	$\overline{\text{RTS}}$ low, at the HART_OUT pin
		77		kΩ	$\overline{\text{RTS}}$ high, at the HART_OUT pin
INTERNAL OSCILLATOR					
Frequency	1.2190	1.2288	1.2386	MHz	−40°C to +85°C
	1.2165	1.2288	1.2411	MHz	−40°C to +125°C
EXTERNAL CLOCK					
External Clock Source Frequency	3.6496	3.6864	3.7232	MHz	

1. Temperature range: −40°C to +125°C; typical at 25°C.
2. Current consumption specifications are based on mean current values.
3. The demodulator and modulator currents are specified using an external clock. If using an external crystal oscillator, the crystal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.
4. The demodulator and modulator currents are specified using an external clock. If using the internal oscillator, the internal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.
5. Guaranteed by design and characterization, but not production tested.
6. Specification set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 21).
7. If the internal oscillator is not used, frequency accuracy is dependent on the accuracy of the crystal or clock source used.

6. TIMING CHARACTERISTICS

V_{CC} = 2.7 V to 5.5 V, IOV_{CC} = 1.71 V to 5.5 V, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	1	Bit time[2] max	Carrier start time. Time from $\overline{\text{RTS}}$ falling edge to carrier reaching its first peak.
t_2	1	Bit time[2] max	Carrier stop time. Time from $\overline{\text{RTS}}$ rising edge to carrier amplitude dropping below the minimum receive amplitude.
t_3	1	Bit time[2] max	Carrier decay time. Time from $\overline{\text{RTS}}$ rising edge to carrier amplitude dropping to ac zero.
t_4	6	Bit times[2] max	Carrier detect on. Time from carrier on to CD rising edge.
t_5	6	Bit times[2] max	Carrier detect off. Time from carrier off to CD falling edge.
t_6	10	Bit times[2] max	Carrier detect on when switching from transmit mode to receive mode in the presence of a constant valid carrier. Time from $\overline{\text{RTS}}$ rising edge to CD rising edge.
t_7	2.2	ms typ	Crystal oscillator power-up time. On application of a valid power supply voltage at V_{CC} or on enabling of the oscillator via the $\overline{\text{XTAL\_EN}}$ pin. Crystal load capacitors = 16 pF.
t_8	6	ms typ	Crystal oscillator power-up time. Crystal load capacitors = 36 pF.
t_9	26	µs typ	Internal oscillator power-up time. On application of a valid power supply voltage at V_{CC} or on enabling of the oscillator via the CLK_CFG0 and CLK_CFG1 pins.
t_{10}	2	ms typ	Reference power-up time.
t_{11}	36	µs typ	Transition time from power-down mode to normal operating mode (external clock source, external reference).

1. Specifications apply to LHE2700 configured with internal or external receive filter.
2. Bit time is the length of time to transfer one bit of data (1 bit time = 1/1200 Hz = 833.333 µs).

7. ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +7 V
IOV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
Digital Output to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
HART_OUT to AGND	−0.3 V to +2.5 V
HART_IN to AGND	−0.3 V to V_{CC} + 0.3 V or +7 V (whichever is less)
ADC_IP	−0.3 V to V_{CC} + 0.3 V or +7 V (whichever is less)
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A) Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\,MAX}$)	150°C
Power Dissipation	$(T_{J\,MAX} - T_A)/\theta_{JA}$
ESD	
Human Body Model	8 kV
Field Induced Charge Model	1.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

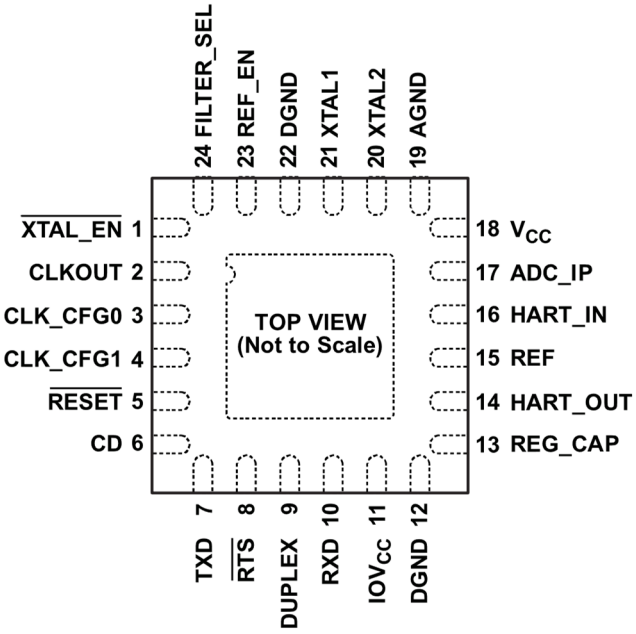
θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA1}	θ_{JC}	Unit
24-Lead QFN	56	3	°C/W

1. Thermal impedance simulated values are based on JEDEC 2S2P thermal test.

8. PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE MUST BE CONNECTED TO AGND OR DGND, OR, ALTERNATIVELY, IT CAN BE LEFT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{XTAL\_EN}}$	Crystal Oscillator Circuit Enable. A low state enables the crystal oscillator circuit, and an external crystal is required. A high state disables the crystal oscillator circuit, and an external clock source or the internal oscillator provides the clock source. This pin is used in conjunction with the CLK_CFG0 and CLK_CFG1 pins in configuring the required clock generation scheme.
2	CLKOUT	Clock Output. If using the crystal oscillator or the internal RC oscillator, a clock output can be configured at the CLKOUT pin. Enabling the clock output consumes extra current to drive the load on this pin. See the CLKOUT section for more details.
3	CLK_CFG0	Clock Configuration Control. See Table 6.
4	CLK_CFG1	Clock Configuration Control. See Table 6.
5	$\overline{\text{RESET}}$	Active Low Digital Input. Holding $\overline{\text{RESET}}$ low places the LHE2700 in power-down mode. A high state on $\overline{\text{RESET}}$ returns the LHE2700 to their power-on state. If not using this pin, tie this pin to IOV_{CC}.
6	CD	Carrier Detect—Digital Output. A high on CD indicates a valid carrier is detected.
7	TXD	Transmit Data—Digital Input. Data input to the modulator.
8	$\overline{\text{RTS}}$	Request to Send—Digital Input. A high state enables the demodulator and disables the modulator. A low state enables the modulator and disables the demodulator.
9	DUPLEX	A high state on this pin enables full duplex operation. See the Theory of Operation section. A low state disables this feature.
10	RXD	Receive Data—UART Interface Digital Data Output. Data output from the demodulator is accessed on this pin.
11	IOV_{CC}	Digital Interface Supply. Digital threshold levels are referenced to the voltage applied to this pin. The applied voltage can be in the range of 1.71 V to 5.5 V. IOV_{CC} should be decoupled to ground with low ESR 10 µF and 0.1 µF capacitors (see the Supply Decoupling section).
12	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
13	REG_CAP	Capacitor Connection for Internal Voltage Regulator. Connect a 1 µF capacitor from this pin to ground.
14	HART_OUT	HART FSK Signal Output. See the FSK Modulator section and Figure 28 for typical connections.
15	REF	Internal Reference Voltage Output, or External 2.5 V Reference Voltage Input. Connect a 1 µF capacitor from this pin to ground. When supplying an external reference, the V_{CC} supply requires a minimum voltage of 2.7 V.
16	HART_IN	HART FSK Signal. When using the internal filter, couple the HART input signal into this pin using a 2.2 nF series capacitor. If using an external band-pass filter as shown in Figure 21, do not connect to this pin.

Pin No.	Mnemonic	Description
17	ADC_IP	If using the internal band-pass filter, connect 680 pF to this pin. Alternatively, this pin allows direct connection to the ADC input, in which case an external band-pass filter network must be used, as shown in Figure 21.
18	V_{CC}	Power Supply Input. 2.7 V to 5.5 V can be applied to this pin. V_{CC} should be decoupled to ground with low ESR 10 µF and 0.1 µF capacitors (see the Supply Decoupling section).
19	AGND	Analog Circuitry Ground Reference Connection.
20	XTAL2	Connection for External 3.6864 MHz Crystal. Do not connect to this pin if using the internal RC oscillator or an external clock source.
21	XTAL1	Connection for External 3.6864 MHz Crystal or External Clock Source Input. Tie this pin to ground if using the internal RC oscillator.
22	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
23	REF_EN	Reference Enable. A high state enables the internal 1.5 V reference and buffer. A low state disables the internal reference and input buffer, and a buffered external 2.5 V reference source must be applied at REF. If REF_EN is tied low, V_{CC} must be greater than 2.7 V.
24	FILTER_SEL	Band-Pass Filter Select. A high state enables the internal filter and the HART signal should be applied to the HART_IN pin. A low state disables the internal filter and an external band-pass filter must then be connected at the ADC_IP input pin. In this case, the HART signal should be applied to the ADC_IP pin.
EPAD	EPAD	The exposed paddle must be connected to AGND or DGND, or, alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

9. TYPICAL PERFORMANCE CHARACTERISTICS

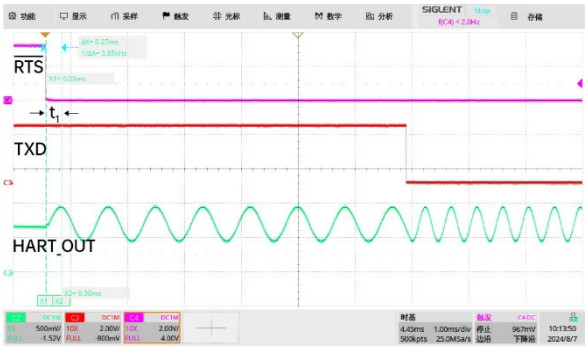


Figure 3. Carrier Start Time

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF $\overline{\text{RTS}}$ AND TXD DC LEVELS HAVE BEEN ADJUSTED FOR CLARITY. IN REALITY, BOTH OF THESE SIGNALS RANGE FROM 0V TO 3.3V.

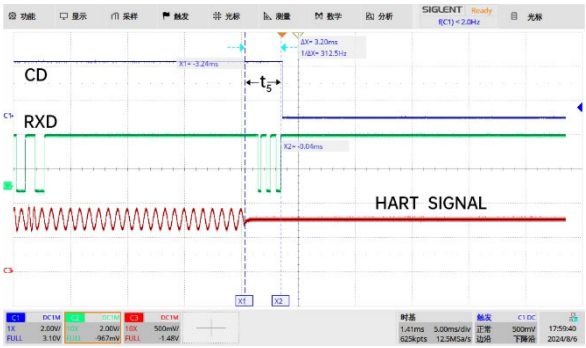


Figure 4. Carrier Detect Off Timing

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF CD AND RXD DC LEVELS HAVE BEEN ADJUSTED FOR CLARITY. IN REALITY, BOTH OF THESE SIGNALS RANGE FROM 0V TO 3.3V.

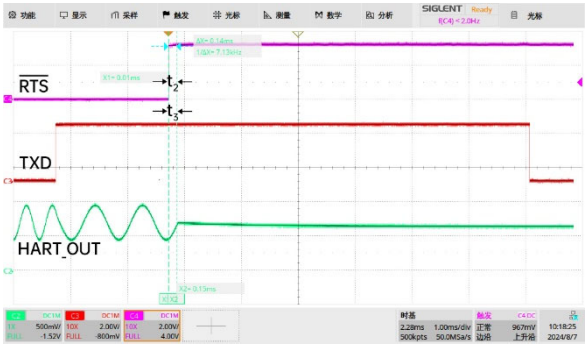


Figure 5. Carrier Stop/Decay Time

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF $\overline{\text{RTS}}$ AND TXD DC LEVELS HAVE BEEN ADJUSTED FOR CLARITY. IN REALITY, BOTH OF THESE SIGNALS RANGE FROM 0V TO 3.3V.

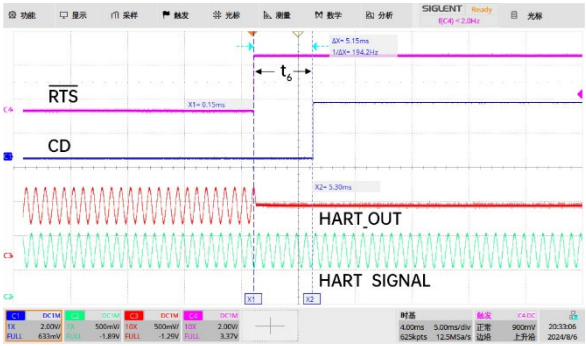


Figure 6. Carrier Detect on When Switching from Transmit Mode to Receive Mode in the Presence of a Constant Valid Carrier

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF $\overline{\text{RTS}}$ AND CD DC LEVELS HAVE BEEN ADJUSTED FOR CLARITY. IN REALITY, BOTH OF THESE SIGNALS RANGE FROM 0V TO 3.3V.

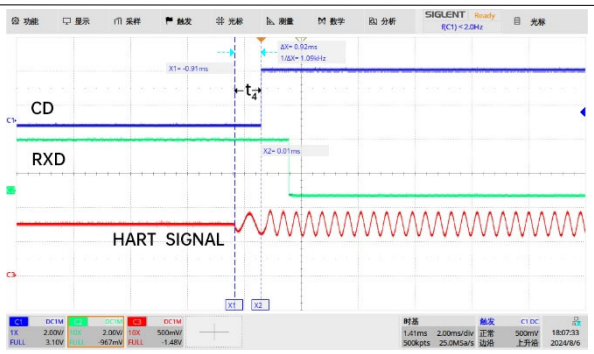


Figure 7. Carrier Detect On Timing

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF CD AND RXD DC LEVELS HAVE BEEN ADJUSTED FOR CLARITY. IN REALITY, BOTH OF THESE SIGNALS RANGE FROM 0V TO 3.3V.

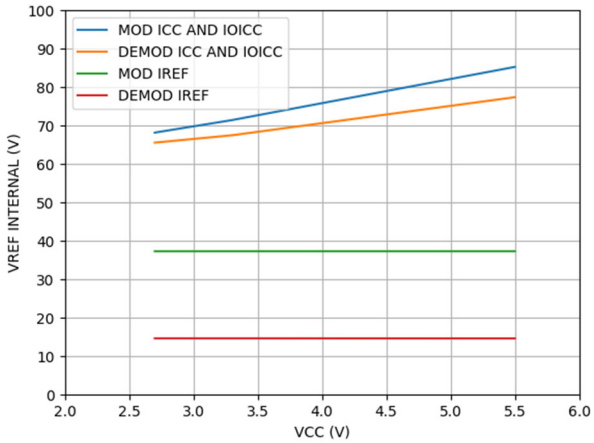


Figure 8. Supply Currents vs. Supply Voltage—External Reference

TA = 25°C VCC = IOVCC = 2.7V TO 5.5V EXT REF

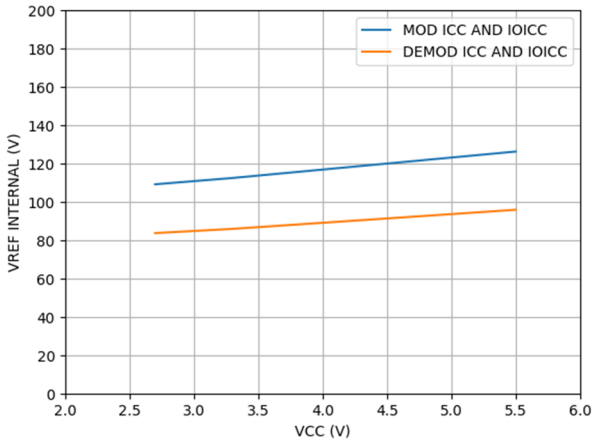


Figure 9. Supply Currents vs. Supply Voltage—Internal Reference

TA = 25°C VCC = IOVCC = 2.7V TO 5.5V INT REF

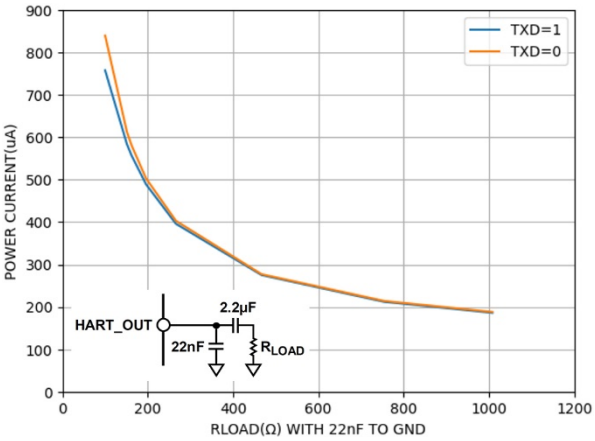


Figure 10. Current in Tx Mode vs. Resistive Load

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF CLK CONFIG = XTAL OSCILLATOR 16 pF at XTAL1 and XTAL2

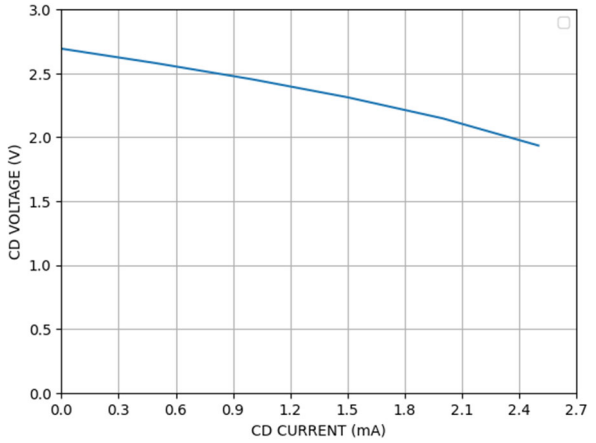


Figure 11. Carrier Detect—Voltage vs. Current, 2 V

TA = 25°C VCC = IOVCC = 2.7V

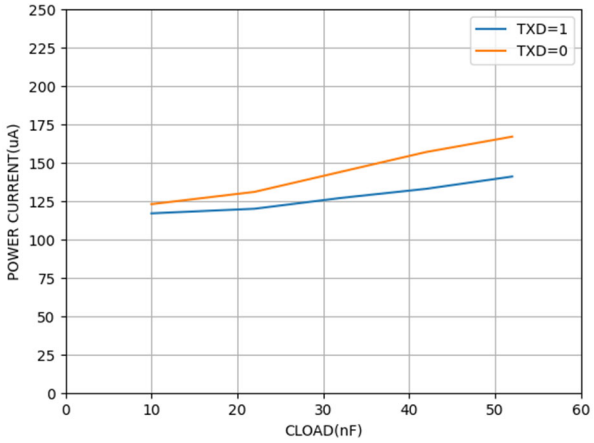


Figure 12. Current in Tx Mode vs. Capacitive Load

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF CLK CONFIG = XTAL OSCILLATOR 16 pF at XTAL1 and XTAL2

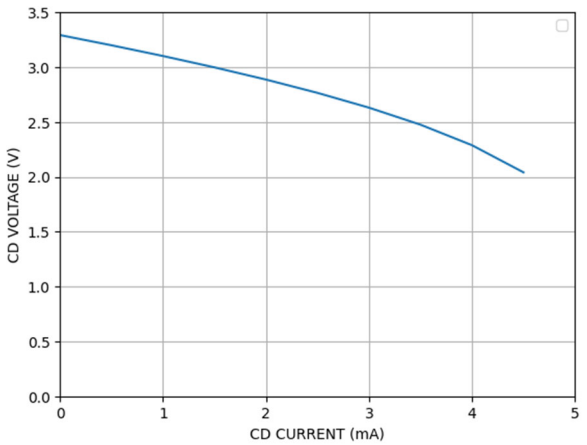


Figure 13. Carrier Detect—Voltage vs. Current, 3.3 V

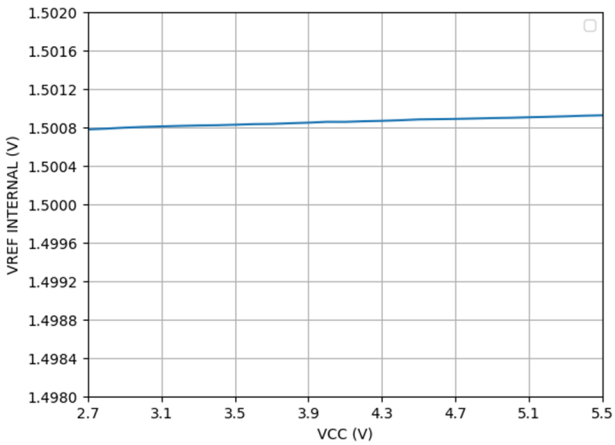


Figure 14. Reference Voltage vs. VCC

TA = 25°C VCC = IOVCC = 3.3V

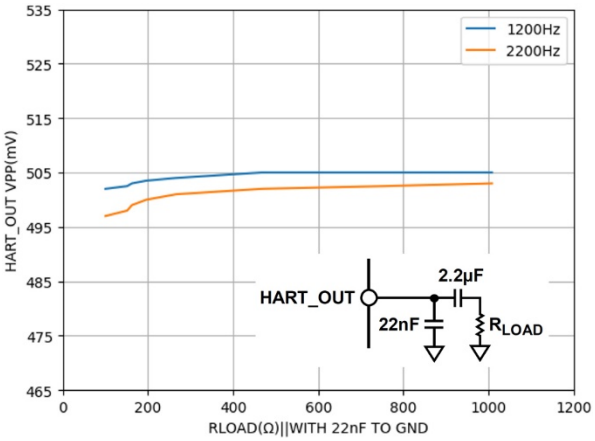


Figure 15. HART_OUT Voltage vs. R_{LOAD}

TA = 25°C; VCC = IOVCC = 1.71V TO 5.5V

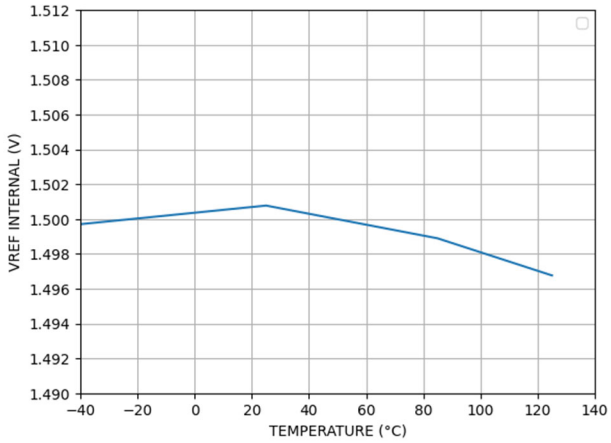


Figure 16. Reference Voltage vs. Temperature

TA = 25°C ; VCC = IOVCC = 3.3V; INT VREF

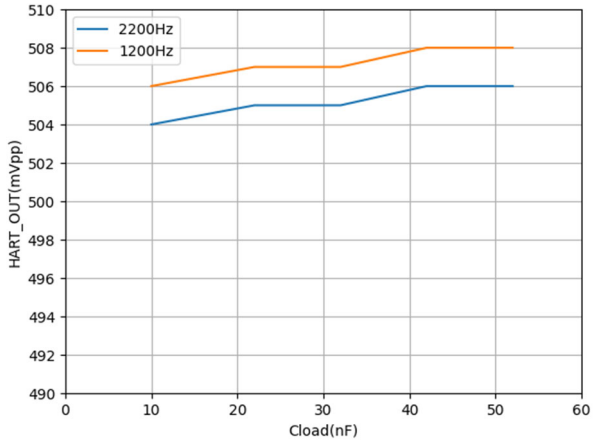


Figure 17. HART_OUT Voltage vs. C_{LOAD}

VCC = IOVCC = 3.3V; TEMPERATURE = –40°C TO +125°C

TA = 25°C; VCC = IOVCC = 3.3V; INT VREF CAPACITIVE LOAD ONLY

10. THEORY OF OPERATION

Highway Addressable Remote Transducer (HART) Communication is the global standard for sending and receiving digital information across analog wires between smart field devices and control systems. This is a digital two-way communication system, in which a 1 mA p-p frequency shift keyed (FSK) signal is modulated on top of a 4 mA to 20 mA analog current signal. The LHE2700 are designed and specified to operate as a single-chip, low power, HART FSK half-duplex modem, complying with the HART physical layer requirements (Revision 8.1).

A single-chip solution, the LHE2700 not only integrate the modulation and demodulation functions, but also contain an internal reference, an integrated receive band-pass filter (which has the flexibility of being bypassed if required), and an internally buffered HART output, giving a high output drive capability and removing the need for external buffering. The LHE2700 also contains a precision internal RC oscillator. The block diagram in Figure 1 shows a graphical illustration of how these circuit blocks are connected together. As a result of such extensive integration options, minimal external components are required. The LHE2700 are suitable for use in both HART field instrument and master configurations.

The LHE2700 either transmit or receive 1.2 kHz and 2.2 kHz carrier signals. A 1.2 kHz signal represents a digital 1, or mark, whereas a 2.2 kHz signal represents a 0, or space. There are three main clocking configurations supported by these parts:

- External crystal
- CMOS clock input
- Internal RC oscillator

The device is controlled via a standard UART interface. The relevant signals are $\overline{\text{RTS}}$, CD, TXD, and RXD (see Table 5 for more detail on individual pin descriptions).

10.1.FSK MODULATOR

The modulator converts a bit stream of UART-encoded HART data at the TXD input to a sequence of 1200 Hz and 2200 Hz tones (see Figure 18). This sinusoidal signal is internally buffered and output on the HART_OUT pin. The modulator is enabled by bringing the $\overline{\text{RTS}}$ signal low.

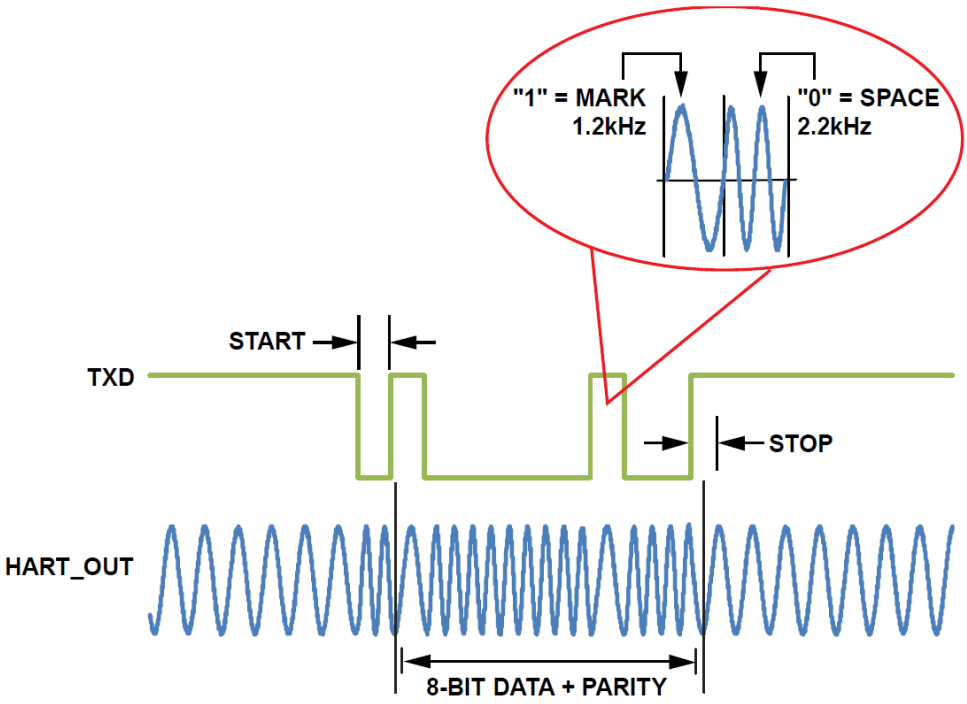


Figure 18. LHE2700 Modulator Waveform

The modulator block contains a DDS engine that produces a 1.2 kHz or 2.2 kHz sine wave in digital form and then performs a digital-to-analog conversion. This DDS engine inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. Figure 19 demonstrates a simple implementation of this FSK encoding.

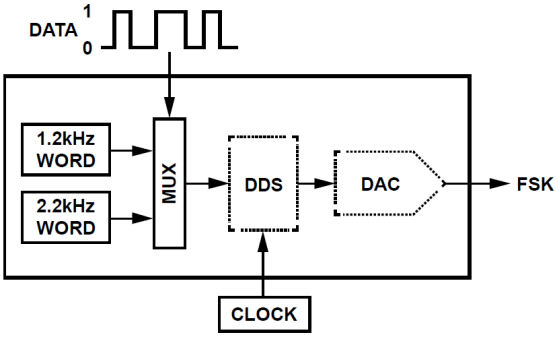


Figure 19. DDS-Based FSK Encoder

10.2.FSK DEMODULATOR

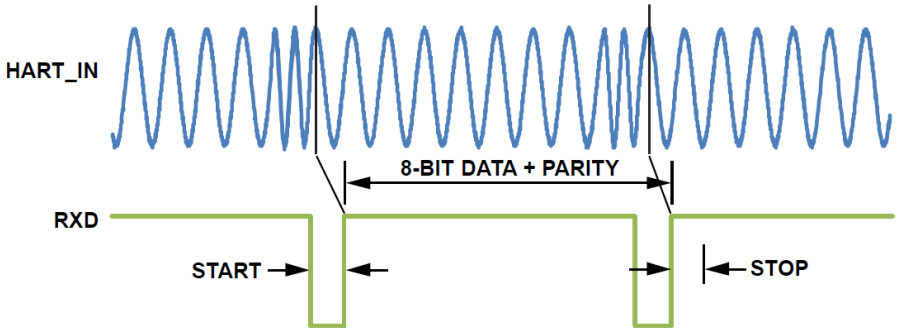


Figure 20. LHE2700 Demodulator Waveform (Preamble Message 0xFF)

When LHE2700 are in receive mode. A high on CD indicates a valid carrier is detected. The demodulator accepts an FSK signal at the HART_IN pin and restores the original modulated signal at the UART interface digital data output pin, RXD. The combination of the ADC, digital filtering and digital demodulation results in a highly accurate output on the RXD pin. The HART bit stream follows a standard UART frame with a start bit, 8-bit data, one parity, and a stop bit (see Figure 20). RTS is logic high, the modulator is disabled and the demodulator is enabled, that is, the

10.3.CONNECTING TO HART_IN OR ADC_IP

The LHE2700 have two filter configuration options: an external filter (HART signal is applied to ACP_IP) and an internal filter (HART signal is applied to HART_IN).

The external filter configuration is shown in Figure 21. In this case, the HART signal is applied to the ADC_IP pin through an external filter circuit. In safety critical applications, the LHE2700 must be isolated from the high voltage of the loop supply. The recommended external band-pass filter includes a 150 kΩ resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments. Assuming the use of a 1% accurate resistor and 10% accurate capacitor components, the calculated variation in CD trip voltage levels vs. the ideal is ±3.5 mV.

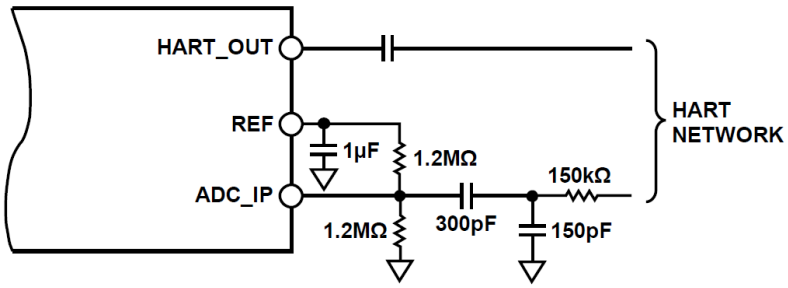


Figure 21. LHE2700 with External Filter on ADC_IP

The internal filter configuration is shown in Figure 22. This option is beneficial where cost or board space is a large concern because it removes the need for multiple external components. This configuration achieves an 8 kV ESD HBM rating but requires extra external protection circuitry for EMC and surge protection purposes if used in harsh industrial environments.

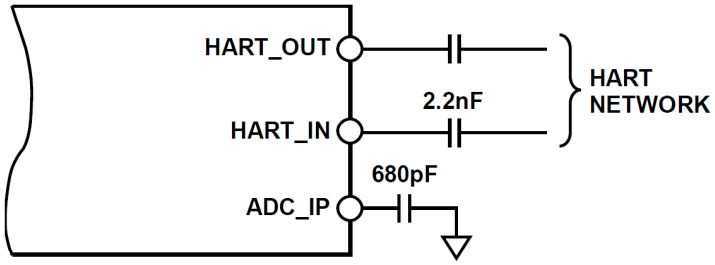


Figure 22. LHE2700 Using Internal Filter on HART_IN

10.4.CLOCK CONFIGURATION

The LHE2700 support numerous clocking configurations to allow the optimal trade-off between cost and power:
- External crystal
- CMOS clock input
- Internal RC oscillator

The CLK_CFG0, CLK_CFG1, and $\overline{\text{XTAL\_EN}}$ pins configure the clock generation as shown in Table 6. The LHE2700 can also provide a clock output at CLKOUT (for more details, see the CLKOUT section).

External Crystal

The typical connection for an external crystal (ABLS-3.6864MHZ-L4Q-T) is shown in Figure 23. To ensure minimum current consumption and to minimize stray capacitances, connections between the crystal, capacitors, and ground should be made as close to the LHE2700 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

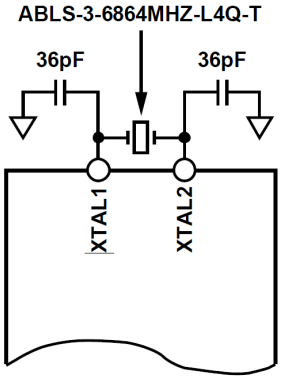


Figure 23. Crystal Oscillator Connection

The ABLS-3.6864MHZ-L4Q-T crystal oscillator data sheet recommended two 36 pF capacitors. Because the crystal current consumption is dominated by the load capacitance, in an effort to reduce the crystal current consumption, two 16 pF capacitors were used on the XTAL1 and XTAL2 pins. The LHE2700 still functioned as expected, even with the resulting reduction in frequency performance from the crystal due to the smaller capacitance values. Crystals are available that support 16 pF capacitors. It is recommended to consult the relevant crystal manufacturers for this information.

CMOS Clock Input

A CMOS clock input can also be used to generate a clock for the LHE2700. To use this mode, connect an external clock source to the XTAL 1 pin, and leave XTAL2 open circuit (see Figure 24).

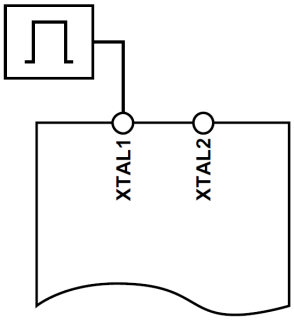


Figure 24. CMOS Clock Connection

Internal Oscillator

Consuming typically 87μA, the low power, internal, 0.8 % precision RC oscillator has an oscillation frequency of 1.2288 MHz. To use this mode, tie the XTAL1 pin to ground and leave the XTAL2 pin open circuit (see Figure 25).

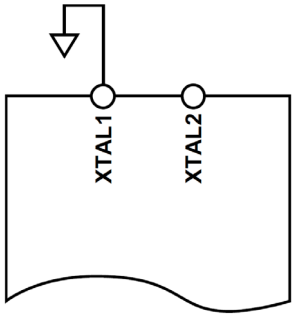


Figure 25. Internal Oscillator Connection

CLKOUT

The LHE2700 can provide a clock output at CLKOUT (see Table 6).
• If using the crystal oscillator, this clock output can be configured as a 3.6864 MHz, 1.8432 MHz, or 1.2288 MHz buffer clock.
• If using a CMOS clock, no clock output can be configured at the CLKOUT pin.
• If using the internal RC oscillator, this clock output is only available as a 1.2288 MHz buffer clock.

The amplitude of the clock output depends on the IOVCC level; therefore, the clock output can be in the range of 1.71 V p-p to 5.5 V p-p. Enabling the clock output of the LHE2700 increases the current consumption of the device. This increase is due to the current required to drive any load at the CLKOUT pin, which should not be more than 30 pF.

This capacitance should be minimized to reduce current consumption and provide the clock with the cleanest edges. The additional current drawn from the IOVCC supply can be calculated using the following equation:

$I = C \times V \times f$

Table 6. Clock Configuration Options

$\overline{\text{XTAL\_EN}}$	CLK_CFG1	CLK_CFG0	CLKOUT	Description
1	0	0	No output	3.6864 MHz CMOS clock connected at XTAL1 pin
1	0	1	No output	1.2288 MHz CMOS clock connected at XTAL1 pin
1	1	0	No output	Internal oscillator enabled
1	1	1	1.2288 MHz output	Internal oscillator enabled, CLKOUT enabled
0	0	0	No output	Crystal oscillator enabled
0	0	1	3.6864 MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	0	1.8432 MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	1	1.2288 MHz output	Crystal oscillator enabled, CLKOUT enabled

POWER-DOWN MODE

The LHE2700 can be placed into power-down mode by holding the RESET pin low. If using the internal reference, it is recommended to tie the REF_EN pin to the RESET pin so that it is also powered down.

In this mode, the receive, transmit, and oscillator circuits are all switched off, and the device consumes a typical current of 30 µA.

FULL DUPLEX OPERATION

Full duplex operation means that the modulator and demodulator of the LHE2700 are enabled at the same time. This is a powerful feature, enabling a self-test procedure of not only the HART device but also the complete signal path between the HART device and the host controller. This provides verification that the local communications loop is functional. This increased level of system diagnostics is useful in production self-test and is advantageous in improving the application's safety integrity level (SIL) rating. The full duplex mode of operation is enabled by connecting the DUPLEX pin to logic high.

11. APPLICATIONS INFORMATION

11.1. SUPPLY DECOUPLING

It is recommended to decouple the VCC and IOVCC supplies with 10 µF in parallel with 0.1 µF capacitors to ground. For many applications, 1 µF in parallel with 0.1 µF ceramic capacitors to ground should be sufficient. Decouple this REG_CAP supply with a 1 µF ceramic capacitor to ground. It is also required to decouple the REF pin with a 1 µF ceramic capacitor to ground. Place decoupling capacitors as close to the relevant pins as possible.

For loop-powered applications, it is recommended to connect a resistance in series with the VCC supply to minimize the effect of any noise, which may, depending on the system configuration, be introduced onto the loop as a result of current draw variations from the LHE2700. For typical applications, 470 Ω of resistance has proven most effective. However, depending on the application conditions, alternative values may also be acceptable.

11.2. TRANSIENT VOLTAGE PROTECTION

Many industrial control applications have requirements for HART-enabled current input and output modules. Figure 26 shows an example of a HART-enabled current input module that contains transient voltage protection circuitry, which is very important in harsh industrial control environments.

The module is powered from a 24 V field supply, and the 250 Ω load is within the low impedance module itself. This configuration is in contrast to Figure 27, which demonstrates a secondary HART device, in which the load is outside of the module. For transient voltage protection, a 10 V unidirectional (for protection against positive high voltage transients) transient voltage suppressor (TVS) is placed at the connection point of the current input module. The TVS component that is used in a given application circuit must have power ratings that are appropriate to the individual system. When choosing the TVS, low leakage current is also an important specification for maintaining the accuracy of the analog current input. In the event of a transient spike, the 22 Ω series resistor acts as a current limiting resistor for the FSK output pin. The FSK input pin is inherently protected by the 150 kΩ resistor, which forms part of the recommended external filter circuitry at the FSK input. The voltage divider, made up of both a 75 kΩ resistor and a 22 kΩ resistor, is used to maintain a 0.75 V dc bias at the field side of the FSK output switch.

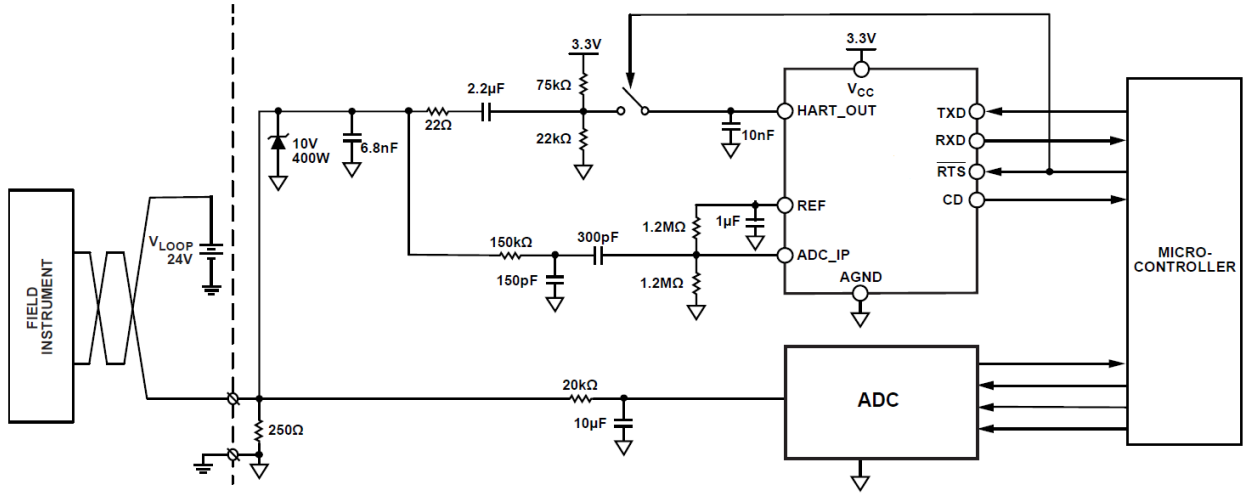


Figure 26. Current Input Module, HART Circuit

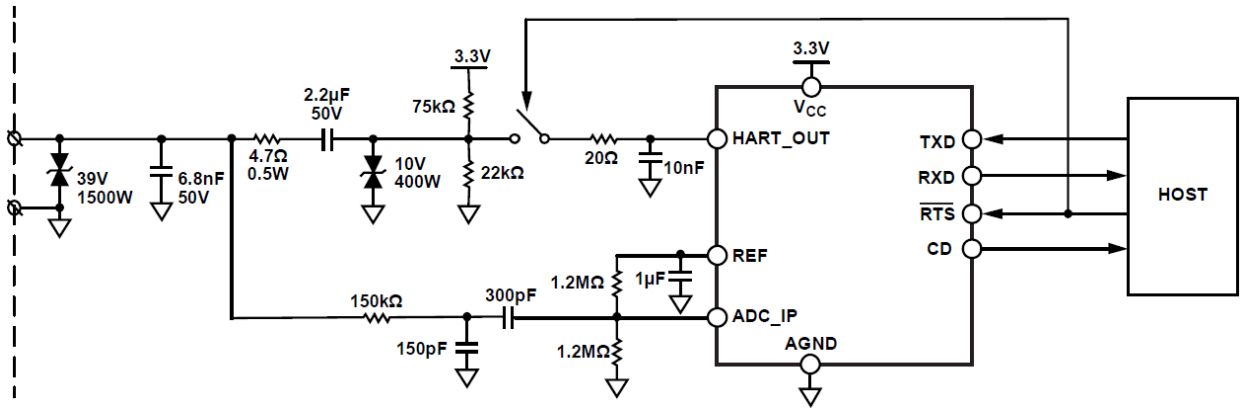


Figure 27. Secondary HART Device

As previously mentioned, Figure 27 shows an example secondary HART device, incorporating two-stage protection circuitry. In this example, a bidirectional (for protection against both positive and negative high voltage transients) TVS is included to provide flexibility in the polarity of the connection points of the module. Because this module could be connected to any point on the current loop, the higher TVS rating was chosen. The lower rated second stage provides added protection for the LHE2700 device.

11.3. TYPICAL CONNECTION DIAGRAMS

Figure 28 shows a typical connection diagram for the LHE2700 using the external and internal options. See the Connecting to HART_IN or ADC_IP section for more details.

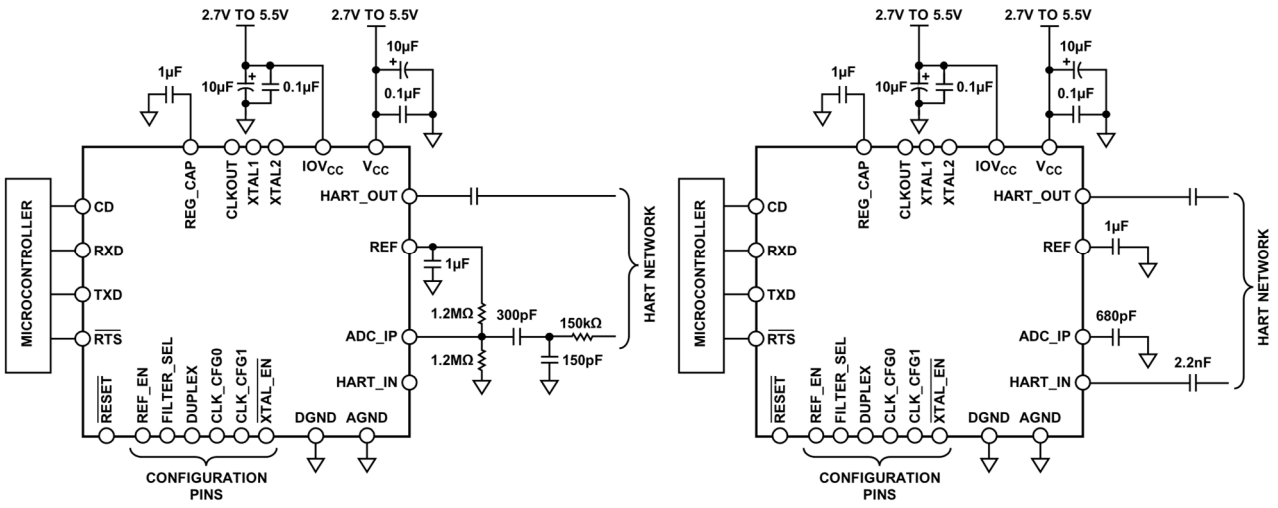
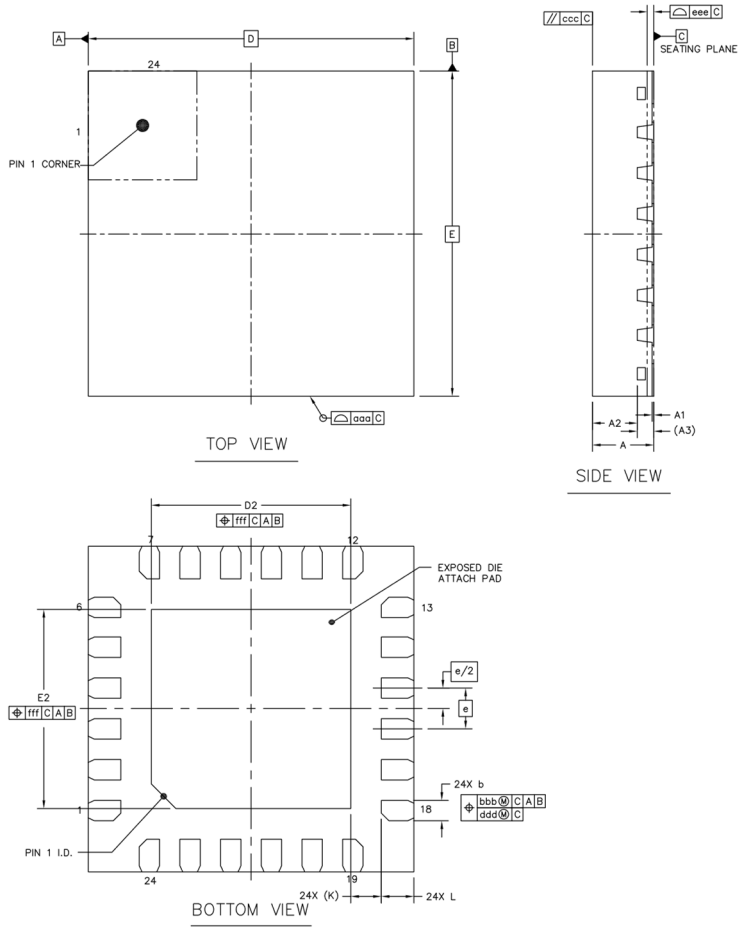


Figure 28. LHE2700 Typical Connection Diagram for External and Internal Filter Options

12. OUTLINE DIMENSIONS



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.35	2.45	2.55
	Y	E2	2.35	2.45	2.55
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.375 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP ·Sn8~20s

Figure 29. Package Description

12.1. ORDERING GUIDE

Table 7. Ordering Guide

Orderable Device	Package Type	Pin number	Op Temp (°C)	MPQ	Remark
LHE2700FQG	QFN	24	-40~125℃	2500EA/RELL	

Exegesis: REEL：REEL packaging;
TRAY：TRAY packaging;
TUBE：TUBE packaging.