1. FEATURES

- PGA gain from 1x to 256x
  - Noise density 6 nV/$\sqrt{\text{Hz}}$, G=128
  - RMS noise 7.1nV @ 5SPS, G=128
- Delta-sigma Analog-to-digital Converter
  - Linearity Error: 0.0002% FS
  - Noise-free Resolution: Up to 24 bits
- Two- or Four-channel Differential MUX
- All gains are factory calibrated
- Scalable VREF Input: Up to Analog Supply
- Simple Three-wire Serial Interface
  - SPI and Microwire Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- R/W Calibration Registers Per Channel
- Selectable Word Rates: 5 to 76,800 SPS
- 50/60 Hz Rejection
- Power consumption: total 3.3mA
- Internal temperature sensor
- Power Supply Configurations
  - VA+ - VA- = +3 V to +5 V;
  - VD+ = +3 V to +5 V

2. GENERAL DESCRIPTION

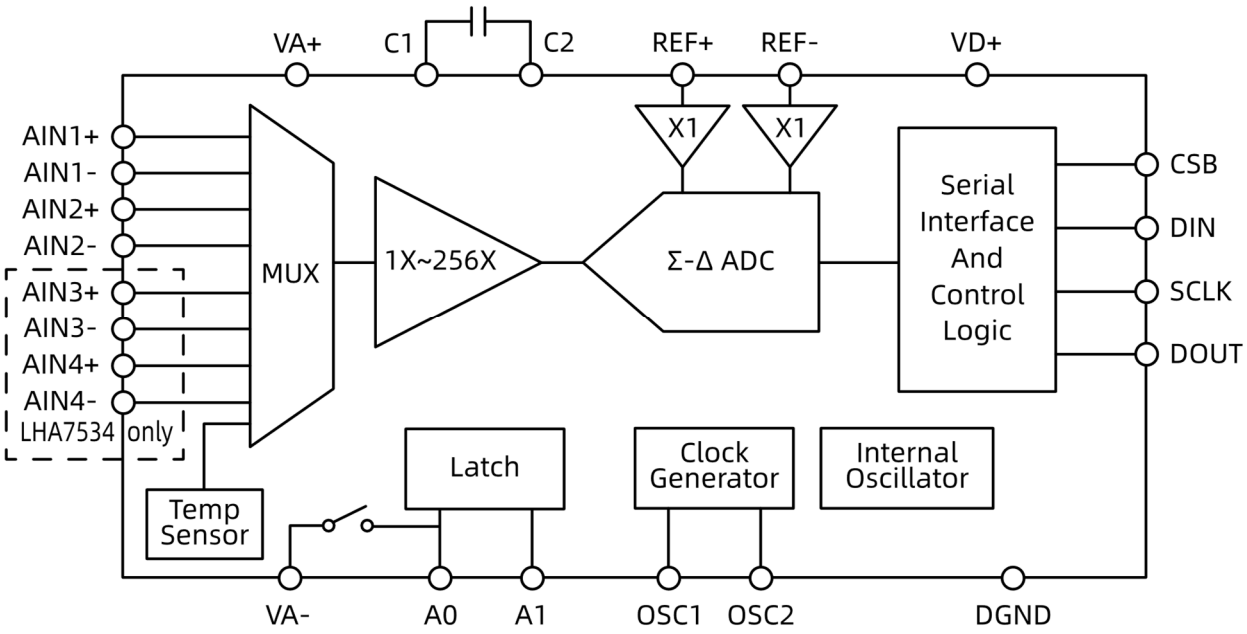
The LHA7532 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 24-bit performance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADCs come as either two-channel or four-channel devices and include a very low-noise, chopper-stabilized instrumentation amplifier (6 nV/√Hz @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, 64×, 128x and 256x. These ADCs also include a fourth-order ΔΣ modulator followed by a digital filter which provides selectable output rates of from 5 SPS to 76.8 kSPS (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a microcontroller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt-trigger input on the serial clock (SCLK).

High dynamic range, programmable output rates, and flexible power supply options makes these ADCs ideal solutions for weigh scale and process control applications.

3. BLOCK DIAGRAM



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4. VERSION HISTORY

Version	Date	Remarks
PreA	January 22, 2025	Initial version. Update the typical legend for the noise and update the image reference numbers in the document.
PreB	February 8, 2025	Add noise table of Effective Resolution、Peak-to-Peak noise、Peak-to-Peak Resolution
	April 22, 2025	Added QFN package information and pin description
PreC	April 23, 2025	Add noise of gain 256 and content of tempensor.

5. CHARACTERISTICS AND SPECIFICATIONS

5.1. ANALOG CHARCTERISTICS

(VA+, VD+ = 5 V ±10%; VREF+ = 5 V; VA-, VREF-, DGND = 0 V; MCLK = 4.9152 MHz;
OWR (Output Word Rate) = 60 SPS; Bipolar Mode; Gain = 32)

Table 1.

Parameter		LHA7532			Unit
		Min	Typ	Max	
Accuracy					
Linearity Error	Gain<=32	-	1		ppm/FS
	Gain>32		3		ppm/FS
No Missing Codes		24	-	-	Bits
Offset		-	50/Gain		μV
Offset Drift	(Notes 3 and 4)	-	15/Gain	-	nV/°C
Gain Error		-	0.005		%
Gain Error Drift	Gain<=32	-	0.5	-	ppm/°C
	Gain>32		1.5		ppm/°C
Analog Input					
Common Mode + Signal on AIN+ or AIN-		VA-	-	VA+	V
CVF Current on AIN+ or AIN-		-	8	-	nA
Open Circuit Detect Current			1	-	uA
Common Mode Rejection	DC	-	140	-	dB
	50, 60 Hz	-	125	-	dB
Input Capacitance		-	18	-	pF
Voltage Reference Input					
Range	(VREF+) - (VREF-)	1	2.5	(VA+)-(VA-)	V
CVF Current		-	400	-	nA
Common Mode Rejection	DC	-	120	-	dB
	50, 60 Hz	-	120	-	dB
Input Capacitance			6		pF
Bridge Power-down Switch					
Ron			5		Ω
Allowable Current			30		mA
Internal clock					
Nominal Frequency			4.9152		MHz
Accuracy		-3%		3%	
External clock					
Frequency Range		1	4.9152	5	MHz
Duty cycle		40%		60%	
TEMPERATURE SENSOR					
Accuracy			±2		°C
System Calibration Specifications					
Full-scale Calibration Range	Bipolar/Unipolar Mode	3	-	110	%FS
Offset Calibration Range	Bipolar Mode	-100	-	100	%FS
Offset Calibration Range	Unipolar Mode	-90	-	90	%FS
Power Supplies					

Parameter		LHA7532			Unit
		Min	Typ	Max	
DC Power Supply Currents (Normal Mode)	I_{A+}, I_{A-}	-	2.1		mA
	I_{D+}	-	1.2		mA
Power Consumption	Normal Mode	-	16.5		mW
	Standby	-	1.7	-	mW
	Sleep	-	5	-	μW
Power Supply Rejection	DC Positive Supplies	-	115	-	dB
	DC Negative Supply	-	115	-	dB

1. Applies after system calibration at any temperature within -40 °C to +125 °C.

2. Specifications guaranteed by design, characterization, and/or test. LSB is 24 bits.

3. This specification applies to the device only and does not include any effects by external parasitic thermocouples.

4. Drift over specified temperature range after calibration at power-up at 25 °C.

5.2. TYPICAL NOISE

All the noise data with VREF=2.5V, resolution is higher with VREF=5V.

Table 2. RMS Noise vs. Gain and Output Data Rate (nV)

Data Rate (SPS)	RMS Noise (nV)								
	Gain=256	Gain=128	Gain=64	Gain=32	Gain=16	Gain=8	Gain=4	Gain=2	Gain=1
5	7.12	7.12	7.15	8.28	10.30	14.80	35.98	65.03	134.6
7.5	8.66	8.67	9.02	9.71	12.61	18.37	36.63	66.82	147.5
10	10.40	10.49	10.22	11.27	14.31	22.24	40.56	74.56	156.4
15	12.79	12.59	12.06	13.18	17.29	25.82	45.71	86.21	173.1
30	17.43	17.40	17.79	19.56	24.35	35.31	59.78	120.6	222.6
60	25.10	25.79	25.24	27.20	31.62	47.72	83.62	164.9	323.9
120	35.47	34.72	36.22	36.93	47.25	66.24	115.4	238.9	436.5
240	50.40	50.24	49.83	50.99	61.99	94.46	170.8	317.9	585.7
480	67.93	68.71	68.60	75.92	89.83	127.7	216.7	431.2	852.8
960	96.07	96.22	97.05	103.8	125.5	185.9	305.8	636.6	1250
1920	134.8	133.4	133.6	156.5	172.5	258.5	445.7	789.0	1702
3840	185.4	184.4	180.5	198.9	227.7	322.1	566.4	1048	2169
9600	291.5	297.0	291.5	304.1	384.1	524.7	937.9	1734	3488
19200	456.5	451.3	463.4	473.1	583.1	793.6	1405	2493	5047
38400	877.2	852.8	844.4	882.4	1019	1330	2262	4129	8131
76800	2001	2034	2036	2051.	2192	2882	4394	8288	16402

Table 3. Effective Resolution vs. Gain and Output Data Rate (Bits)

Data Rate (SPS)	Effective Resolution(Bits)								
	Gain=256	Gain=128	Gain=64	Gain=32	Gain=16	Gain=8	Gain=4	Gain=2	Gain=1
5	21.39	22.4	23.4	24.0	24.0	24.0	24.0	24.0	24.0
7.5	21.10	22.1	23.0	23.9	24.0	24.0	24.0	24.0	24.0

Data Rate (SPS)	Effective Resolution(Bits)								
	Gain=256	Gain=128	Gain=64	Gain=32	Gain=16	Gain=8	Gain=4	Gain=2	Gain=1
10	20.84	21.8	22.9	23.7	24.0	24.0	24.0	24.0	24.0
15	20.54	21.6	22.6	23.5	24.0	24.0	24.0	24.0	24.0
30	20.10	21.1	22.1	22.9	23.6	24.0	24.0	24.0	24.0
60	19.57	20.5	21.6	22.5	23.2	23.6	23.8	23.9	23.9
120	19.07	20.1	21.0	22.0	22.7	23.2	23.4	23.3	23.4
240	18.56	19.6	20.6	21.5	22.3	22.7	22.8	22.9	23.0
480	18.13	19.1	20.1	21.0	21.7	22.2	22.5	22.5	22.5
960	17.63	18.6	19.6	20.5	21.2	21.7	22.0	21.9	21.9
1920	17.14	18.2	19.2	19.9	20.8	21.2	21.4	21.6	21.5
3840	16.68	17.7	18.7	19.6	20.4	20.9	21.1	21.2	21.1
9600	16.03	17.0	18.0	19.0	19.6	20.2	20.3	20.5	20.5
19200	15.38	16.4	17.4	18.3	19.0	19.6	19.8	19.9	19.9
38400	14.44	15.5	16.5	17.4	18.2	18.8	19.1	19.2	19.2
76800	13.25	14.2	15.2	16.3	17.1	17.7	18.1	18.2	18.2

Table 4. Peak-to-Peak Noise vs. Gain and Output Data Rate (nV)

Data Rate (SPS)	RMS Noise (nV)								
	Gain=256	Gain=128	Gain=64	Gain=32	Gain=16	Gain=8	Gain=4	Gain=2	Gain=1
5	48.80	48.89	51.22	55.88	55.88	74.51	149.0	298.0	596.0
7.5	54.72	53.51	55.88	65.19	74.51	111.8	223.5	298.0	596.0
10	68.69	67.52	69.85	74.51	74.51	149.0	223.5	447.0	894.1
15	76.83	86.15	74.51	83.82	93.13	149.0	223.5	596.0	1192
30	101.4	101.8	111.8	111.8	167.6	186.3	372.5	596.0	1192
60	153.5	153.7	177.0	186.3	204.9	260.8	521.5	894.1	1788
120	208.4	223.5	228.2	232.8	316.7	372.5	745.1	1341	2682
240	306.3	307.3	335.3	344.6	391.2	558.8	1043	1788	3874
480	408.6	402.8	409.8	437.7	596.0	819.6	1416	2980	5364
960	600.7	621.7	628.6	670.6	689.2	1378	2086	3874	7451
1920	895.2	847.5	852.2	922.0	1080	1453	2459	5513	12219
3840	1076	1257	1141	1490	1453	1974	3725	7153	13709
9600	1642	1672	1844	1928	2496	3390	6482	11176	21756
19200	2740	2752	2761	3017	3651	5104	10654	19372	36955
38400	5585	5641	6473	5979	7749	9239	22799	36657	63777
76800	11757	12778	13332	13774	13951	17807	27418	62138	100136

Table 5. Peak-to-Peak Resolution vs. Gain and Output Data Rate (Bits)

Data Rate (SPS)	Peak-to-Peak Resolution(Bits)								
	Gain=256	Gain=128	Gain=64	Gain=32	Gain=16	Gain=8	Gain=4	Gain=2	Gain=1
5	18.61	19.61	20.54	21.42	22.42	23.00	23.00	23.00	23.00
7.5	18.45	19.48	20.42	21.19	22.00	22.42	22.42	23.00	23.00
10	18.12	19.14	20.09	21.00	22.00	22.00	22.42	22.42	22.42
15	17.96	18.79	20.00	20.83	21.68	22.00	22.42	22.00	22.00
30	17.56	18.55	19.42	20.42	20.83	21.68	21.68	22.00	22.00
60	16.96	17.96	18.75	19.68	20.54	21.19	21.19	21.42	21.42
120	16.52	17.42	18.39	19.36	19.91	20.68	20.68	20.83	20.83
240	15.96	16.96	17.83	18.79	19.61	20.09	20.19	20.42	20.30
480	15.54	16.57	17.54	18.45	19.00	19.54	19.75	19.68	19.83
960	14.99	15.94	16.92	17.83	18.79	18.79	19.19	19.30	19.36
1920	14.41	15.49	16.48	17.37	18.14	18.71	18.96	18.79	18.64
3840	14.15	14.92	16.06	16.68	17.71	18.27	18.36	18.42	18.48
9600	13.54	14.51	15.37	16.31	16.93	17.49	17.56	17.77	17.81
19200	12.80	13.79	14.79	15.66	16.39	16.90	16.84	16.98	17.05
38400	11.77	12.76	13.56	14.67	15.30	16.05	15.74	16.06	16.26
76800	10.70	11.58	12.52	13.47	14.45	15.10	15.48	15.30	15.61

5.3. 5 V DIGITAL CHARACTERISTICS

(VA+, VD+ = 5 V ±10%; VA-, DGND = 0 V)

Table 6.

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except SCLK	V_{IH}	0.6 VD+	-	VD+	V
	SCLK		(VD+) - 0.45	-	VD+	
Low-level Input Voltage	All Pins Except SCLK	V_{IL}	0.0	-	0.8	V
	SCLK		0.0		0.6	
High-level Output Voltage	A0 and A1, I_{out} = -1.0 mA	V_{OH}	(VA+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0			
Low-level Output Voltage	A0 and A1, I_{out} = 1.0 mA	V_{OL}	-	-	(VA-) + 0.4	V
	SDO, I_{out} = 5.0 mA				0.4	
Input Leakage Current		I_{in}	-	±1	±10	μA
SDO Tri-State Leakage Current		I_{OZ}	-	-	±10	μA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

5.4. 3 V DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+ = 5V ±10%; VD+ = 3.0V±10%; VA-, DGND = 0V)

Table 7.

Parameter		Symbol	Min	Typ	Max	Unit
High-level Input Voltage	All Pins Except SCLK	V_{IH}	0.6 VD+	-	VD+	V
	SCLK		(VD+) - 0.45		VD+	
Low-level Input Voltage	All Pins Except SCLK	V_{IL}	0.0	-	0.8	V

Parameter		Symbol	Min	Typ	Max	Unit
	SCLK		0.0		0.6	
High-level Output Voltage	A0 and A1, I_{out} = -1.0 mA	V_{OH}	(VA+) - 1.0	-	-	V
	SDO, I_{out} = -5.0 mA		(VD+) - 1.0			
Low-level Output Voltage	A0 and A1, I_{out} = 1.0 mA	V_{OL}	-	-	(VA-) + 0.4	V
	SDO, I_{out} = 5.0 mA				0.4	
Input Leakage Current		I_{in}	-	±1	±10	μA
SDO Tri-State Leakage Current		I_{OZ}	-	-	±10	μA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

1. All measurements performed under static conditions.

5.5. DYNAMIC CHARACTERISTICS

Table 8.

Parameter	Symbol	Ratio	Unit
Modulator Sampling Rate	f_s	MCLK/16	SPS
Filter Settling Time to 1/2 LSB (Full Scale Step Input)			
Single Conversion mode	t_s	$1/OWR_{SC}$	s
Continuous Conversion mode, OWR < 3200 SPS	t_s	$5/OWR_{sinc5}$ + 3/OWR	s
Continuous Conversion mode, OWR ⩾ 3200 SPS	t_s	5/OWR	s

1. The ADCs use a $Sinc^5$ filter for the 3200 SPS and 3840 SPS output word rate (OWR) and a $Sinc^5$ filter followed by a $Sinc^3$ filter for the other OWRs. OWR_{sinc5} refers to the 3200 SPS (FRS = 1) or 3840 SPS (FRS = 0) word rate associated with the $Sinc^5$ filter.

2. The single conversion mode only outputs fully settled conversions. See Table 14 for more details about single conversion mode timing. OWR_{SC} is used here to designate the different conversion time associated with single conversions.

3. The continuous conversion mode outputs every conversion. This means that the filter's settling time with a full scale step input in the continuous conversion mode is dictated by the OWR.

5.6. ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V)

Table 9.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 1 and 2)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-3.75	V
Input Current, Any Pin Except Supplies	(Notes 3 and 4)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 5)	PDN	-	-	500	mW
Analog Input Voltage	VREF pins	V_{INR}	(VA-) -0.3	-	(VA+) + 0.3	V
	AIN Pins	V_{INA}	(VA-) -0.3	-	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C

1. All voltages with respect to ground.

2. VA+ and VA- must satisfy {(VA+) - (VA-)} ⩽ +6.6 V.

3. VD+ and VA- must satisfy {(VD+) - (VA-)} ⩽ +7.5 V.

4. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

5. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

6. Total power dissipation, including all input currents and output currents.

5.7. SWITCHING CHARACTERISTICS

(VA+ = 2.5 V or 5 V ±5%; VA- = -2.5V±5% or 0 V; VD+ = 3.0 V ±10% or 5 V ±5%;DGND = 0 V; Levels: Logic 0 = 0 V, Logic 1 = VD+; CL = 50 pF; See Figure 1 and Figure 2.)

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 1)	MCLK				
External Clock or Crystal Oscillator		1	4.9152	5	MHz
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 2)	t_{rise}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times (Note 2)	t_{fall}				
Any Digital Input Except SCLK		-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-up Time XTAL = 4.9152 MHz (Note 3)	t_{ost}	-	20	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
Serial Clock Pulse Width High	t_1	250	-	-	ns
Pulse Width Low	t_2	250	-	-	ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

1. Device parameters are specified with a 4.9152 MHz clock.

2. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

3. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

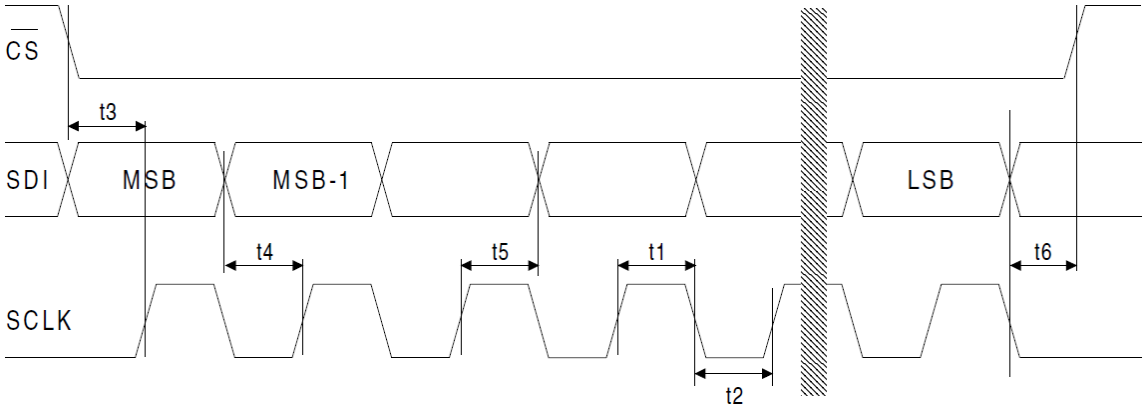


Figure 1. SDI Write Timing (Not to Scale)

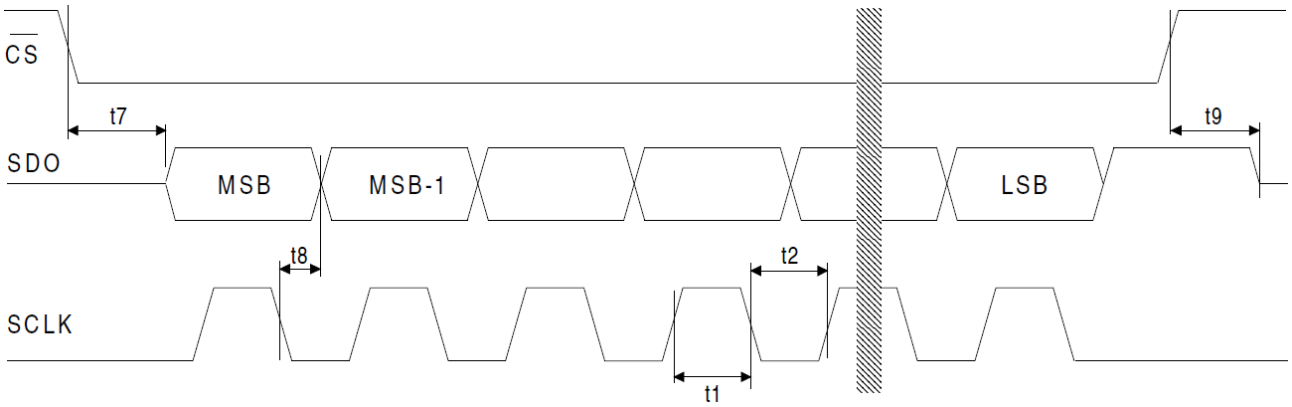


Figure 2. SDO Read Timing (Not to Scale)

5.8. TYPICAL PERFORMANCE CHARACTERISTICS

VA+, VD+ = 5 V; VREF+ = 5 V; VA-, VREF-, DGND = 0 V; MCLK = 4.9152 MHz; T_A = 25°C, unless otherwise noted.

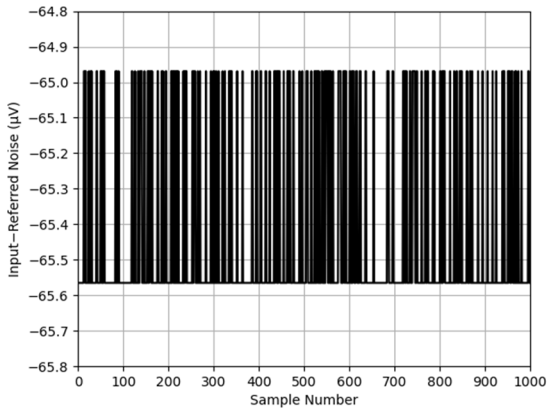


Figure 3. Input-Referred Noise (Output Data Rate = 5 SPS, PGA gain =1)

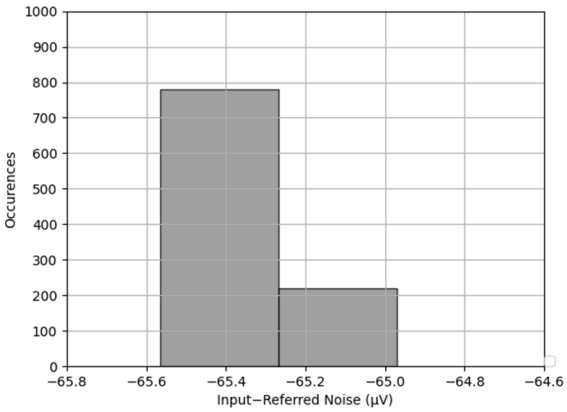


Figure 4. Histogram (Output Data Rate = 5 SPS, PGA gain =1)

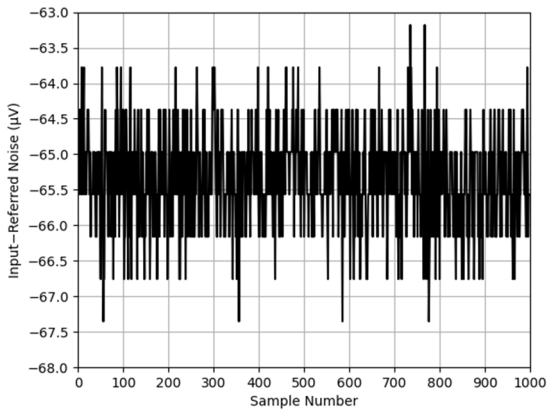


Figure 5. Input-Referred Noise(Output Data Rate = 240 SPS，PGA gain =1)

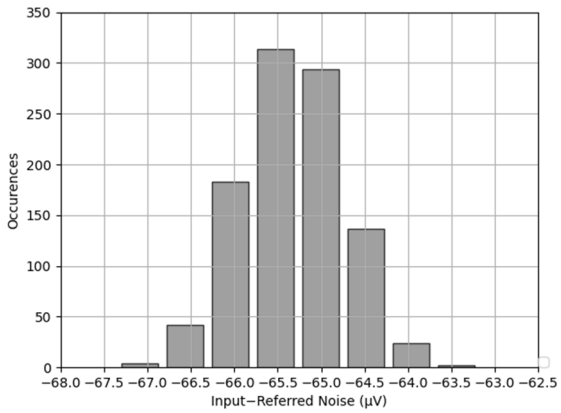


Figure 6. Histogram(Output Data Rate = 240 SPS, PGA gain =1)

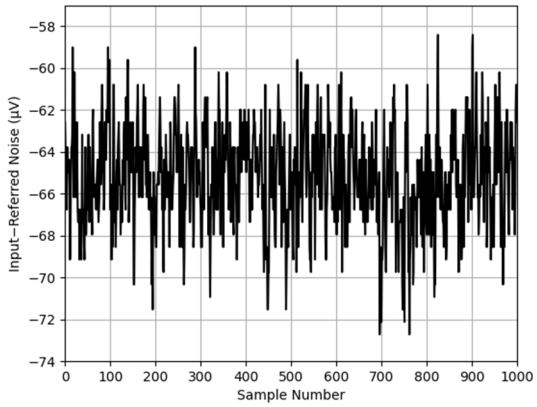


Figure 7. Input-Referred Noise(Output Data Rate = 3840 SPS，PGA gain =1)

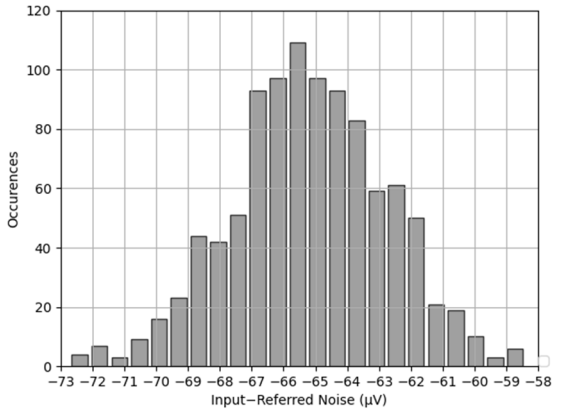


Figure 8. Histogram(Output Data Rate = 3840 SPS，PGA gain =1)

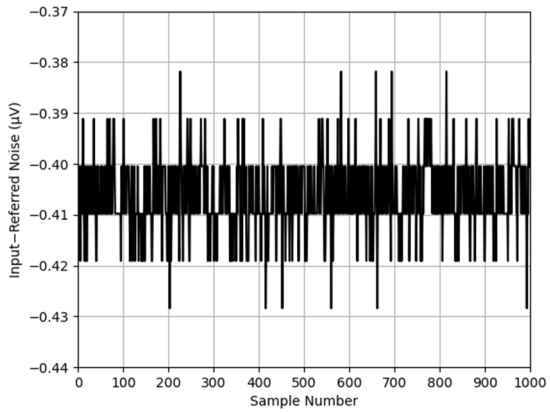


Figure 9. Input-Referred Noise (Output Data Rate = 5 SPS，PGA gain =64)

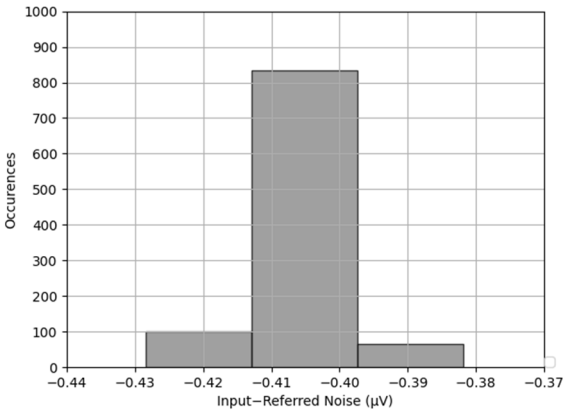


Figure 10. Histogram (Output Data Rate = 5 SPS, PGA gain =64)

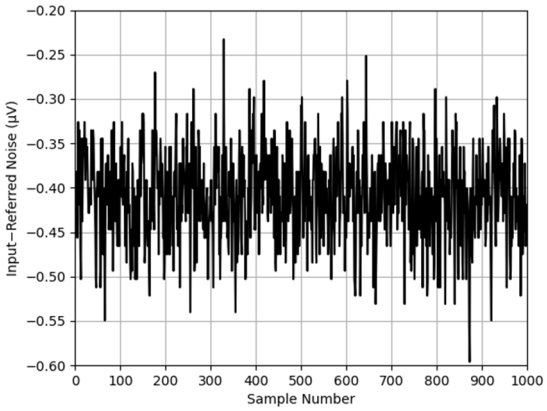


Figure 11. Input-Referred Noise(Output Data Rate = 240 SPS， PGA gain =64)

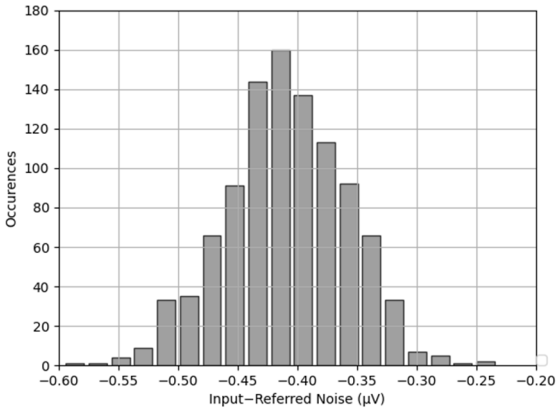


Figure 12. Histogram(Output Data Rate = 240 SPS， PGA gain =64)

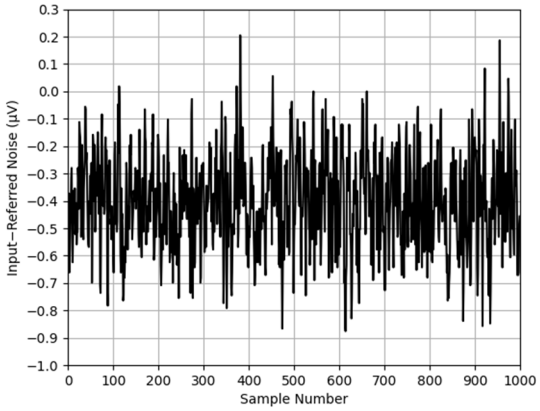


Figure 13. Input-Referred Noise(Output Data Rate = 3840 SPS， PGA gain =64)

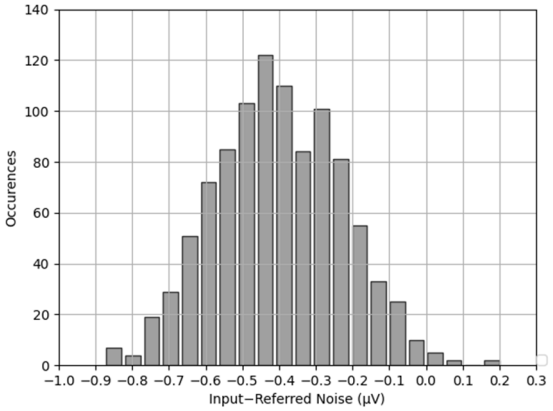


Figure 14. Histogram(Output Data Rate = 3840 SPS， PGA gain =64)

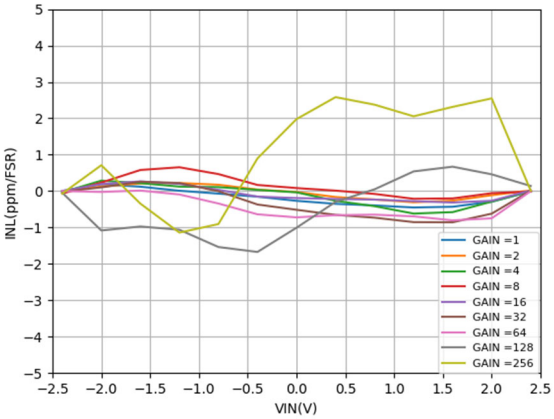


Figure 15. Integral Nonlinearity (INL) vs. VIN (External 2.5 V Reference)

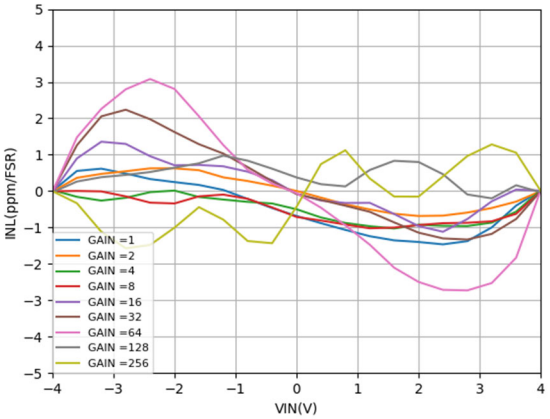


Figure 16. Integral Nonlinearity (INL) vs. VIN (External 5 V Reference)

6. PIN DESCRIPTIONS

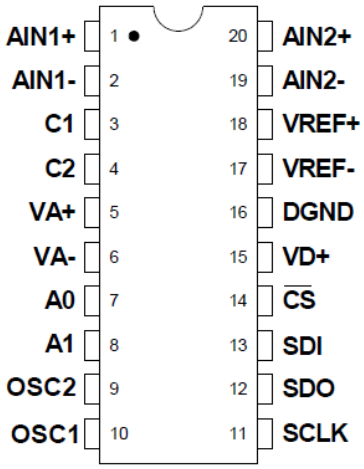


Figure 17. LHA7532

Table 11.

Pin NO.	Pin Name	Function Description
1	AIN1+	Positive analog input
2	AIN1-	Negative analog input
3	C1	Put >=100nF CERAMIC Cap connection to C2,
4	C2	Put >=100nF CERAMIC Cap connection to C1
5	VA+	Analog positive supply
6	VA-	Analog negative supply
7	A0	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+. An internal switch connect to VA- via A0 can be configured for some sensor to save power.
8	A1	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+.
9	OSC2	XTAL pin, external clock can be applied to this pin
10	OSC1	XTAL pin
11	SCLK	A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
12	SDO	Serial Data Output. SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1
13	SDI	Serial Data Input. SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK
14	$\overline{CS}$	Chip Select. When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{CS}$ should be changed when SCLK = 0.
15	VD+	Digital supply
16	DGND	Digital ground
17	VREF-	Negative reference input
18	VREF+	Positive reference input
19	AIN2-	Negative analog input
20	AIN2+	Positive analog input

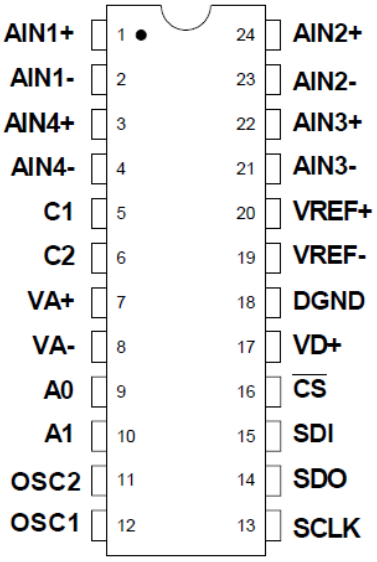


Figure 18. LHA7534 SS0P24

Table 12.

Pin NO.	Pin Name	Function Description
1	AIN1+	Positive analog input
2	AIN1-	Negative analog input
3	AIN4+	Positive analog input
4	AIN4-	Negative analog input
5	C1	Put >=100nF CERAMIC Cap connection to C2,
6	C2	Put >=100nF CERAMIC Cap connection to C1
7	VA+	Analog positive supply
8	VA-	Analog negative supply
9	A0	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+. An internal switch connect to VA- via A0 can be configured for some sensor to save power.
10	A1	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+.
11	OSC2	XTAL pin, external clock can be applied to this pin
12	OSC1	XTAL pin
13	SCLK	A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
14	SDO	Serial Data Output. SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1
15	SDI	Serial Data Input. SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK
16	$\overline{CS}$	Chip Select. When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{CS}$ should be changed when SCLK = 0.
17	VD+	Digital supply
18	DGND	Digital ground
19	VREF-	Negative reference input
20	VREF+	Positive reference input
21	AIN3-	Negative analog input
22	AIN3+	Positive analog input
23	AIN2-	Negative analog input
24	AIN2+	Positive analog input

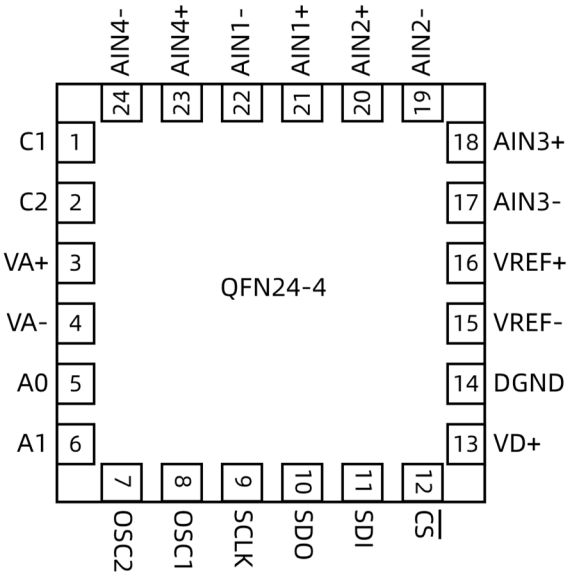


Figure 19. LHA7534 QFN24

Table 13.

Pin NO.	Pin Name	Function Description
1	C1	Put >=100nF CERAMIC Cap connection to C2,
2	C2	Put >=100nF CERAMIC Cap connection to C1
3	VA+	Analog positive supply
4	VA-	Analog negative supply
5	A0	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+. An internal switch connect to VA- via A0 can be configured for some sensor to save power.
6	A1	Logic Output (Analog). Logic Output 0 = VA-, and Logic Output 1 = VA+.
7	OSC2	XTAL pin, external clock can be applied to this pin
8	OSC1	XTAL pin
9	SCLK	A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
10	SDO	Serial Data Output. SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1
11	SDI	Serial Data Input. SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK
12	$\overline{CS}$	Chip Select. When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{CS}$ should be changed when SCLK = 0.
13	VD+	Digital supply
14	DGND	Digital ground
15	VREF-	Negative reference input
16	VREF+	Positive reference input
17	AIN3-	Negative analog input
18	AIN3+	Positive analog input
19	AIN2-	Negative analog input
20	AIN2+	Positive analog input
21	AIN1+	Positive analog input
22	AIN1-	Negative analog input
23	AIN4+	Positive analog input
24	AIN4-	Negative analog input

7. GENERAL DESCRIPTION

The LHA7532 are highly integrated ΔΣ Analog to-Digital Converters (ADCs) which use charge balance techniques to achieve 24-Bitperformance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADCs come as either two-channel (LHA7532) or four-channel (LHA7534) devices and include a very-low-noise, chopper-stabilized, programmable-gain amplifier (PGA, 6 nV/$\sqrt{\text{Hz}}$ @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, 64×, 128x and 256x. These ADCs also include a fourth-order ΔΣ modulator followed by a digital filter which provides twenty selectable output word rates of 5, 6.25, 7.5, 10, 12.5, 15, 25, 30, 50, 60, 100, 120, 200, 240, 400, 480, 800, 960, 1600, 1920, 3200, 3840, 9600, 19200, 38400 and 76800 Samples per second (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a microcontroller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt-trigger input on the serial clock (SCLK).

7.1. Analog Input

Figure 20 illustrates a block diagram of the LHA7532. The front end consists of a multiplexer and a programmable-gain, chopper-stabilized instrumentation amplifier. And the reference inputs are buffer with two unity gain buffers.

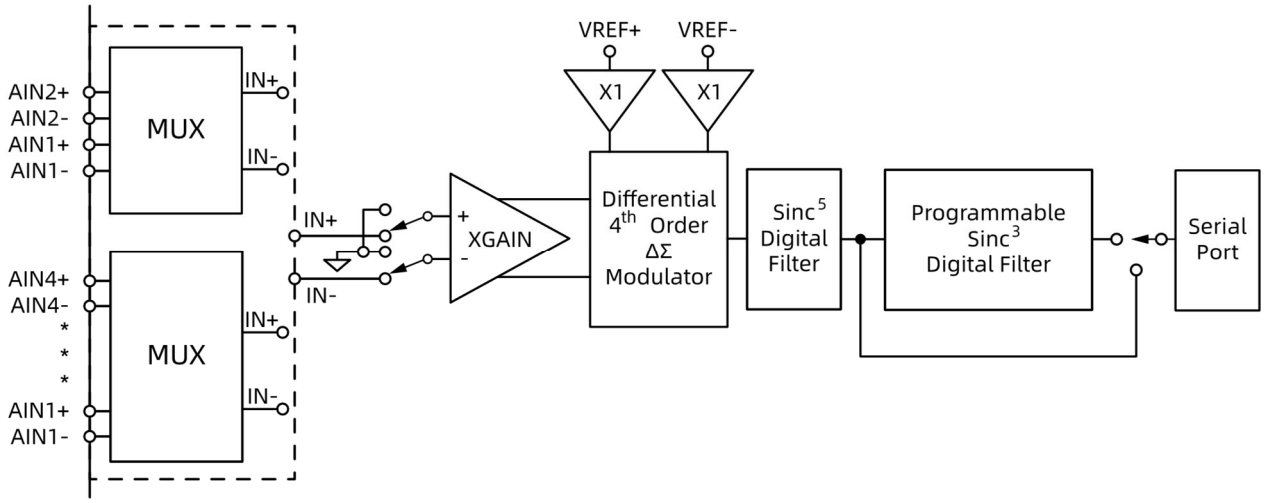


Figure 20. Multiplexer Configuration

Analog Input Span

The full-scale input signal that the converter can digitize is a function of the gain setting and the reference voltage connected between the VREF+ and VREF- pins. The full-scale input span of the converter is ((VREF+) - (VREF-))/(GxA), where G is the gain of the amplifier and A is 2 for VRS = 0, or A is 1 for VRS = 1. VRS is the Voltage Range Select bit, can get extra 2x gain if needed.

Note, if the reference is 5V and VRS =1, the input range is ±5V/Gain. While it may not achieve real 5V if supply voltage is also 5V. To guarantee performance, it's suggested to limit the input voltage range to ±((VA+ - VA-)-0.3V)/Gain.

7.2. Overview of ADC Register Structure and Operating Modes

The LHA7532 ADCs have an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 21 depicts a block diagram of the on-chip controller's internal registers.

Each of the converters has 32-bit registers to function as offset and gain calibration registers for each channel.

The LHA7532 has two offset and two gain calibration registers, the LHA7534 has four offset and four gain calibration registers. These registers hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converters include a 32-bit configuration register which is used for setting options such as the power down modes, resetting the converter, shorting the analog inputs, and enabling diagnostic test bits like the guard signal.

A group of registers, called Channel Setup Registers, are used to hold pre-loaded conversion instructions. Each channel setup register is 32 bits wide, and holds two 16-bit conversion instructions referred to as Setups. Upon power up, these registers can be initialized by the system microcontroller with conversion instructions. The user can then instruct the converter to perform single or multiple conversions or calibrations with the converter in the mode defined by one of these Setups.

Using the single conversion mode, an 8-bit command word can be written into the serial port. The command includes pointer bits which 'point' to a 16-bit command in one of the Channel Setup Registers which is to be executed. The 16-bit Setups can be programmed to perform a conversion on any of the input channels of the converter. More than one of the 16-bit Setups can be used for the same analog input channel. This allows the user to convert on the same signal with either a different conversion speed, a different gain range, or any of the other options available in the channel setup registers. Alternately, the user can set up the registers to perform different conversion conditions on each of the input channels.

The ADCs also include continuous conversion capability. The ADCs can be instructed to continuously convert, referencing one 16-bit command Setup. In the continuous conversion mode, the conversion data words are loaded into a shift register. The converter issues a flag on the SDO pin when a conversion cycle is completed so the user can read the register, if need be. See "Performing Conversions" section for more details.

The following pages document how to initialize the converter, perform offset and gain calibrations, and how to configure the converter for the various conversion modes. Each of the bits of the configuration register and of the Channel Setup Registers is described. A list of examples follows the description section. Also the Command Register Quick Reference can be used to decode all valid commands (the first 8 bits into the serial port).

System Initialization

The LHA7532 provide power-on-reset function. The user can also perform a software reset by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting at least 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Note that this sequence can be initiated at anytime to reinitialize the serial port. To complete the system initialization sequence, the user must also perform a system reset sequence which is as follows: Write a logic 1 into the RS bit of the configuration register. This will reset the calibration registers and other logic (but not the serial port). A valid reset will set the RV bit in the configuration register to a logic 1. After writing the RS bit to a logic 1, wait 20 microseconds, then write the RS bit back to logic 0. While this involves writing an entire word into the configuration register, the RV bit is a read-only bit, therefore a write to the configuration register will not overwrite the RV bit. After clearing the RS bit back to logic 0, read the configuration register to check the state of the RV bit as this indicates that a valid reset occurred. Reading the configuration register clears the RV bit back to logic 0.

Completing the reset cycle initializes the on-chip registers to the following states:

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

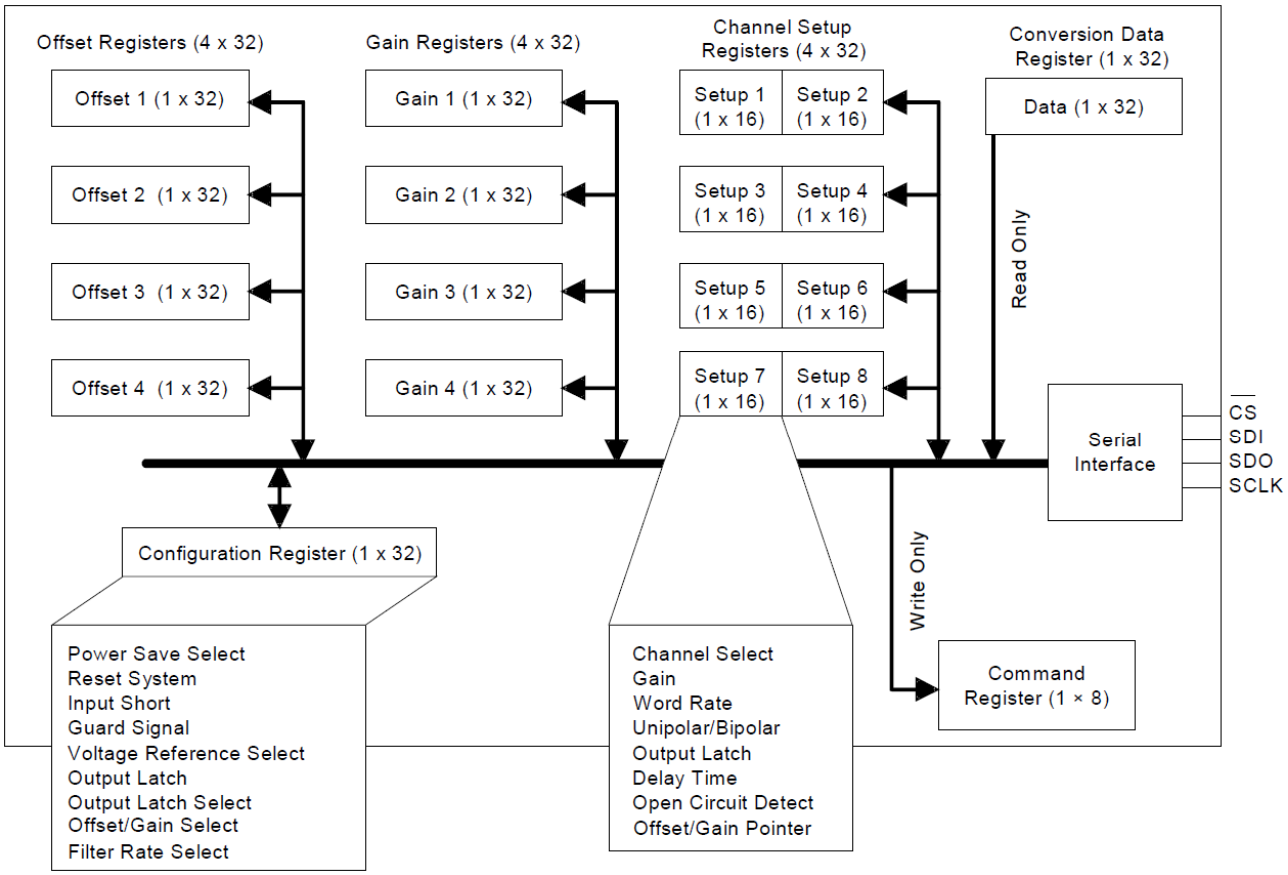


Figure 21. LHA7532 Register Diagram

The RV bit in the Configuration Register is set to indicate a valid reset has occurred. The RS bit should be written back to logic 0 to complete the reset cycle. After a system initialization or reset, the on-chip controller is initialized into command mode where it waits for a valid command (the first 8 bits written into the serial port are shifted into the command register). Once a valid command is received and decoded, the byte instructs the converter to either acquire data from or transfer data to an internal register(s), or perform a conversion or a calibration. The Command Register Descriptions section can be used to decode all valid commands.

Command Register Quick Reference

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/W	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as	0	Ignore this function.
	Arrays, ARA	1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00 01 10 11	CS1-CS0 provide the address of one of the two (four for LHA7532) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
D3	Read/$\overline{\text{Write}}$, R/$\overline{\text{W}}$	0	Write to selected register.

		1	Read from selected register.
D2-D0	Register Select Bit,	000	Reserved
	RSB3-RSB0	001	Offset Register
		010	Gain Register
		011	Configuration Register
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conver-	0	Perform fully settled single conversions.
	sions, MC	1	Perform conversions continuously.
D5-D3	Channel-Setup Reg-	000	These bits are used as pointers to the channel-setup registers. Either a single con-
	ister Pointer Bits,	...	version or continuous conversions are performed on the channel setup register
	CSRP	111	pointed to by these bits.
D2-D0	Conversion/Calibra-	000	Normal Conversion
	tion Bits, CC2-CC0	001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

Command Register Descriptions

READ/$\overline{\text{WRITE}}$ ALL OFFSET CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{\text{W}}$	0	0	1

Function: These commands are used to access the offset registers as arrays.

R/$\overline{\text{W}}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ ALL GAIN CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{\text{W}}$	0	1	0

Function: These commands are used to access the gain registers as arrays.

R/$\overline{\text{W}}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ ALL CHANNEL-SETUP REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	1	0	1

Function: These commands are used to access the channel-setup registers as arrays.

R/$\overline{W}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected registers.

1 Read from selected registers.

READ/$\overline{\text{WRITE}}$ INDIVIDUAL OFFSET REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	0	0	1

Function: These commands are used to access each offset register separately. CS1 - CS0 decode the registers accessed.

R/$\overline{W}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Offset Register 1

01 Offset Register 2

10 Offset Register 3 (LHA7534 only)

11 Offset Register 4 (LHA7534 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL GAIN REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	0	1	0

Function: These commands are used to access each gain register separately. CS1 - CS0 decode the registers accessed.

R/$\overline{W}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Offset Register 1

01 Offset Register 2

10 Offset Register 3 (LHA7534 only)

11 Offset Register 4 (LHA7534 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL CHANNEL-SETUP REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	1	0	1

Function: These commands are used to access each channel-setup register separately. CS1 - CS0 decode the registers accessed.

R/$\overline{W}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Channel-Setup Register 1

01 Channel-Setup Register 2

10 Channel-Setup Register 3

11 Channel-Setup Register 4

READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{\text{W}}$	0	1	1

Function: These commands are used to read from or write to the configuration register.

R/$\overline{\text{W}}$ (Read/$\overline{\text{WRITE}}$)

0 Write to selected register.

1 Read from selected register.

PERFORM CONVERSION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	0	0	0

Function: These commands instruct the ADC to perform either a single, fully-settled conversion or continuous conversions on the physical input channel pointed to by the pointer bits (CSRP2 - CRSP0) in the channel-setup register.

MC (Multiple Conversions)

0 Perform a single conversion.

1 Perform continuous conversions.

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1

001 Setup 2

010 Setup 3

011 Setup 4

100 Setup 5

101 Setup 6

110 Setup 7

111 Setup 8

PERFORM CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	0	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

Function: These commands instruct the ADC to perform a calibration on the physical input channel selected by the setup register which is chosen by the command byte pointer bits (CSRP2 - CSRP0).

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1

001 Setup 2

010 Setup 3

011 Setup 4

100 Setup 5

101 Setup 6

110 Setup 7

111 Setup 8

CC [2:0] (Calibration Control Bits)

0 Reserved

1 Self-Offset Calibration

10 Self-Gain Calibration

11 Reserved

100 Reserved

101 System-Offset Calibration

110 System-Gain Calibration

111 Reserved

SYNC1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Function: Part of the serial port re-initialization sequence.

SYNC0

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

Function: End of the serial port re-initialization sequence.

NULL

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Function: This command is used to clear a port flag and keep the converter in the continuous conversion mode.

Serial Port Interface

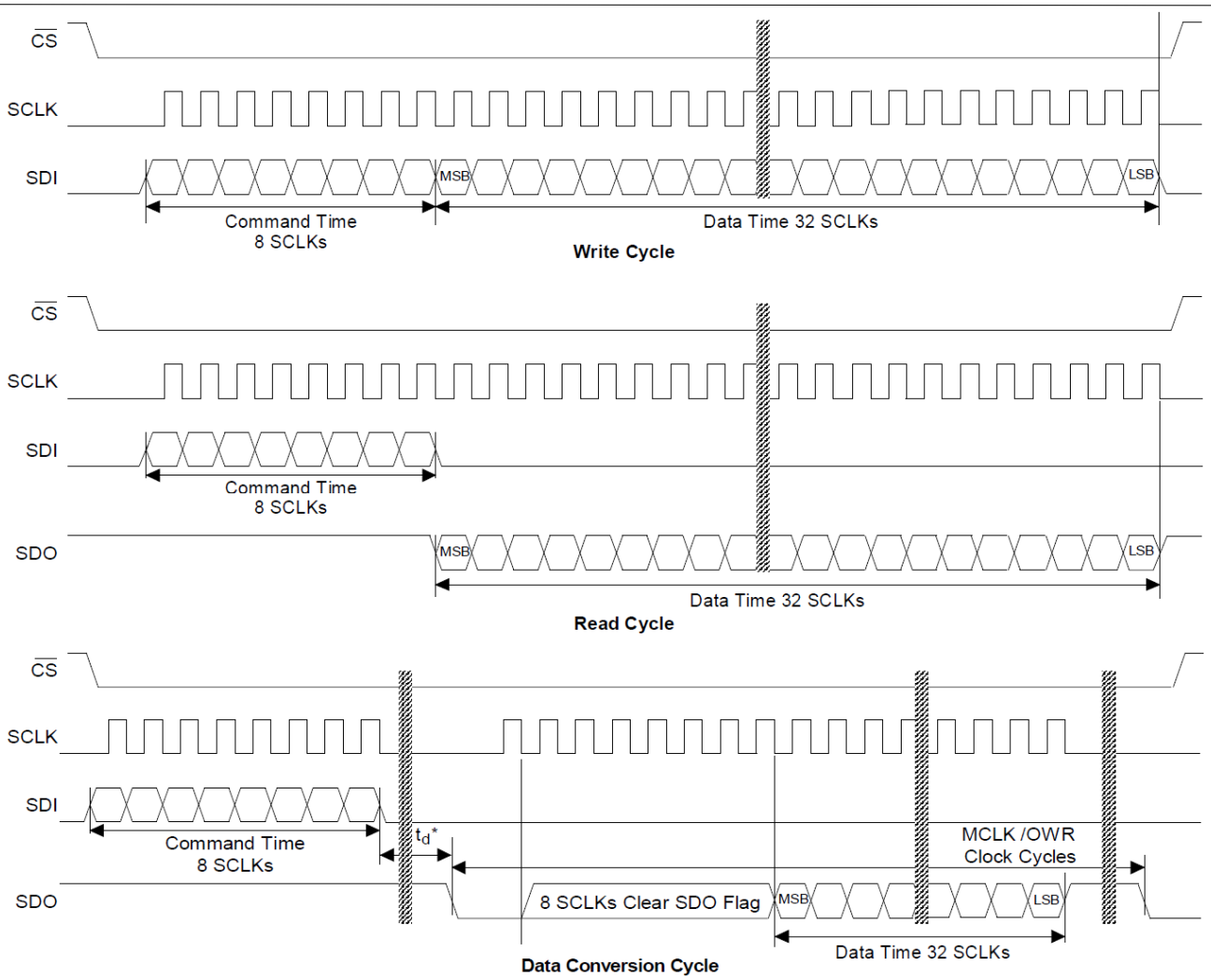
The LHA7532's serial interface consists of four control lines: CS, SDI, SDO, SCLK. Figure 22 details the command and data word timing.

CS, Chip Select, is the control line which enables access to the serial port. If the CS pin is tied low, the port can function as a three wire interface.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time CS is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The CS pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate optoisolators SCLK is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.



* td is the time it takes the ADC to perform a conversion. See the Single Conversion and Continuous Conversion sections of the data sheet for more details about conversion timing.

Figure 22. Command and Data Word Timing

Reading/Writing On-Chip Registers

The LHA7532's offset, gain, configuration, and channel-setup registers are readable and writable while the conversion data register is read only.

As shown in Figure 22, to write to a particular register the user must transmit the appropriate write command and then follow that command by 32 bits of data. For example, to write 0x80000000 (hexadecimal) to physical channel one's gain register, the user would first transmit the command byte 0x02 (hexadecimal) followed by the data 0x80000000 (hexadecimal). Similarly, to read a particular register the user must transmit the appropriate read command and then acquire the 32 bits of data. Once a register is written to or read from, the serial port returns to the command mode.

In addition to accessing the internal registers one at a time, the gain and offset registers as well as the channel setup registers can be accessed as arrays (i.e. the entire register set can be accessed with one command). In the LHA7532, there are two gain and offset registers, and in the LHA7534, there are four gain and offset registers. There are four channel setup registers in both devices. As an example, to write 0x80000000 (hexadecimal) to all four gain registers in the LHA7534, the user would transmit the command 0x42 (hexadecimal) followed by four iterations of 0x80000000 (hexadecimal), (i.e. 0x42 followed by 0x80000000, 0x80000000, 0x80000000, 0x80000000). The registers are written to or read from in sequential order (i.e, 1, followed by 2, 3, and 4). Once the registers are written to or read from, the serial port returns to the command mode.

7.3. Configuration Register

To ease the architectural design and simplify the serial interface, the configuration register is thirty two bits long,

however, only eleven of the thirty two bits are used. The following sections detail the bits in the configuration register.

Power Consumption

The LHA7532 accommodate three power consumption modes: normal, standby, and sleep. The default mode, “normal mode”, is entered after power is applied., The other two modes are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the power down (PDW) bit of the configuration register is set to logic 1. The particular power save mode entered depends on state of the PSS (Power Save Select) bit. If PSS is logic 0, the converter enters the standby mode reducing the power consumption to 4 mW. The standby mode leaves the oscillator and the onchip bias generator for the analog portion of the chip active. This allows the converter to quickly return to the normal mode once PDW is set back to a logic 1. If PSS and PDW are both set to logic 1, the sleep mode is entered reducing the consumed power to around 10 μW. Since this sleep mode disables the oscillator, approximately a 20 ms oscillator start-up delay period is required before returning to the normal mode. If an external clock is used, there will be no delay. Further note that when the chips are used in the Gain = 1 mode, the PGIA is powered down. With the PGIA powered down, the power consumed in the normal power mode is reduced by approximately 1/2. Power consumption in the sleep and standby modes is not affected by the amplifier setting.

System Reset Sequence

The reset system (RS) bit permits the user to perform a system reset. A system reset can be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After the RS bit has been set, the internal logic of the chip will be initialized to a reset state. The reset valid (RV) bit is set indicating that the internal logic was properly reset. The RV bit is cleared after the configuration register is read. The on-chip registers are initialized to the following default states:

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

After reset, the RS bit should be written back to logic 0 to complete the reset cycle. The ADC will return to the command mode where it waits for a valid command. Also, the RS bit is the only bit in the configuration register that can be set when initiating a reset (i.e. a second write command is needed to set other bits in the Configuration Register after the RS bit has been cleared).

Input Short

The input short bit allows the user to internally ground all the inputs of the multiplexer. This is a useful function because it allows the user to easily test the grounded input performance of the ADC and eliminate the noise effects due to the external system components.

Voltage Range Select

The Voltage Range Select (VRS) bit can select 2x extra gain. For example, PGA gain=128 set by register, if VRS=0, the gain will be 128 x 2 = 256.

Output Latch Pins

The A1-A0 pins of the ADCs mimic the D21-D20/D5-D4 bits of the channel-setup registers if the output latch select (OLS) bit is logic 0 (default). If the OLS bit is logic 1, A1-A0 mimic the output latch bit settings in the configuration register. These two options give the user a choice of allowing the latch outputs to change anytime a different CSR is selected for a conversion, or to allow the latch bits to remain latched to a fixed state (determined

by the configuration register bit) for all CSR selections. In either case, A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The A1-A0 outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 μA to reduce self-heating of the chip. These outputs are powered from VA+ and VA-. Their output voltage will be limited to the VA+ voltage for a logic 1 and VA-for a logic 0.

Offset and Gain Select

The Offset and Gain Select bit (OGS) is used to select the source of the calibration registers to use when performing conversions and calibrations. When the OGS bit is set to '0', the offset and gain registers corresponding to the desired physical channel (CS1-CS0 in the selected Setup) will be accessed. When the OGS bit is set to '1', the offset and gain registers pointed to by the OG1-OG0 bits in the selected Setup will be accessed. This feature allows multiple calibration values (e.g. for different gain settings) to be used on a single physical channel without having to re-calibrate or manipulate the calibration registers.

Filter Rate Select

The Filter Rate Select bit (FRS) modifies the output word rates of the converter to allow either 50 Hz or 60 Hz rejection when operating from a 4.9152 MHz crystal. If FRS is cleared to logic 0, the word rates and corresponding filter characteristics can be selected (using the Channel Setup Registers) from 7.5, 15, 30, 60, 120, 240, 480, 960, 1920, or 3840 SPS when using a 4.9152 MHz clock. If FRS is set to logic 1, the word rates and corresponding filter characteristics scale by a factor of 5/6, making the selectable word rates 6.25, 12.5, 25, 50, 100, 200, 400, 800, 1600, and 3200 SPS when using a 4.9152 MHz clock. When using other clock frequencies, these selectable word rates will scale linearly with the clock frequency that is used.

Configuration Register Descriptions

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
PSS	PDW	RS	RV	IS	GB	VRS	A1	A0	OLS	NU	FRS	FRS	TEMP_SEL	NU	NU
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU

PSS (Power Save Select)[31]

0 Standby Mode (Oscillator active, allows quick power-up).

1 Sleep Mode (Oscillator inactive).

PDW (Power Down Mode)[30]

0 Normal Mode

1 Activate the power save select mode.

RS (Reset System)[29]

0 Normal Operation.

1 Activate a Reset cycle. See System Reset Sequence in the datasheet text.

RV (Reset Valid)[28]

0 Normal Operation

1 System was reset. This bit is read only. Bit is cleared to logic zero after the configuration register is read.

IS (Input Short)[27]

0 Normal Input

1 All signal input pairs for each channel are disconnected from the pins and shorted internally.

GB (Guard Signal Bit)[26]

0 Normal Operation of A0 as an output latch.

1 A0's output is modified to output the common mode output voltage of the instrumentation amplifier (typically 2.5 V). The output latch select bit is ignored when the guard buffer is activated.

VRS (Voltage Range Select) [25]

0 2x extra Gain

1 1x Gain

A1-A0 (Output Latch bits) [24:23]

The latch bits (A0 and A1) will be set to the logic state of these bits upon command word execution if the output latch select bit (OLS) is set. Note that these logic outputs are powered from VA+ and VA-.

00 A0=0, A1=0

01 A0=0, A1=1

10 A0=1, A1=0

11 A0=1, A1=1

Output Latch Select, OLS[22]

0 When low, uses the Channel-Setup Register as the source of A1 and A0.

1 When set, uses the Configuration Register as the source of A1 and A0.

NU (Not Used)[21]

0 Must always be logic 0. Reserved for future upgrades.

Offset and Gain Select OGS[20]

0 Calibration registers used are based on the CS1-CS0 bits of the referenced Setup.

1 Calibration registers used are based on the OG1-OG0 bits of the referenced Setup.

Filter Rate Select, FRS[19]

0 Use the default output word rates.

1 Scale all output word rates and their corresponding filter characteristics by a factor of 5/6.

Temp Channel Select, TEMP_SEL [19]

0 Select the channel by the setup register.

1 Select the Temp channel， no care the setup register CS bits.

NU (Not Used)[17:0]

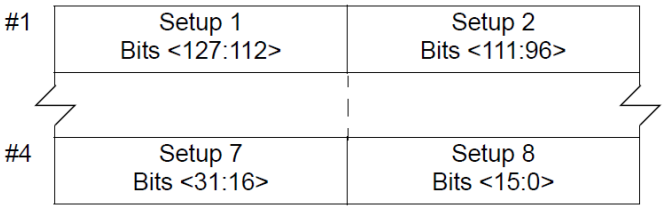
0 Must always be logic 0. Reserved for future upgrades.

7.4. Setting up the CSRs for a Measurement

The LHA7532 have four Channel-Setup Registers (CSRs). Each CSR contains two 16-bit Setups which are programmed by the user to contain data conversion information such as: 1) which physical channel will be converted, 2) at what gain will the channel be converted, 3) at what word rate will the channel be converted, 4) will the output conversion be unipolar or bipolar, 5) what will be the state of the output latch during the conversion, 6) will the converter delay the start of a conversion to allow time for the output latch to settle before the conversion is begun, and 7) will the open circuit detect current source be activated for that Setup. In addition, when the OGS bit in the Configuration Register is set, the Setup selects which set of offset and gain registers to use when performing conversions or calibrations. Note that a particular physical input channel can be represented in more than one Setup with different output rates, gain ranges, etc. (i.e. each Setup is independently defined). Refer to section 2.4.1 for more details about the Channel Setup Registers. Each 32-bit CSR is individually accessible and contains two 16-bit Setups. As an example, to configure Setup 1 in the LHA7532 with the write individual channel-setup register command (0x05 hexadecimal), bits 31 to 16 of CSR 1 contains the information for Setup 1 and bits 15 to 0 contain the information for Setup 2. Note that while reading/writing CSRs, two Setups are accessed in pairs as a single 32-bit CSR register. Even if one of the Setups isn't used, it must be written to or read.

Channel-Setup Register Descriptions

CSR



D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
CS1	CS0	G2	G1	G0	WR3	WR2	WR1	WR0	U/B	OL1	OL0	DT	OCD	OG1	OG0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CS1	CS0	G2	G1	G0	WR3	WR2	WR1	WR0	U/B	OL1	OL0	DT	OCD	OG1	OG0

CS1-CS0 (Channel Select Bits) [31:30] [15:14]

00	Select physical channel 1
01	Select physical channel 2
10	Select physical channel 3 (LHA7532 only)
11	Select physical channel 4 (LHA7532 only)

G2-G0 (Gain Bits) [29:27] [13:11]

For VRS = 0, A = 2; For VRS = 1, A = 1; Bipolar input span is twice the unipolar input span.

0	Gain = 1, (Input Span = [(VREF+)-(VREF-)]/1*A for unipolar).
1	Gain = 2, (Input Span = [(VREF+)-(VREF-)]/2*A for unipolar).
10	Gain = 4, (Input Span = [(VREF+)-(VREF-)]/4*A for unipolar).
11	Gain = 8, (Input Span = [(VREF+)-(VREF-)]/8*A for unipolar).
100	Gain = 16, (Input Span = [(VREF+)-(VREF-)]/16*A for unipolar).
101	Gain = 32, (Input Span = [(VREF+)-(VREF-)]/32*A for unipolar).
110	Gain = 64, (Input Span = [(VREF+)-(VREF-)]/64*A for unipolar).
111	Gain = 128, (Input Span = [(VREF+)-(VREF-)]/128*A for unipolar).

WR3-WR0 (Word Rate) [26:23] [10:7]

The listed Word Rates are for continuous conversion mode using a 4.9152 MHz clock. All word rates will scale linearly with the clock frequency used. The very first conversion using continuous conversion mode will last longer, as will conversions done with the single conversion mode.

Bit	WR (FRS = 0)	WR (FRS = 1)
0000	120 SPS	100 SPS
0001	60 SPS	50 SPS
0010	30 SPS	25 SPS
0011	15 SPS	12.5 SPS
0101	10 SPS	10 SPS
0110	5 SPS	5 SPS
0111	9600 SPS	9600 SPS
1000	3840 SPS	3200 SPS
1001	1920 SPS	1600 SPS
1010	960 SPS	800 SPS
1011	480 SPS	400 SPS
1100	240 SPS	200 SPS
1101	19200 SPS	19200 SPS

1110	38400 SPS	38400 SPS
1111	76800 SPS	76800 SPS

U/$\overline{B}$ (Unipolar / $\overline{\text{Bipolar}}$) [22] [6]

0	Select Bipolar mode.
1	Select Unipolar mode.

OL1-OL0 (Output Latch Bits) [21:20] [5:4]

The latch bits will be set to the logic state of these bits upon command word execution when the output latch select bit (OLS) in the configuration register is logic 0. Note that the logic outputs on the chip are powered from VA+ and VA-.

00	A0=0, A1=0
01	A0=0, A1=1
10	A0=1, A1=0
11	A0=1, A1=1

DT (Delay Time Bit) [19] [3]

When set, the converter will wait for a delay time before starting a conversion. This allows settling time for A0 and A1 outputs before a conversion begins. The delay time will be 1280 MCLK cycles when FRS = 0, and 1536 MCLK cycles when FRS = 1.

0	Begin Conversions Immediately.
1	Wait 1280 MCLK cycles (FRS = 0) or 1536 MCLK cycles (FRS = 1) before starting conversion.

OCD (Open Circuit Detect Bit) [18] [2]

When set, this bit activates a 1 μA current source on the input channel (AIN+) selected by the channel select bits.

0	Normal mode.
1	Activate current source.

OG1-OG0 (Offset / Gain Register Pointer Bits) [17:16] [1:0]

These bits are only used when OGS in the Configuration Register is set to '1'. They allow the user to select the offset and gain register to use while performing a conversion or calibration. When the OGS bit in the Configuration Register is set to '0', the offset and gain register for the referenced physical channel (CS1-CS0 bits of the Setup) will be used.

00	Use offset and gain register from physical channel 1
01	Use offset and gain register from physical channel 2
10	Use offset and gain register from physical channel 3
11	Use offset and gain register from physical channel 4

7.5. Calibration

Calibration is used to set the zero and gain slope of the ADC's transfer function. The LHA7532 offer both self calibration and system calibration.

Note: After the ADCs are reset, they are functional and can perform measurements without being calibrated (remember that the VRS bit in the configuration register must be properly configured). In this case, the converter will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words. Any initial offset and gain errors in the internal circuitry of the chip will remain.

Calibration Registers

The LHA7532 converters have an individual offset and gain register for each channel input. The gain and offset registers, which are used during both self and system calibration, are used to set the zero and gain slope of the

converter's transfer function. As shown in *Offset Register* section, one LSB in the offset register is 1.835007966 X 2-24 proportion of the input span (bipolar span is 2 times the unipolar span, gain register = 1.000...000 decimal). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). Note that the magnitude of the offset that is trimmed from the input is mapped through the gain register. The converter can typically trim ±100 percent of the input span. As shown in the *Gain Register* section, the gain register spans from 0 to (64 - 2-24). The decimal equivalent meaning of the gain register is

$$D = b_{D29}2^{5} + b_{D28}2^{4} + b_{D27}2^{3} + \ldots + b_{D0}2^{-24}) = \sum_{i=0}^{29} b_{Di}2^{(-24+i)}$$

where the binary numbers have a value of either zero or one (bD29 is the binary value of bit D29). While gain register settings of up to 64 - 2-24 are available, the gain register should never be set to values above 40.

Gain Register

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
NU	NU	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB
2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{22}	2^{-23}	2^{-24}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The gain register span is from 0 to (64-2^{-24}). After Reset D24 is 1, all other bits are '0'.

Offset Register

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Sign	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	NU	NU	NU	NU	NU	NU	NU	NU
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

One LSB represents 1.835007966 X 2^{-24} proportion of the input span (bipolar span is 2 times unipolar span).
Offset and data word bits align by MSB. After reset, all bits are '0'.
The offset register is stored as a 32-bit, two's complement number, where the last 8 bits are all 0.

Performing Calibrations

To perform a calibration, the user must send a command byte with its MSB=1, its pointer bits (CSRP2-CSRP0) set to address the desired Setup to calibrate, and the appropriate calibration bits (CC2- CC0) set to choose the type of calibration to be performed. Note that calibration assumes that the CSRs have been previously initialized because the information concerning the physical channel, its filter rate, gain range, and polarity, comes from the channel-setup register addressed by the pointer bits in the command byte. Once the CSRs are initialized, a calibration can be performed with one command byte.

The length of time it takes to do a calibration is slightly less than the amount of time it takes to do a single conversion (see Table 14 for single conversion timing). Offset calibration takes 608 clock cycles less than a single conversion when FRS = 0, and 729 clock cycles less when FRS = 1. Gain calibration takes 128 clock cycles less than a single conversion when FRS = 0, and 153 clock cycles less when FRS = 1.

Once a calibration cycle is complete, SDO falls and the results are automatically stored in either the gain or offset register for the physical channel being calibrated when the OGS bit in the Configuration Register is set to '0'. If the OGS bit is set to '1', the results will be stored in the register specified by the OG1-OG0 bits of the selected Setup. See the OGS bit description for more details (Section 2.3.7). SDO will remain low until the next command word is begun. If additional calibrations are performed while referencing the same calibration registers, the last calibration results will replace the effects from the previous calibration as only one offset and gain register is available per physical channel. Only one calibration is performed with each command byte. To calibrate all the channels, additional calibration commands are necessary.

Self Calibration

The LHA7532 offer both self-offset and self-gain calibrations. For the self calibration of offset, the converters internally tie the inputs of the 1x amplifier together and routes them to the AIN- pin as shown in Figure 23. For accurate self calibration of offset to occur, the AIN pins must be at the proper common-mode voltage as specified in the Analog Characteristics section. Self-offset calibration uses the 1x gain amplifier, and is therefore not valid in the 2x-64x gain ranges. A self-offset calibration of these gain ranges can be performed by setting the IS bit in the configuration register to a '1', and performing a system offset calibration. The IS bit must be returned to '0' afterwards for normal operation of the device.

For self calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure 24. Self calibration of gain is performed in the GAIN = 1x mode without regard to the setup register's gain setting. LHA753x all gains are calibrated factory achieving 0.01% accuracy. Normally, the gain accuracy is good enough that customer does not need to do more calibration.

System Calibration

For the system calibration functions, the user must supply the converter's calibration signals which represent ground and full scale. When a system offset calibration is performed, a ground-referenced signal must be applied to the converters. Figure 25 illustrates system offset calibration.

As shown in Figure 26, the user must input a signal representing the positive full-scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the System Calibration Specifications).

Calibration Tips

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the channel setup registers. Due to limited register lengths in the faster word-rate filters (240 SPS and higher), channels that are used at these rates should also be calibrated in one of these word rates, and channels used in the lower word rates (120 SPS and lower) should be calibrated at one of these lower rates. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at the lowest possible output word rate for maximum accuracy. For the 7.5 SPS to 120 SPS word rate settings, calibrations can be performed at 7.5 SPS, and for 240 SPS and higher, calibration can be performed at 240 SPS. To minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port. Reading the calibration registers and averaging multiple calibrations together can produce a more accurate calibration result. Note that accessing the ADC's serial port before a calibration has finished may result in the loss of synchronization between the microcontroller and the ADC, and may prematurely halt the calibration cycle.

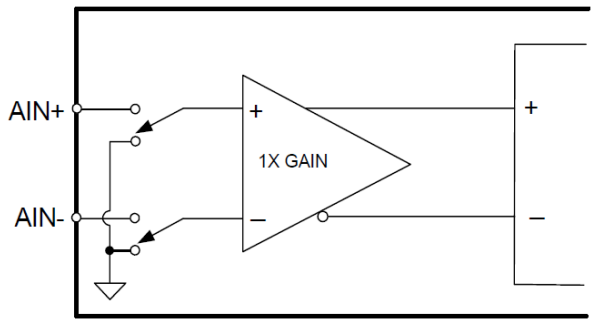


Figure 23. Self Calibration of Offset

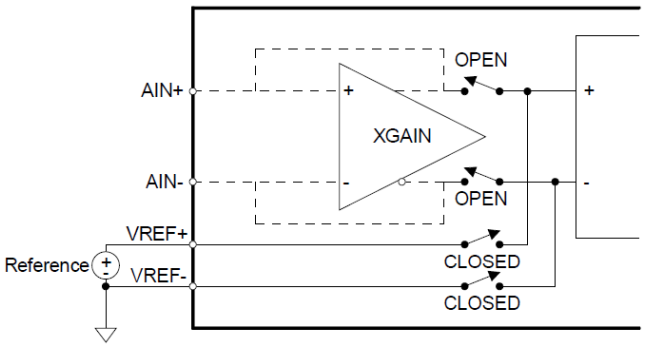


Figure 24. Self Calibration of Gain

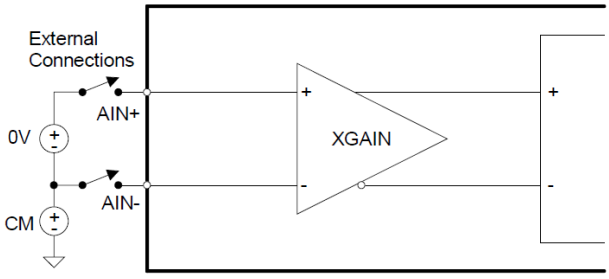


Figure 25. System Calibration of Offset

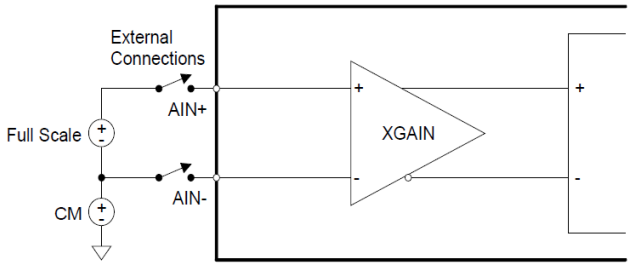


Figure 26. System Calibration of Gain

For maximum accuracy, calibrations should be performed for both offset and gain (selected by changing the G2-G0 bits of the channel-setup registers). Note that only one gain range can be calibrated per physical channel when the OGS bit in the Configuration Register is set to '0'. Multiple gain ranges can be calibrated for a single channel by manipulating the OGS bit and the OG1-OG0 bits of the selected Setup (see Section 2.3.7 for more details). If factory calibration of the user's system is performed using the system calibration capabilities of the LHA7532, the offset and gain register contents can be read by the system microcontroller and recorded in non-volatile memory. These same calibration words can then be uploaded into the offset and gain registers of the converter when power is first applied to the system, or when the gain range is changed.

When the device is used without calibration, the uncalibrated gain accuracy is about ±0.01% because the device is already calibrated in factory.

Note that the gain from the offset register to the output is 1.83007966 decimal, not 1. If a user wants to adjust the calibration coefficients externally, they will need to divide the information to be written to the offset register by the scale factor of 1.83007966. (This discussion assumes that the gain register is 1.000...000 decimal. The offset register is also multiplied by the gain register before being applied to the output conversion words).

Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the Analog Input section of this data sheet. For gain calibration, the full-scale input signal can be reduced to 3% of the nominal full scale value. At this point, the gain register is approximately equal to 33.33 (decimal). While the gain register can hold numbers all the way up to 64 - 2-24, gain register settings above a decimal value of 40 should not be used. With the converter's intrinsic gain error, this minimum full-scale input signal may be higher or lower. In defining the minimum Full Scale Calibration Range (FSCR) under Analog Characteristics, margin is retained to accommodate the intrinsic gain error. Inversely, the input full-scale signal can be increased to a point in which the modulator reaches its 1's density limit of 86 percent, which under nominal conditions occurs when the full-scale input signal is 1.1 times the nominal full-scale value. With the chip's intrinsic gain error, this maximum full-scale input signal maybe higher or lower. In defining the maximum FSCR, margin is again incorporated to accommodate the intrinsic gain error.

7.6. Performing Conversions

The LHA7532 offers two distinctly different conversion modes. The three sections that follow detail the differences

and provide examples illustrating how to use the conversion modes with the channel setup registers.

Single Conversion Mode

Based on the information provided in the channel setup registers (CSRs), after the user transmits the conversion command, a single, fully settled conversion is performed. The command byte includes a pointer address to the Setup register to be used during the conversion. Once transmitted, the serial port enters data mode where it waits until the conversion is complete. When the conversion data is available, SDO falls to logic 0. Forty SCLKs are then needed to read the conversion data word. The first 8 SCLKs are used to clear the SDO flag. During the first 8 SCLKs, SDI must be logic 0. The last 32 SCLKs are needed to read the conversion result. Note that the user is forced to read the conversion in single conversion mode as SDO will remain low (i.e. the serial port is in data mode) until SCLK transitions 40 times. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued. The single conversion mode will take longer than conversions performed in the continuous conversion mode. The number of clock cycles a single conversion takes for each Output Word Rate (OWR) setting is listed in Table 14. The ±8 (FRS = 0) or ±10 (FRS = 1) clock ambiguity is due to internal synchronization between the SCLK input and the oscillator.

Note: In the single conversion mode, more than one conversion is actually performed, but only the final, fully settled result is output to the conversion data register.

Table 14. Conversion Timing – Single Mode

(WR3-WR0)	Clock Cycles	
	FRS=0	FRS=1
0000	171448 ± 8	205738 ± 10
0001	335288 ± 8	402346 ± 10
0010	662968 ± 8	795562 ± 10
0011	1318328 ± 8	1581994 ± 10
0100	2629048 ± 8	3154858 ± 10
1000	7592 ± 8	9110 ± 10
1001	17848 ± 8	21418 ± 10
1010	28088 ± 8	33706 ± 10
1011	48568 ± 8	58282 ± 10
1100	89528 ± 8	107434 ± 10

Continuous Conversion Mode

Based on the information provided in the channel setup registers (CSRs), continuous conversions are performed using the Setup register contents pointed to by the conversion command. The command byte includes a pointer address to the Setup register to be used during the conversion. Once transmitted, the serial port enters data mode where it waits until a conversion is complete. After the conversion is done, SDO falls to logic 0. Forty SCLKs are then needed to read the conversion. The first 8 SCLKs are used to clear the SDO flag. The last 32 SCLKs are needed to read the conversion result. If '00000000' is provided to SDI during the first 8 SCLKs when the SDO flag is cleared, the converter remains in this conversion mode and continues to convert the selected channel using the same CSR Setup. In continuous conversion mode, not every conversion word needs to be read. The user needs only to read the conversion words required for the application as SDO rises and falls to indicate the availability of new conversion data. Note that if a conversion is not read before the next conversion data becomes available, it will be lost and replaced by the new conversion data. To exit this conversion mode, the user must provide '11111111' to the SDI pin during the first 8 SCLKs after SDO falls. If the user decides to exit, 32 SCLKs are required to clock out the last conversion before the converter returns to command mode. The number of clock cycles a continuous conversion takes for each Output Word Setting is listed in Table 15. The first conversion from the part in continuous conversion mode will be longer than the following conversions due to start-up overhead. The ± 8 (FRS = 0) or ± 10 (FRS = 1) clock ambiguity is due to internal synchronization between the SCLK input and the

oscillator.

Note: When changing channels, or after performing calibrations and/or single conversions, the user must ignore the first three (for OWRs less than 3200 SPS, MCLK = 4.9152 MHz) or first five (for OWR ⩾ 3200 SPS) conversions in continuous conversion mode, as residual filter coefficients must be flushed from the filter before accurate conversions are performed.

Table 15. Conversion Timing – Continuous Mode

FRS	(WR3-WR0)	Clock Cycles (First Conversion)	Clock Cycles (All Other Conversions)
0	0000	89528 ± 8	40960
0	0001	171448 ± 8	81920
0	0010	335288 ± 8	163840
0	0011	662968 ± 8	327680
0	0100	1318328 ± 8	655360
0	1000	2472 ± 8	1280
0	1001	12728 ± 8	2560
0	1010	17848 ± 8	5120
0	1011	28088 ± 8	10240
0	1100	48568 ± 8	20480
1	0000	107434 ± 10	49152
1	0001	205738 ± 10	98304
1	0010	402346 ± 10	196608
1	0011	795562 ± 10	393216
1	0100	1581994 ± 10	786432
1	1000	2966 ± 10	1536
1	1001	15274 ± 10	3072
1	1010	21418 ± 10	6144
1	1011	33706 ± 10	12288
1	1100	58282 ± 10	24576

Examples of Using CSRs to Perform Conversions and Calibrations

Any time a calibration or conversion command is issued (C, MC, and CC2-CC0 bits must be properly set), the CSRP2-CSRP0 bits in the command byte are used as pointers to address one of the Setups in the channel-setup registers (CSRs). Table 16 details the address decoding of the pointer the bits.

Table 16. Command Byte Pointer

(CSRP2-CSRP0)	CSR Location	Setup
000	CSR #1	1
001	CSR #1	2
010	CSR #2	3
011	CSR #2	4
100	CSR #3	5
101	CSR #3	6
110	CSR#4	7
111	CSR #4	8

The examples that follow detail situations that a user might encounter when acquiring a conversion or calibrating the converter. These examples assume that the CSRs are programmed with the following physical channel order: 4, 1, 1, 2, 4, 3, 4, 4. A physical channel is defined as the actual input channel (AIN1 to AIN4) to which an external

signal is connected.

Example 1: Single conversion using Setup 1. The command issued is '10000000'. This instructs the converter to perform a single conversion referencing Setup 1 (CSRP2 - CSRP0 = '000') In this example, Setup 1 points to physical channel 4. After the command is received and decoded, the ADC performs a conversion on physical channel 4 and SDO falls to indicate that the conversion is complete. To read the conversion, 40 SCLKs are then required. Once the conversion data has been read, the serial port returns to the command mode.

Example 2: Continuous conversions using Setup 3. The command issued is '11010000'. This instructs the converter to perform continuous conversions referencing Setup 3 (CSRP2 - CSRP0 = '010'). In this example, Setup 3 points to physical channel 1. After the command is received and decoded, the ADC performs a conversion on physical channel 1 and SDO falls to indicate that the conversion is complete. The user now has three options. The user can acquire the conversion and remain in this mode, acquire the conversion and exit this mode, or ignore the conversion and wait for a new conversion at the next update interval, as detailed in the continuous conversion section.

Example 3: Calibration using Setup 4. This example assumes that the OGS bit in the Configuration Register is set to '0'. The command issued is '10011001'. This instructs the converter to perform a self offset calibration referencing Setup 4 (CSRP2 - CSRP0 = '011'). In this example, Setup 4 points to physical channel 2. After the command is received and decoded, the ADC performs a self offset calibration on physical channel 2 and SDO falls to indicate that the calibration is complete. To perform additional calibrations, more commands must be issued.

Note: The CSRs need not be written. If they are not initialized, all the Setups point to their default settings irrespective of the conversion or calibration mode (i.e conversions can be performed, but only physical channel 1 will be converted). Further note that filter convolutions are reset (i.e. flushed) if consecutive conversions are performed on two different physical channels. If consecutive conversions are performed on the same physical channel, the filter is not reset. This allows the ADCs to more quickly settle full scale step inputs.

7.7. Using Multiple ADCs Synchronously

Some applications require synchronous data outputs from multiple ADCs converting different analog channels. Multiple LHA7532 parts can be synchronized in a single system by using the following guidelines:

1) All of the ADCs in the system must be operated from the same oscillator source.

2) All of the ADCs in the system must share common SCLK and SDI lines.

3) A software reset must be performed at the same time for all of the ADCs after system power-up (by selecting all of the ADCs using their respective CS pins, and writing the reset sequence to all parts, using SDI and SCLK).

4) A start conversion command must be sent to all of the ADCs in the system at the same time. The ±8 clock cycles of ambiguity for the first conversion (or for a single conversion) will be the same for all ADCs, provided that they were all reset at the same time.

5) Conversions can be obtained by monitoring SDO on only one ADC, (bring CS high for all but one part) and reading the data out of each part individually, before the next conversion data words are ready.

An example of a synchronous system using two LHA7532 parts is shown in Figure 27.

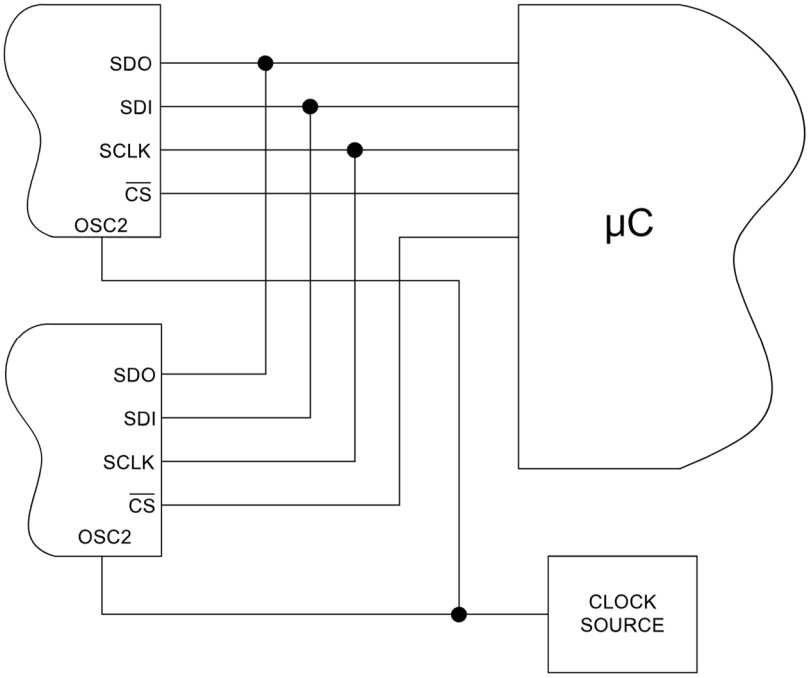


Figure 27. Synchronizing Multiple ADCs

7.8. Conversion Output Coding

The LHA7532 output 24-bit data conversion words. To read a conversion word the user must read the conversion data register. The conversion data register is 32 bits long and outputs the conversions MSB first. The last byte of the conversion data register contains data monitoring flags. The channel indicator (CI) bits keep track of which physical channel was converted and the overrange flag (OF) monitors to determine if a valid conversion

was performed. Refer to the Conversion Data Output Descriptions section for more details.

The LHA7532 output data conversions in binary format when operating in unipolar mode and in two's complement format when operating in bipolar mode. Table 17 shows the code mapping for both unipolar and bipolar mode. VFS in the tables refers to the positive full-scale voltage range of the converter in the specified gain range, and -VFS refers to the negative full-scale voltage range of the converter. The total differential input range (between AIN+ and AIN-) is from 0 to VFS in unipolar mode, and from -VFS to VFS in bipolar mode.

Table 17. Output Coding for 24-bit LHA7532 and LHA7534

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFFF	>(VFS-1.5 LSB)	7FFFFF
VFS-1.5 LSB	FFFFFF ------ FFFFFE	VFS-1.5 LSB	7FFFFF ------ 7FFFFE
VFS/2-0.5 LSB	800000 ------ 7FFFFF	-0.5 LSB	000000 ------ FFFFFF
+0.5 LSB	000001 ------ 000000	-VFS+0.5 LSB	800001 ------ 800000
<(+0.5 LSB)	000000	<(-VFS+0.5 LSB)	800000

Conversion Data Output Descriptions

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
MSB	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	LSB	0	0	0	0	0	OF	CI1	CI0

Conversion Data Bits [31:8]

These bits depict the latest output conversion.

NU (Not Used) [7:3]

These bits are masked logic zero.

OF (Over-range Flag Bit) [2]

0 Bit is clear when over-range condition has not occurred.

1 Bit is set when input signal is more positive than the positive full scale, more negative than zero (unipolar mode) or when the input is more negative than the negative full scale (bipolar mode).

CI (Channel Indicator Bits) [1:0]

These bits indicate which physical input channel was converted.

00 Physical Channel 1

01 Physical Channel 2

10 Physical Channel 3

11 Physical Channel 4

7.9. Digital Filter

The LHA7532 have linear phase digital filters which are programmed to achieve a range of output word rates (OWRs) as stated in the Channel-Setup Register Descriptions section. The ADCs use a Sinc5 digital filter to output word rates at 3200 SPS and 3840 SPS (MCLK = 4.9152 MHz). Other output word rates are achieved by using the Sinc5 filter followed by a Sinc3 filter with a programmable decimation rate. Figure 28 shows the magnitude response of the 60 SPS filter, while Figure 29 and Figure 30 show the magnitude and phase response of the filter at 120 SPS. The Sinc3 is active for all output word rates except for the 3200 SPS and 3840 SPS (MCLK = 4.9152 MHz) rate. The Z-transforms of the two filters are shown in Figure 31. For the Sinc3 filter, “D” is the programmable decimation ratio, which is equal to 3840/OWR when FRS = 0 and 3200/OWR when FRS = 1.

The converter’s digital filters scale with MCLK. For example, with an output word rate of 120 SPS, the filter’s corner frequency is at 31 Hz. If MCLK is increased to 5.0 MHz, the OWR increases by 1.0175% and the filter’s corner frequency moves to 31.54 Hz. Note that the converter is not specified to run at MCLK clock frequencies greater than 5 MHz.

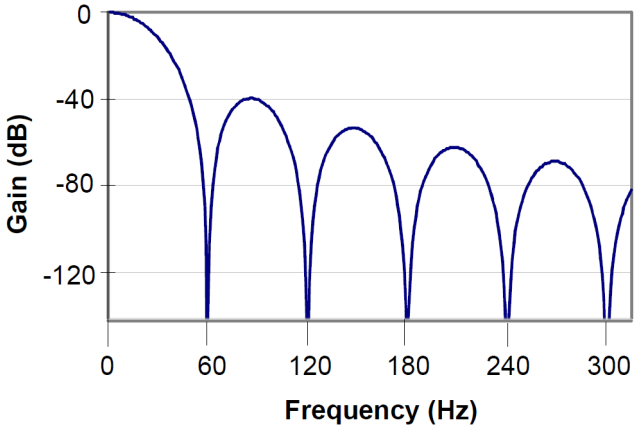


Figure 28. Digital Filter Response (WR = 60 SPS)

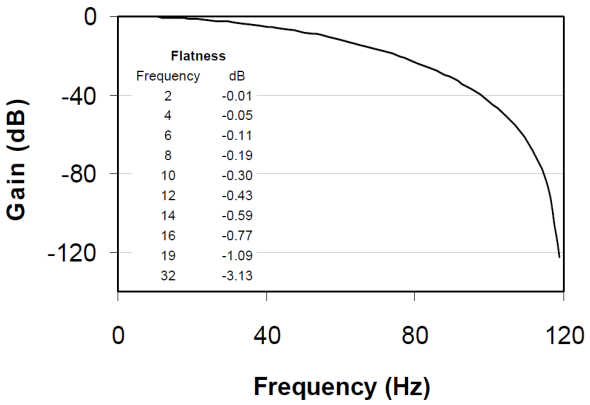


Figure 29. 120 SPS Filter Magnitude Plot to 120 Hz

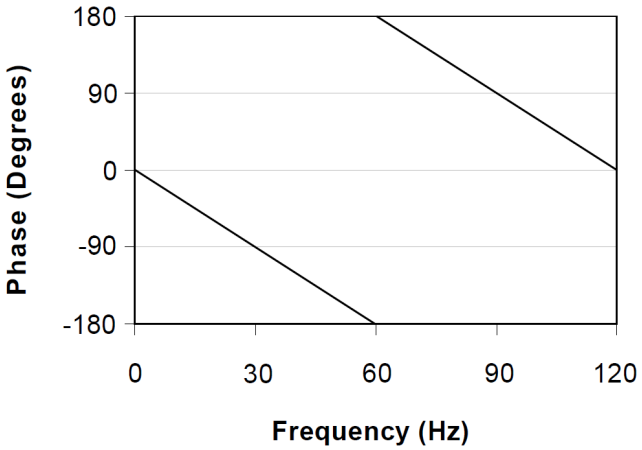


Figure 30. 120 SPS Filter Phase Plot to 120 Hz

$$Sinc^5 = \frac{(1-z^{-80})^5}{(1-z^{-16})^5} \times \frac{(1-z^{-16})^3}{(1-z^{-4})^3} \times \frac{(1-z^{-4})^2}{(1-z^{-2})^2} \times \frac{(1-z^{-2})^3}{(1-z^{-1})^3}$$

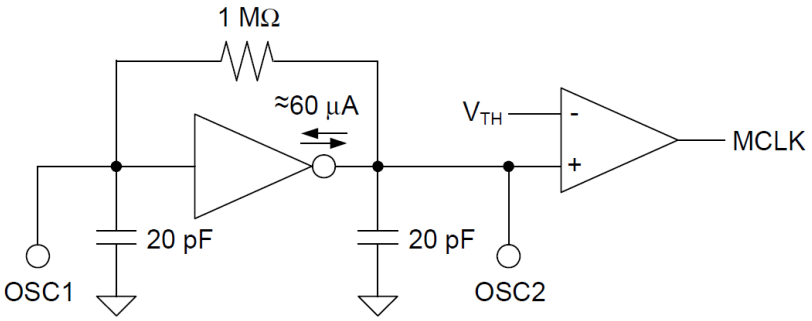
$$Sinc^3 = \frac{(1-z^{-D})^3}{(1-z^{-1})^3}$$

Figure 31. Z-Transforms of Digital Filters

7.10. CLOCK GENERATOR

The LHA7532 include an on-chip inverting amplifier which can be connected with an external crystal to provide the master clock for the chip. Figure 32 illustrates the on-chip oscillator. It includes loading capacitors and a feedback resistor to form a Pierce oscillator configuration. The chips are designed to operate using a 4.9152 MHz crystal; however, other crystals with frequencies between 1 MHz to 5 MHz can be used. One lead of the crystal should be connected to OSC1 and the other to OSC2. Lead lengths should be minimized to reduce stray capacitance. Note that while using the on-chip oscillator, neither OSC1 or OSC2 is capable of directly driving any off-chip logic. When the on-chip oscillator is used, the voltage on OSC2 is typically 0.5 V peak-to-peak. This signal is not compatible with external logic unless additional external circuitry is added. The OSC2 output should be used if the on-chip oscillator output is used to drive other circuitry.

The designer can use an external CMOS compatible oscillator to drive OSC2 with a 1 MHz to 5 MHz clock for the ADC. The external clock into OSC2 must overdrive the 60 µA output of the on-chip amplifier. This will not harm the on-chip circuitry. In this scheme, OSC1 should be left unconnected.



NOTE: 20 pF capacitors are on chip and should not be added externally.

Figure 32. On-chip Oscillator Model

7.11. TEMPERATURE SENSOR

Embedded in the LHA7532/34 is a temperature sensor that is useful to monitor the die temperature. This is selected using the TEMP_SEL bit in the Configuration register. Thus, the analog input is Temperature Sensor – AVSS. The equation forthe temperature sensor is

Temperature (°C) = ((Volt/0.00034) - 290.5

The Volt voltage is the voltage value calculated from the ADC code.The temperature sensor has an accuracy of ±2°C typically and only support for PGA gain 1.

7.12. Power Supply Arrangements

The LHA7532 are designed to operate from single or dual analog supplies and a single digital supply. The following power supply connections are possible:

VA+ = +3 V to +5 V; VA- = 0 V; VD+ = +3 V to +5 V

VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V

VA+ = +1.8 V; VA- = -1.8 V; VD+ = +3 V to +5 V

A VA+ supply of +2.5 V, +3.0 V, or +5.0 V should be maintained at ±5% tolerance. A VA- supply of -2.5 V or -3.0 V should be maintained at ±5% tolerance. VD+ can extend from +2.7 V to +5.5 V with the additional restriction that

[(VD+) – (VA-)] < 7.5 V.

Figure 33 illustrates the LHA7532 connected with a single +5.0 V supply to measure differential inputs relative to a common mode of 2.5 V. Figure 34 illustrates the LHA7532 connected with ±2.5 V bipolar analog supplies and a +3 V to +5 V digital supply to measure ground referenced bipolar signals.

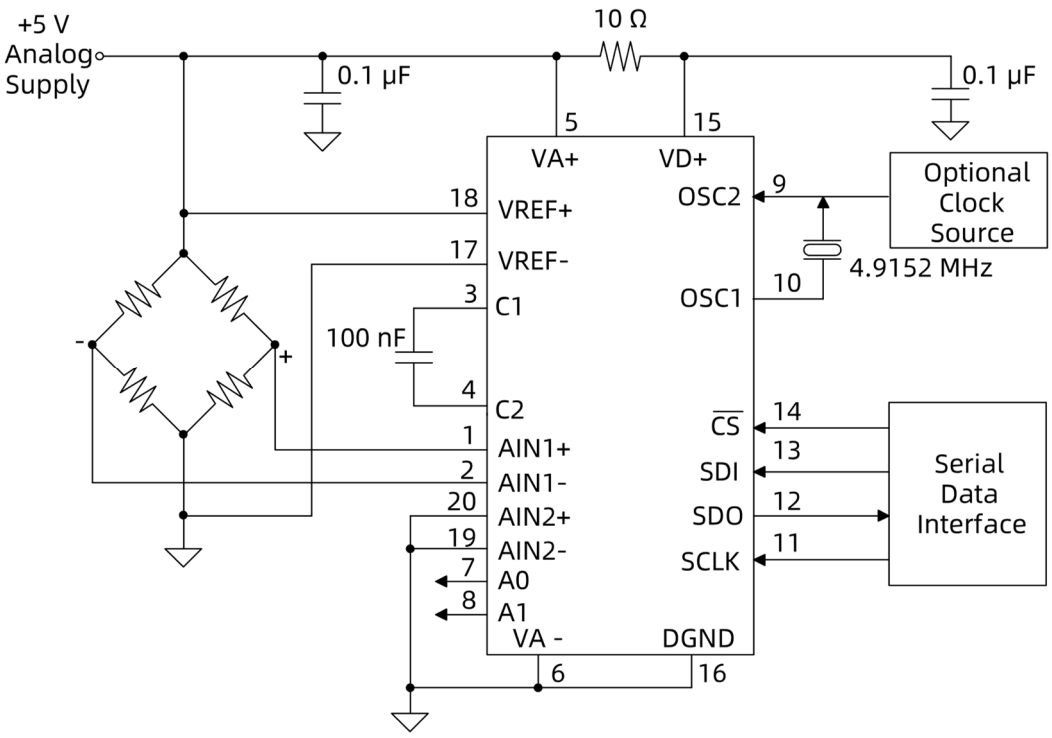


Figure 33. LHA7532 Configured with a Single +5 V Supply

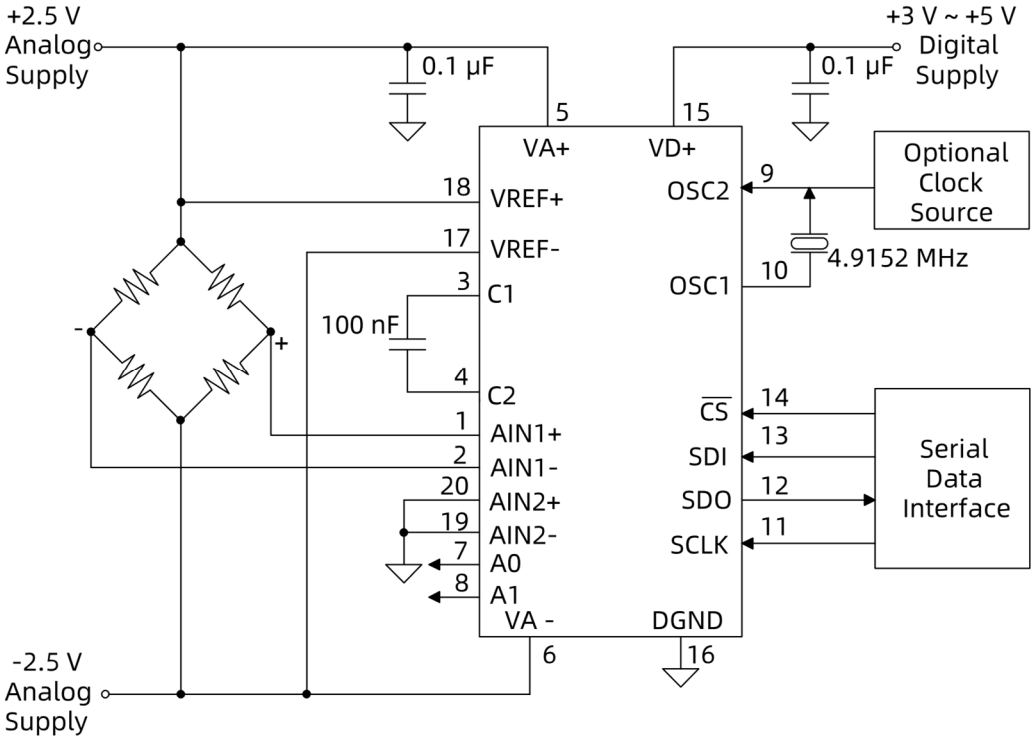


Figure 34. LHA7532 Configured with ±2.5 V Analog Supplies

7.13. Getting Started

This A/D converter has several features. From a software programmer's prospective, what should be done first? To begin, a 4.9152 MHz or 4.096 MHz crystal takes approximately 20 ms to start. To accommodate for this, it is recommended that a software delay of approximately 20 ms start the processor's ADC initialization code. Next, since the LHA7532 do not provide a power-on-reset function, the user must first initialize the ADC to a known state. This is accomplished by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Once the serial port of the ADC is in the command mode, the user must reset all the internal logic by performing a system reset sequence (see 2.3.2 System Reset Sequence). The next action is to initialize the voltage reference mode. The Voltage Range Select (VRS) bit in the configuration register must be set based upon the magnitude of the reference voltage between the VREF+ and the VREF- pins.

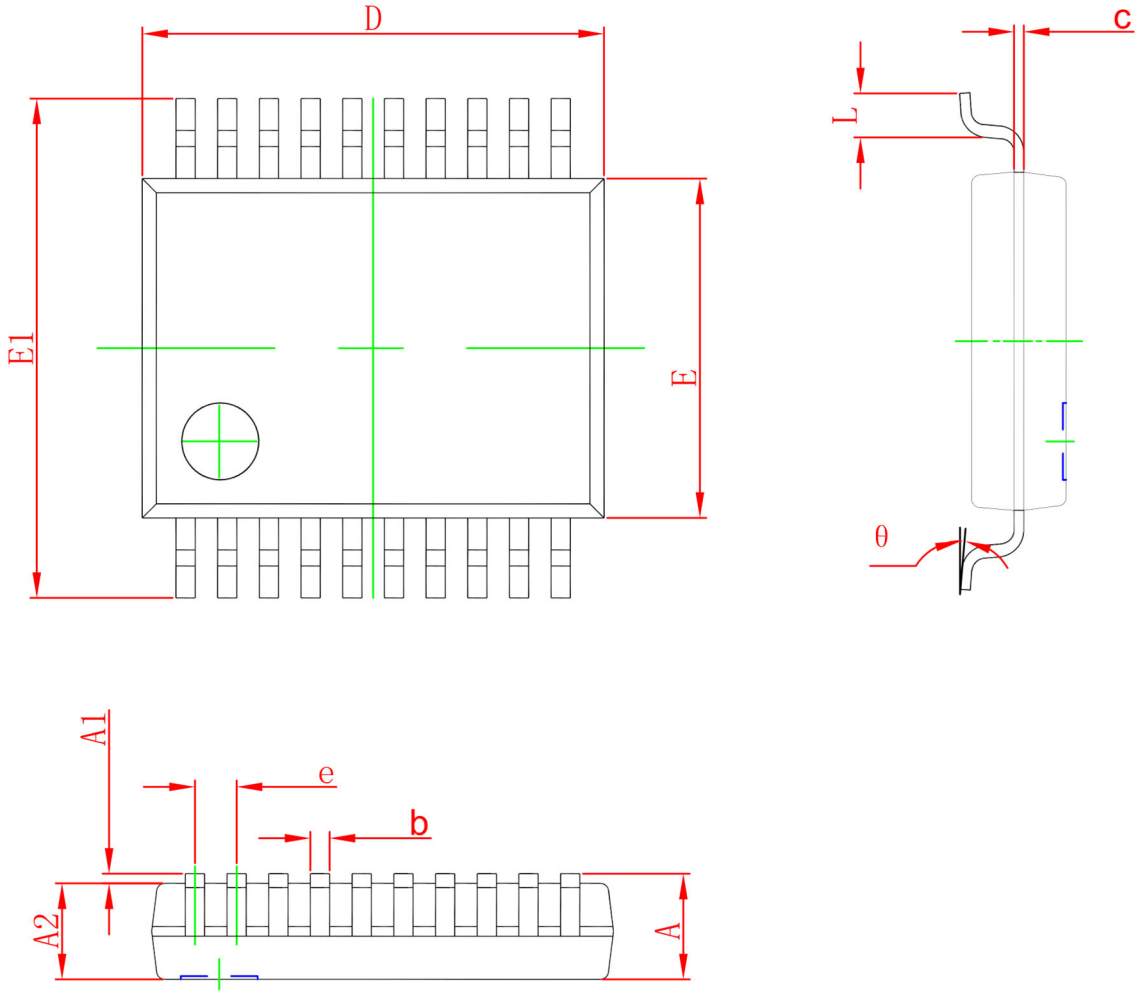
After this, the channel-setup registers (CSRs) should be initialized, as these registers determine how calibrations and conversions will be performed. Once the CSRs are initialized, the user has three options in calibrating the ADC: 1) don't calibrate and use the default settings; 2) perform self or system calibrations; or 3) upload previously saved calibration results to the offset and gain registers. At this point, the ADC is ready to perform conversions.

7.14. PCB Layout

For optimal performance, the LHA7532 should be placed entirely over an analog ground plane. All grounded pins on the ADC, including the DGND pin, should be connected to the analog ground plane that runs beneath the chip. In a split-plane system, place the analog-digital plane split immediately adjacent to the digital portion of the chip.

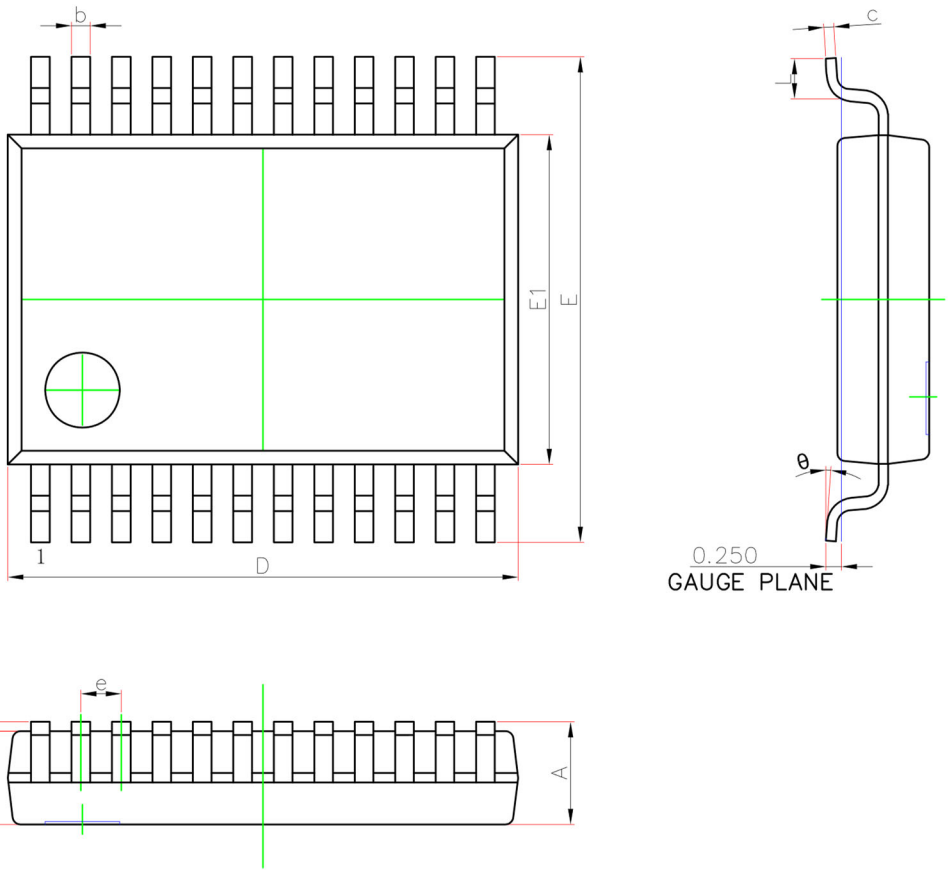
8. PACKAGE DRAWINGS

SSOP20(209mil) PACKAGE OUTLINE DIMENSIONS



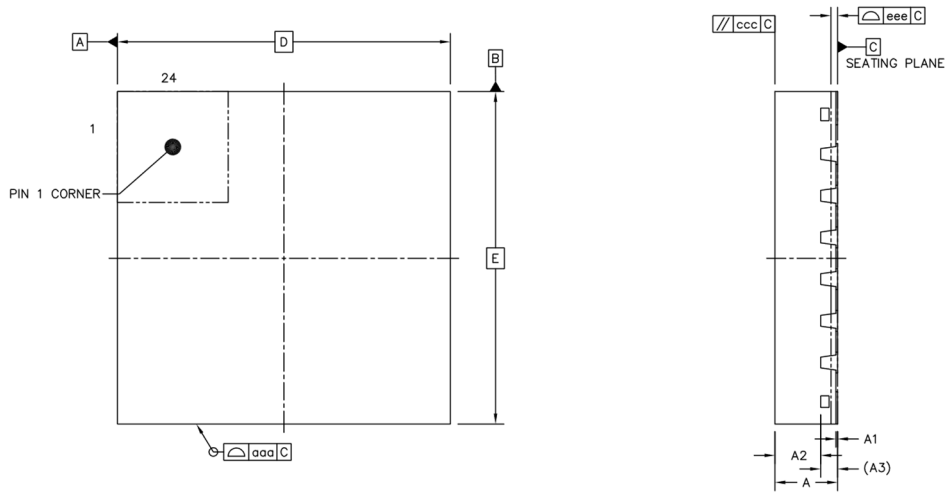
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.730		0.068
A1	0.050	0.230	0.002	0.009
A2	1.400	1.600	0.055	0.063
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	7.000	7.400	0.276	0.291
E	5.100	5.500	0.201	0.217
E1	7.600	8.000	0.299	0.315
e	0.65(BSC)		0.026(BSC)	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

SSOP24(209mil) PACKAGE OUTLINE DIMENSIONS



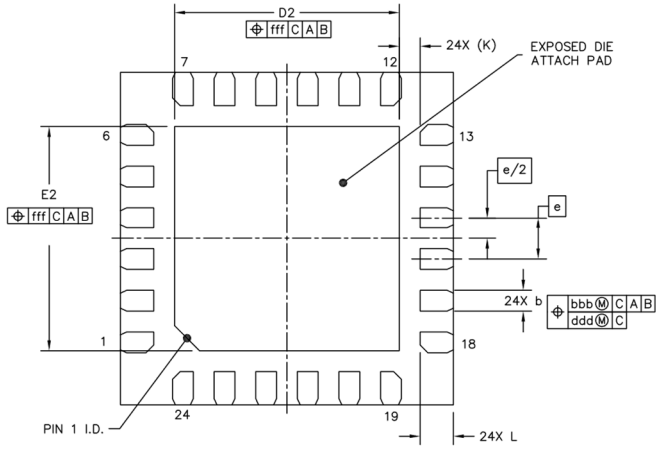
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.850	—	0.073
A1	0.050	—	0.002	—
A2	1.400	1.600	0.055	0.063
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	7.900	8.500	0.311	0.335
E1	5.000	5.600	0.197	0.220
E	7.400	8.200	0.291	0.323
e	0.650(BSC)		0.026(BSC)	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

QFN24 PACKAGE OUTLINE DIMENSIONS



TOP VIEW

SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

NOTES

1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP·Sn8~20s

9. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating	Max Floor Life
LHA7532SFSP	240 °C	2	365 Days
LHA7534SFSG	240 °C	2	365 Days
LHA7534SFQG	240 °C	2	365 Days

10. ORDERING GUIDE

Orderable Device	Channels	Package Type	Pin number	Packaging Type	MPQ	Remark
LHA7532SFSP	2	SSOP	20	REEL	2500EA/PACK	
LHA7534SFSG	4	SSOP	24	REEL	2500EA/PACK	
LHA7534SFQG	4	QFN	24	REEL	2500EA/PACK	