SSD1353

Advance Information

160RGB x 132 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD1353 is a CMOS OLED/PLED driver with 480 segments and 132 commons output, supporting up to 160RGB x 132 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1353 had embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 9, 16, 18 bits 8080 / 6800 parallel interface as well as Serial Peripheral Interface. It has 256-step contrast and 262K color control, giving vivid color display to OLED panels. This driver IC can be widely used in many applications such as MP3, PDA, PMP, mobile phone and Digital Camera.

2 FEATURES

- Resolution: 160 RGB x 132 dot matrix panel
- Portrait and Landscape mode data input
- 262k color depth supported by embedded 160x132x18 bit SRAM display buffer
- Power supply
  - V_{DD} = 2.4V – 2.6V (Core V_{DD} power supply)
  - V_{DDIO} = 1.6V – V_{CI} (MCU interface logic level)
  - V_{CI} = 2.4V - 3.5V (Low voltage power supply)
  - V_{CC} = 10.0V – 21.0V (Panel driving power supply)
- Segment maximum source current: 160uA
- Common maximum sink current: 60mA
- 256 step brightness current control for the each color component plus 16 step master current control
- Pin selectable MCU Interfaces:
  - 8/9/16/18 bits 6800-series parallel interface
  - 8/9/16/18 bits 8080-series parallel interface
  - Serial Peripheral Interface
- Color swapping function (RGB – BGR)
- Support various color depth
  - 262k color (6:6:6)
  - 65k color (5:6:5)
  - 256 color (3:3:2)
- Screen saving continuous scrolling function in both horizontal and vertical action
- Graphic Accelerating Command (GAC) set
- Programmable Gamma functions
- RAM write synchronization signal
- Programmable Frame Rate
- On Chip Oscillator
- Power saving mode
- Dim mode
- Non-Volatile Memory (OTP) for color coordinate calibration
- Slim chip layout best suit for COF
- Operating temperature range -40°C to 85°C.

3 ORDERING INFORMATION

Table 3-1 : Ordering Information

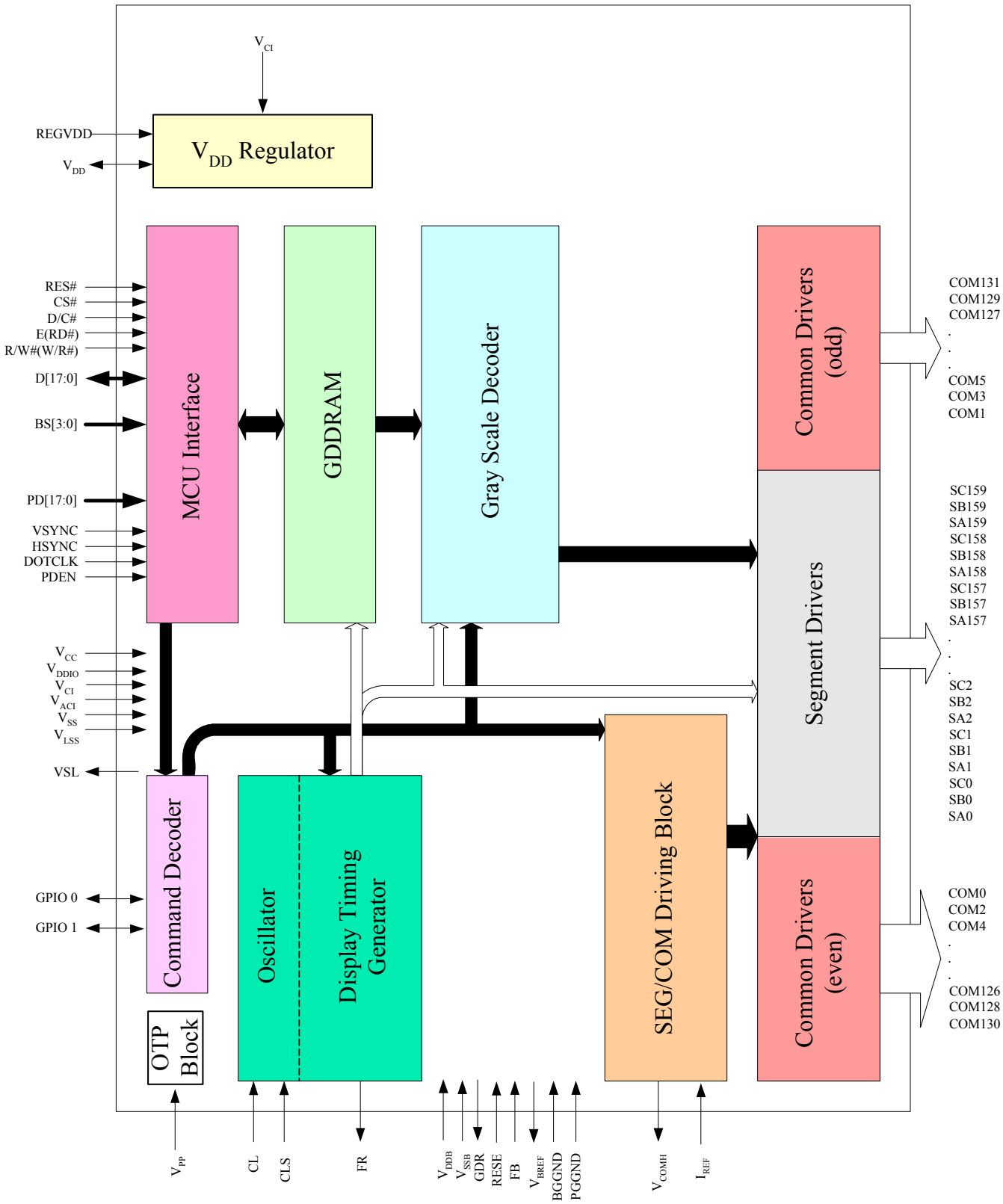
Ordering Part Number	SEG	COM	Package Form	Reference	Remark

SSD1353U7R1	160RGB	128	COF	Page 15, 72	• 48mm film, 4 sprocket holes
					• Output lead pitch:
					  • SEG: 0.05mm x 0.999=0.04995mm
					  • COM: 0.07mm x 0.999=0.06993mm
					• 8-/9-/16-/18-bit 80 / 68 parallel & SPI interface

SSD1353Z	160RGB	128	Gold Bump Die	Page 9, 74	• Min SEG pad pitch : 40.1um • Min COM pad pitch : 40um

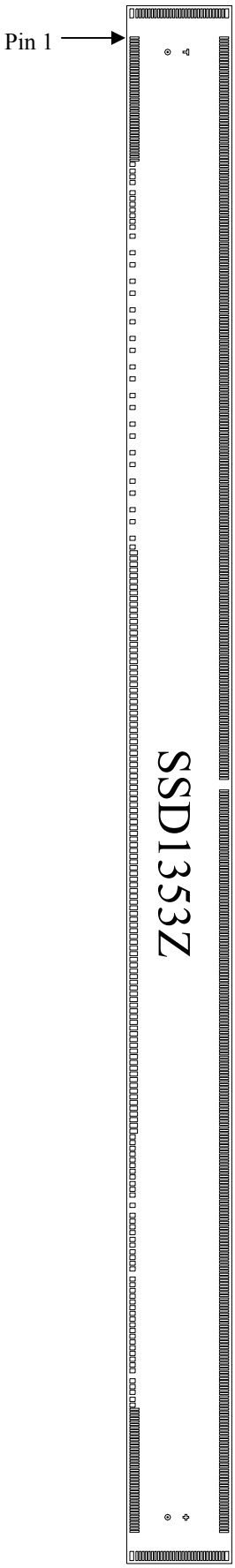
4 BLOCK DIAGRAM

Figure 4-1 : SSD1353 Block Diagram



5 DIE FLOOR PLAN

Figure 5-1 SSD1353Z Die drawing

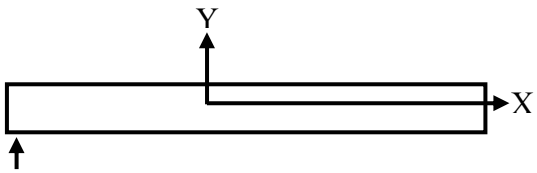


Alignment marks
(For details dimension please refer to Figure 5-2)

	Position	Size
o shape	(9594.26, -152.08)	R37.5um, inner 18um
+ shape	(9594.26, 86.2)	75um x 75um
o shape	(-9594.27, -152.08)	R37.5um, inner 18um
T shape	(-9594.27, 86.2)	75um x 75um

Die Size	20.4mm x 1.4mm
Die Thickness	457um
Min I/O pad pitch	75um
Min SEG pad pitch	40.1um
Min COM pad pitch	40um
Bump Height	nominal 15um

Bump Size	
Pad #	**size [um^2]**
Pad 2-42, 223-263, 265-293, 295-780, 782-810	25um x 120um
Pad 43-76, 179-222	55um x 70um
Pad 77-178	55um x 100um
Pad 1, 264, 294, 781	120um x 50um



Pad 1,2,3,…->264
Gold Bumps face

Table 5-1 : SSD1353Z Die Pad Coordinates

Pad no.	Pad Name	X-Axis	Y-Axis	Pad no.	Pad Name	X-Axis	Y-Axis	Pad no.	Pad Name	X-Axis	Y-Axis
1	NC	-10101.4	-620.0	81	GDR	-2737.0	-595.0	161	D11	3263.0	-595.0
2	NC	-9779.9	-585.0	82	GDR	-2662.0	-595.0	162	D12	3338.0	-595.0
3	NC	-9739.9	-585.0	83	GDR	-2587.0	-595.0	163	D13	3413.0	-595.0
4	COM95	-9699.9	-585.0	84	GDR	-2512.0	-595.0	164	D14	3488.0	-595.0
5	COM96	-9659.9	-585.0	85	VDDB	-2437.0	-595.0	165	D15	3563.0	-595.0
6	COM97	-9619.9	-585.0	86	VDDB	-2362.0	-595.0	166	D16	3638.0	-595.0
7	COM98	-9579.9	-585.0	87	FB	-2287.0	-595.0	167	D17	3713.0	-595.0
8	COM99	-9539.9	-585.0	88	VBREF	-2212.0	-595.0	168	VSS	3788.0	-595.0
9	COM100	-9499.9	-585.0	89	BGGND	-2137.0	-595.0	169	CLS	3863.0	-595.0
10	COM101	-9459.9	-585.0	90	BGGND	-2062.0	-595.0	170	VDDIO	3938.0	-595.0
11	COM102	-9419.9	-585.0	91	VSS	-1987.0	-595.0	171	VDDIO	4013.0	-595.0
12	COM103	-9379.9	-585.0	92	PGGND	-1912.0	-595.0	172	VCI	4088.0	-595.0
13	COM104	-9339.9	-585.0	93	RESE	-1837.0	-595.0	173	VCI	4163.0	-595.0
14	COM105	-9299.9	-585.0	94	VCI	-1762.0	-595.0	174	VCI	4238.0	-595.0
15	COM106	-9259.9	-585.0	95	VDDB	-1687.0	-595.0	175	VDD	4313.0	-595.0
16	COM107	-9219.9	-585.0	96	VSL	-1612.0	-595.0	176	VDD	4388.0	-595.0
17	COM108	-9179.9	-585.0	97	VSL	-1537.0	-595.0	177	VDD	4463.0	-595.0
18	COM109	-9139.9	-585.0	98	VSL	-1462.0	-595.0	178	VDD	4538.0	-595.0
19	COM110	-9099.9	-585.0	99	VSL	-1387.0	-595.0	179	NC	4613.0	-610.0
20	COM111	-9059.9	-585.0	100	VACI	-1312.0	-595.0	180	NC	4688.0	-610.0
21	COM112	-9019.9	-585.0	101	VACI	-1237.0	-595.0	181	NC	4763.0	-610.0
22	COM113	-8979.9	-585.0	102	VCI	-1162.0	-595.0	182	IREF	4838.0	-610.0
23	COM114	-8939.9	-585.0	103	VCI	-1087.0	-595.0	183	VCI	4913.0	-610.0
24	COM115	-8899.9	-585.0	104	VCC	-1012.0	-595.0	184	VCI	4988.0	-610.0
25	COM116	-8859.9	-585.0	105	VCC	-937.0	-595.0	185	VCI	5063.0	-610.0
26	COM117	-8819.9	-585.0	106	VCC	-862.0	-595.0	186	VCI	5138.0	-610.0
27	COM118	-8779.9	-585.0	107	VLSS	-787.0	-595.0	187	VCI	5224.6	-610.0
28	COM119	-8739.9	-585.0	108	VLSS	-712.0	-595.0	188	VCI	5299.6	-610.0
29	COM120	-8699.9	-585.0	109	VLSS	-637.0	-595.0	189	VCI	5374.6	-610.0
30	COM121	-8659.9	-585.0	110	VLSS	-562.0	-595.0	190	NC	5509.5	-610.0
31	COM122	-8619.9	-585.0	111	VPP	-487.0	-595.0	191	VCC	5641.0	-610.0
32	COM123	-8579.9	-585.0	112	VPP	-412.0	-595.0	192	VCC	5716.0	-610.0
33	COM124	-8539.9	-585.0	113	VPP	-337.0	-595.0	193	VCC	5791.0	-610.0
34	COM125	-8499.9	-585.0	114	VPP	-262.0	-595.0	194	VCC	5866.0	-610.0
35	COM126	-8459.9	-585.0	115	VPP	-187.0	-595.0	195	VDD	5955.6	-610.0
36	COM127	-8419.9	-585.0	116	VDD	-112.0	-595.0	196	VDD	6030.6	-610.0
37	COM128	-8379.9	-585.0	117	VDD	-37.0	-595.0	197	VDD	6117.2	-610.0
38	COM129	-8339.9	-585.0	118	VDD	38.0	-595.0	198	VDD	6192.2	-610.0
39	COM130	-8299.9	-585.0	119	VDD	113.0	-595.0	199	VDD	6267.2	-610.0
40	COM131	-8259.9	-585.0	120	VDD	188.0	-595.0	200	VDD	6342.2	-610.0
41	NC	-8219.9	-585.0	121	VDD	263.0	-595.0	201	VDD	6474.0	-610.0
42	NC	-8179.9	-585.0	122	VSS	338.0	-595.0	202	VDD	6549.0	-610.0
43	NC	-8124.9	-610.0	123	VDDIO	413.0	-595.0	203	VSS	6624.0	-610.0
44	VCC	-8035.3	-610.0	124	VDDIO	488.0	-595.0	204	VSS	6699.0	-610.0
45	VCC	-7960.3	-610.0	125	VSS	563.0	-595.0	205	VSS	6774.0	-610.0
46	VCC	-7885.3	-610.0	126	REGVDD	638.0	-595.0	206	VLSS	6849.0	-610.0
47	VCOMH	-7751.4	-610.0	127	VDDIO	713.0	-595.0	207	VLSS	6924.0	-610.0
48	VCOMH	-7676.4	-610.0	128	GP0	788.0	-595.0	208	VLSS	6999.0	-610.0
49	VLSS	-7601.4	-610.0	129	VSS	863.0	-595.0	209	VLSS	7074.0	-610.0
50	VLSS	-7526.4	-610.0	130	GP1	938.0	-595.0	210	VLSS	7149.0	-610.0
51	VSS	-7451.4	-610.0	131	VDDIO	1013.0	-595.0	211	VLSS	7224.0	-610.0
52	VSS	-7376.4	-610.0	132	BS0	1088.0	-595.0	212	VLSS	7299.0	-610.0
53	VSS	-7301.4	-610.0	133	VSS	1163.0	-595.0	213	VLSS	7374.0	-610.0
54	PDEN	-7183.6	-610.0	134	BS1	1238.0	-595.0	214	VCOMH	7449.0	-610.0
55	PD17	-6966.3	-610.0	135	VDDIO	1313.0	-595.0	215	VCOMH	7524.0	-610.0
56	PD16	-6809.7	-610.0	136	BS2	1388.0	-595.0	216	VCOMH	7599.0	-610.0
57	PD15	-6592.4	-610.0	137	VSS	1463.0	-595.0	217	VCOMH	7674.0	-610.0
58	PD14	-6435.7	-610.0	138	BS3	1538.0	-595.0	218	VCC	7807.9	-610.0
59	PD13	-6218.4	-610.0	139	VDDIO	1613.0	-595.0	219	VCC	7882.9	-610.0
60	PD12	-6061.7	-610.0	140	FR	1688.0	-595.0	220	VCC	7957.9	-610.0
61	PD11	-5844.5	-610.0	141	CL	1763.0	-595.0	221	NC	8049.9	-610.0
62	PD10	-5687.8	-610.0	142	VSS	1838.0	-595.0	222	NC	8124.9	-610.0
63	PD9	-5470.5	-610.0	143	CS#	1913.0	-595.0	223	NC	8179.9	-585.0
64	PD8	-5313.8	-610.0	144	RES#	1988.0	-595.0	224	NC	8219.9	-585.0
65	PD7	-5096.5	-610.0	145	D/C#	2063.0	-595.0	225	COM65	8259.9	-585.0
66	PD6	-4939.9	-610.0	146	VSS	2138.0	-595.0	226	COM64	8299.9	-585.0
67	PD5	-4722.6	-610.0	147	R/W#	2213.0	-595.0	227	COM63	8339.9	-585.0
68	PD4	-4565.9	-610.0	148	E	2288.0	-595.0	228	COM62	8379.9	-585.0
69	PD3	-4348.6	-610.0	149	VDDIO	2363.0	-595.0	229	COM61	8419.9	-585.0
70	PD2	-4191.9	-610.0	150	D0	2438.0	-595.0	230	COM60	8459.9	-585.0
71	PD1	-3974.7	-610.0	151	D1	2513.0	-595.0	231	COM59	8499.9	-585.0
72	PD0	-3818.0	-610.0	152	D2	2588.0	-595.0	232	COM58	8539.9	-585.0
73	HSYNC	-3600.7	-610.0	153	D3	2663.0	-595.0	233	COM57	8579.9	-585.0
74	VSYNC	-3444.0	-610.0	154	D4	2738.0	-595.0	234	COM56	8619.9	-585.0
75	DOTCLK	-3226.7	-610.0	155	D5	2813.0	-595.0	235	COM55	8659.9	-585.0
76	VSS	-3112.0	-610.0	156	D6	2888.0	-595.0	236	COM54	8699.9	-585.0
77	VSSB	-3037.0	-595.0	157	D7	2963.0	-595.0	237	COM53	8739.9	-585.0
78	VSSB	-2962.0	-595.0	158	D8	3038.0	-595.0	238	COM52	8779.9	-585.0
79	GDR	-2887.0	-595.0	159	D9	3113.0	-595.0	239	COM51	8819.9	-585.0
80	GDR	-2812.0	-595.0	160	D10	3188.0	-595.0	240	COM50	8859.9	-585.0

Pad no.	Pad Name	X-Axis	Y-Axis	Pad no.	Pad Name	X-Axis	Y-Axis	Pad no.	Pad Name	X-Axis	Y-Axis
241	COM49	8899.9	-585.0	321	SA8	8737.4	585.0	401	SC34	5531.0	585.0
242	COM48	8939.9	-585.0	322	SB8	8697.4	585.0	402	SA35	5491.0	585.0
243	COM47	8979.9	-585.0	323	SC8	8657.3	585.0	403	SB35	5450.9	585.0
244	COM46	9019.9	-585.0	324	SA9	8617.2	585.0	404	SC35	5410.8	585.0
245	COM45	9059.9	-585.0	325	SB9	8577.1	585.0	405	SA36	5370.7	585.0
246	COM44	9099.9	-585.0	326	SC9	8537.0	585.0	406	SB36	5330.6	585.0
247	COM43	9139.9	-585.0	327	SA10	8497.0	585.0	407	SC36	5290.6	585.0
248	COM42	9179.9	-585.0	328	SB10	8456.9	585.0	408	SA37	5250.5	585.0
249	COM41	9219.9	-585.0	329	SC10	8416.8	585.0	409	SB37	5210.4	585.0
250	COM40	9259.9	-585.0	330	SA11	8376.7	585.0	410	SC37	5170.3	585.0
251	COM39	9299.9	-585.0	331	SB11	8336.6	585.0	411	SA38	5130.2	585.0
252	COM38	9339.9	-585.0	332	SC11	8296.6	585.0	412	SB38	5090.2	585.0
253	COM37	9379.9	-585.0	333	SA12	8256.5	585.0	413	SC38	5050.1	585.0
254	COM36	9419.9	-585.0	334	SB12	8216.4	585.0	414	SA39	5010.0	585.0
255	COM35	9459.9	-585.0	335	SC12	8176.3	585.0	415	SB39	4969.9	585.0
256	COM34	9499.9	-585.0	336	SA13	8136.2	585.0	416	SC39	4929.8	585.0
257	COM33	9539.9	-585.0	337	SB13	8096.2	585.0	417	SA40	4889.8	585.0
258	COM32	9579.9	-585.0	338	SC13	8056.1	585.0	418	SB40	4849.7	585.0
259	COM31	9619.9	-585.0	339	SA14	8016.0	585.0	419	SC40	4809.6	585.0
260	COM30	9659.9	-585.0	340	SB14	7975.9	585.0	420	SA41	4769.5	585.0
261	COM29	9699.9	-585.0	341	SC14	7935.8	585.0	421	SB41	4729.4	585.0
262	NC	9739.9	-585.0	342	SA15	7895.8	585.0	422	SC41	4689.4	585.0
263	NC	9779.9	-585.0	343	SB15	7855.7	585.0	423	SA42	4649.3	585.0
264	NC	10101.4	-620.0	344	SC15	7815.6	585.0	424	SB42	4609.2	585.0
265	COM28	10101.4	-552.5	345	SA16	7775.5	585.0	425	SC42	4569.1	585.0
266	COM27	10101.4	-512.5	346	SB16	7735.4	585.0	426	SA43	4529.0	585.0
267	COM26	10101.4	-472.5	347	SC16	7695.4	585.0	427	SB43	4489.0	585.0
268	COM25	10101.4	-432.5	348	SA17	7655.3	585.0	428	SC43	4448.9	585.0
269	COM24	10101.4	-392.5	349	SB17	7615.2	585.0	429	SA44	4408.8	585.0
270	COM23	10101.4	-352.5	350	SC17	7575.1	585.0	430	SB44	4368.7	585.0
271	COM22	10101.4	-312.5	351	SA18	7535.0	585.0	431	SC44	4328.6	585.0
272	COM21	10101.4	-272.5	352	SB18	7495.0	585.0	432	SA45	4288.6	585.0
273	COM20	10101.4	-232.5	353	SC18	7454.9	585.0	433	SB45	4248.5	585.0
274	COM19	10101.4	-192.5	354	SA19	7414.8	585.0	434	SC45	4208.4	585.0
275	COM18	10101.4	-152.5	355	SB19	7374.7	585.0	435	SA46	4168.3	585.0
276	COM17	10101.4	-112.5	356	SC19	7334.6	585.0	436	SB46	4128.2	585.0
277	COM16	10101.4	-72.5	357	SA20	7294.6	585.0	437	SC46	4088.2	585.0
278	COM15	10101.4	-32.5	358	SB20	7254.5	585.0	438	SA47	4048.1	585.0
279	COM14	10101.4	7.5	359	SC20	7214.4	585.0	439	SB47	4008.0	585.0
280	COM13	10101.4	47.5	360	SA21	7174.3	585.0	440	SC47	3967.9	585.0
281	COM12	10101.4	87.5	361	SB21	7134.2	585.0	441	SA48	3927.8	585.0
282	COM11	10101.4	127.5	362	SC21	7094.2	585.0	442	SB48	3887.8	585.0
283	COM10	10101.4	167.5	363	SA22	7054.1	585.0	443	SC48	3847.7	585.0
284	COM9	10101.4	207.5	364	SB22	7014.0	585.0	444	SA49	3807.6	585.0
285	COM8	10101.4	247.5	365	SC22	6973.9	585.0	445	SB49	3767.5	585.0
286	COM7	10101.4	287.5	366	SA23	6933.8	585.0	446	SC49	3727.4	585.0
287	COM6	10101.4	327.5	367	SB23	6893.8	585.0	447	SA50	3687.4	585.0
288	COM5	10101.4	367.5	368	SC23	6853.7	585.0	448	SB50	3647.3	585.0
289	COM4	10101.4	407.5	369	SA24	6813.6	585.0	449	SC50	3607.2	585.0
290	COM3	10101.4	447.5	370	SB24	6773.5	585.0	450	SA51	3567.1	585.0
291	COM2	10101.4	487.5	371	SC24	6733.4	585.0	451	SB51	3527.0	585.0
292	COM1	10101.4	527.5	372	SA25	6693.4	585.0	452	SC51	3487.0	585.0
293	COM0	10101.4	567.5	373	SB25	6653.3	585.0	453	SA52	3446.9	585.0
294	NC	10101.4	620.0	374	SC25	6613.2	585.0	454	SB52	3406.8	585.0
295	NC	9780.2	585.0	375	SA26	6573.1	585.0	455	SC52	3366.7	585.0
296	NC	9740.2	585.0	376	SB26	6533.0	585.0	456	SA53	3326.6	585.0
297	SA0	9699.4	585.0	377	SC26	6493.0	585.0	457	SB53	3286.6	585.0
298	SB0	9659.3	585.0	378	SA27	6452.9	585.0	458	SC53	3246.5	585.0
299	SC0	9619.2	585.0	379	SB27	6412.8	585.0	459	SA54	3206.4	585.0
300	SA1	9579.1	585.0	380	SC27	6372.7	585.0	460	SB54	3166.3	585.0
301	SB1	9539.0	585.0	381	SA28	6332.6	585.0	461	SC54	3126.2	585.0
302	SC1	9499.0	585.0	382	SB28	6292.6	585.0	462	SA55	3086.2	585.0
303	SA2	9458.9	585.0	383	SC28	6252.5	585.0	463	SB55	3046.1	585.0
304	SB2	9418.8	585.0	384	SA29	6212.4	585.0	464	SC55	3006.0	585.0
305	SC2	9378.7	585.0	385	SB29	6172.3	585.0	465	SA56	2965.9	585.0
306	SA3	9338.6	585.0	386	SC29	6132.2	585.0	466	SB56	2925.8	585.0
307	SB3	9298.6	585.0	387	SA30	6092.2	585.0	467	SC56	2885.8	585.0
308	SC3	9258.5	585.0	388	SB30	6052.1	585.0	468	SA57	2845.7	585.0
309	SA4	9218.4	585.0	389	SC30	6012.0	585.0	469	SB57	2805.6	585.0
310	SB4	9178.3	585.0	390	SA31	5971.9	585.0	470	SC57	2765.5	585.0
311	SC4	9138.2	585.0	391	SB31	5931.8	585.0	471	SA58	2725.4	585.0
312	SA5	9098.2	585.0	392	SC31	5891.8	585.0	472	SB58	2685.4	585.0
313	SB5	9058.1	585.0	393	SA32	5851.7	585.0	473	SC58	2645.3	585.0
314	SC5	9018.0	585.0	394	SB32	5811.6	585.0	474	SA59	2605.2	585.0
315	SA6	8977.9	585.0	395	SC32	5771.5	585.0	475	SB59	2565.1	585.0
316	SB6	8937.8	585.0	396	SA33	5731.4	585.0	476	SC59	2525.0	585.0
317	SC6	8897.8	585.0	397	SB33	5691.4	585.0	477	SA60	2485.0	585.0
318	SA7	8857.7	585.0	398	SC33	5651.3	585.0	478	SB60	2444.9	585.0
319	SB7	8817.6	585.0	399	SA34	5611.2	585.0	479	SC60	2404.8	585.0
320	SC7	8777.5	585.0	400	SB34	5571.1	585.0	480	SA61	2364.7	585.0

Pad no.	Pad Name	X-Axis	Y-Axis
481	SB61	2324.6	585.0
482	SC61	2284.6	585.0
483	SA62	2244.5	585.0
484	SB62	2204.4	585.0
485	SC62	2164.3	585.0
486	SA63	2124.2	585.0
487	SB63	2084.2	585.0
488	SC63	2044.1	585.0
489	SA64	2004.0	585.0
490	SB64	1963.9	585.0
491	SC64	1923.8	585.0
492	SA65	1883.8	585.0
493	SB65	1843.7	585.0
494	SC65	1803.6	585.0
495	SA66	1763.5	585.0
496	SB66	1723.4	585.0
497	SC66	1683.4	585.0
498	SA67	1643.3	585.0
499	SB67	1603.2	585.0
500	SC67	1563.1	585.0
501	SA68	1523.0	585.0
502	SB68	1483.0	585.0
503	SC68	1442.9	585.0
504	SA69	1402.8	585.0
505	SB69	1362.7	585.0
506	SC69	1322.6	585.0
507	SA70	1282.6	585.0
508	SB70	1242.5	585.0
509	SC70	1202.4	585.0
510	SA71	1162.3	585.0
511	SB71	1122.2	585.0
512	SC71	1082.2	585.0
513	SA72	1042.1	585.0
514	SB72	1002.0	585.0
515	SC72	961.9	585.0
516	SA73	921.8	585.0
517	SB73	881.8	585.0
518	SC73	841.7	585.0
519	SA74	801.6	585.0
520	SB74	761.5	585.0
521	SC74	721.4	585.0
522	SA75	681.4	585.0
523	SB75	641.3	585.0
524	SC75	601.2	585.0
525	SA76	561.1	585.0
526	SB76	521.0	585.0
527	SC76	481.0	585.0
528	SA77	440.9	585.0
529	SB77	400.8	585.0
530	SC77	360.7	585.0
531	SA78	320.6	585.0
532	SB78	280.6	585.0
533	SC78	240.5	585.0
534	SA79	200.4	585.0
535	SB79	160.3	585.0
536	SC79	120.2	585.0
537	NC	80.2	585.0
538	NC	-80.2	585.0
539	SA80	-120.3	585.0
540	SB80	-160.3	585.0
541	SC80	-200.4	585.0
542	SA81	-240.5	585.0
543	SB81	-280.6	585.0
544	SC81	-320.7	585.0
545	SA82	-360.7	585.0
546	SB82	-400.8	585.0
547	SC82	-440.9	585.0
548	SA83	-481.0	585.0
549	SB83	-521.1	585.0
550	SC83	-561.1	585.0
551	SA84	-601.2	585.0
552	SB84	-641.3	585.0
553	SC84	-681.4	585.0
554	SA85	-721.5	585.0
555	SB85	-761.5	585.0
556	SC85	-801.6	585.0
557	SA86	-841.7	585.0
558	SB86	-881.8	585.0
559	SC86	-921.9	585.0
560	SA87	-961.9	585.0

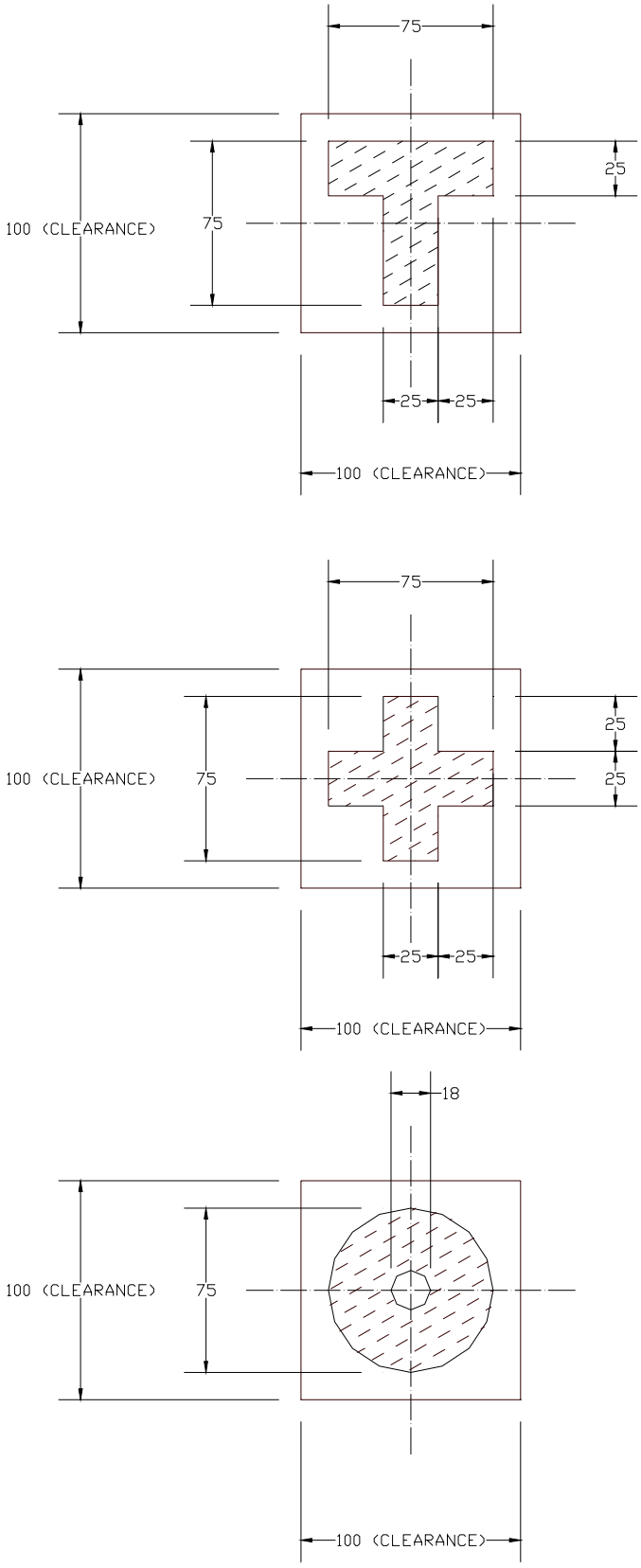
Pad no.	Pad Name	X-Axis	Y-Axis
561	SB87	-1002.0	585.0
562	SC87	-1042.1	585.0
563	SA88	-1082.2	585.0
564	SB88	-1122.3	585.0
565	SC88	-1162.3	585.0
566	SA89	-1202.4	585.0
567	SB89	-1242.5	585.0
568	SC89	-1282.6	585.0
569	SA90	-1322.7	585.0
570	SB90	-1362.7	585.0
571	SC90	-1402.8	585.0
572	SA91	-1442.9	585.0
573	SB91	-1483.0	585.0
574	SC91	-1523.1	585.0
575	SA92	-1563.1	585.0
576	SB92	-1603.2	585.0
577	SC92	-1643.3	585.0
578	SA93	-1683.4	585.0
579	SB93	-1723.5	585.0
580	SC93	-1763.5	585.0
581	SA94	-1803.6	585.0
582	SB94	-1843.7	585.0
583	SC94	-1883.8	585.0
584	SA95	-1923.9	585.0
585	SB95	-1963.9	585.0
586	SC95	-2004.0	585.0
587	SA96	-2044.1	585.0
588	SB96	-2084.2	585.0
589	SC96	-2124.3	585.0
590	SA97	-2164.3	585.0
591	SB97	-2204.4	585.0
592	SC97	-2244.5	585.0
593	SA98	-2284.6	585.0
594	SB98	-2324.7	585.0
595	SC98	-2364.7	585.0
596	SA99	-2404.8	585.0
597	SB99	-2444.9	585.0
598	SC99	-2485.0	585.0
599	SA100	-2525.1	585.0
600	SB100	-2565.1	585.0
601	SC100	-2605.2	585.0
602	SA101	-2645.3	585.0
603	SB101	-2685.4	585.0
604	SC101	-2725.5	585.0
605	SA102	-2765.5	585.0
606	SB102	-2805.6	585.0
607	SC102	-2845.7	585.0
608	SA103	-2885.8	585.0
609	SB103	-2925.9	585.0
610	SC103	-2965.9	585.0
611	SA104	-3006.0	585.0
612	SB104	-3046.1	585.0
613	SC104	-3086.2	585.0
614	SA105	-3126.3	585.0
615	SB105	-3166.3	585.0
616	SC105	-3206.4	585.0
617	SA106	-3246.5	585.0
618	SB106	-3286.6	585.0
619	SC106	-3326.7	585.0
620	SA107	-3366.7	585.0
621	SB107	-3406.8	585.0
622	SC107	-3446.9	585.0
623	SA108	-3487.0	585.0
624	SB108	-3527.1	585.0
625	SC108	-3567.1	585.0
626	SA109	-3607.2	585.0
627	SB109	-3647.3	585.0
628	SC109	-3687.4	585.0
629	SA110	-3727.5	585.0
630	SB110	-3767.5	585.0
631	SC110	-3807.6	585.0
632	SA111	-3847.7	585.0
633	SB111	-3887.8	585.0
634	SC111	-3927.9	585.0
635	SA112	-3967.9	585.0
636	SB112	-4008.0	585.0
637	SC112	-4048.1	585.0
638	SA113	-4088.2	585.0
639	SB113	-4128.3	585.0
640	SC113	-4168.3	585.0

Pad no.	Pad Name	X-Axis	Y-Axis
641	SA114	-4208.4	585.0
642	SB114	-4248.5	585.0
643	SC114	-4288.6	585.0
644	SA115	-4328.7	585.0
645	SB115	-4368.7	585.0
646	SC115	-4408.8	585.0
647	SA116	-4448.9	585.0
648	SB116	-4489.0	585.0
649	SC116	-4529.1	585.0
650	SA117	-4569.1	585.0
651	SB117	-4609.2	585.0
652	SC117	-4649.3	585.0
653	SA118	-4689.4	585.0
654	SB118	-4729.5	585.0
655	SC118	-4769.5	585.0
656	SA119	-4809.6	585.0
657	SB119	-4849.7	585.0
658	SC119	-4889.8	585.0
659	SA120	-4929.9	585.0
660	SB120	-4969.9	585.0
661	SC120	-5010.0	585.0
662	SA121	-5050.1	585.0
663	SB121	-5090.2	585.0
664	SC121	-5130.3	585.0
665	SA122	-5170.3	585.0
666	SB122	-5210.4	585.0
667	SC122	-5250.5	585.0
668	SA123	-5290.6	585.0
669	SB123	-5330.7	585.0
670	SC123	-5370.7	585.0
671	SA124	-5410.8	585.0
672	SB124	-5450.9	585.0
673	SC124	-5491.0	585.0
674	SA125	-5531.1	585.0
675	SB125	-5571.1	585.0
676	SC125	-5611.2	585.0
677	SA126	-5651.3	585.0
678	SB126	-5691.4	585.0
679	SC126	-5731.5	585.0
680	SA127	-5771.5	585.0
681	SB127	-5811.6	585.0
682	SC127	-5851.7	585.0
683	SA128	-5891.8	585.0
684	SB128	-5931.9	585.0
685	SC128	-5971.9	585.0
686	SA129	-6012.0	585.0
687	SB129	-6052.1	585.0
688	SC129	-6092.2	585.0
689	SA130	-6132.3	585.0
690	SB130	-6172.3	585.0
691	SC130	-6212.4	585.0
692	SA131	-6252.5	585.0
693	SB131	-6292.6	585.0
694	SC131	-6332.7	585.0
695	SA132	-6372.7	585.0
696	SB132	-6412.8	585.0
697	SC132	-6452.9	585.0
698	SA133	-6493.0	585.0
699	SB133	-6533.1	585.0
700	SC133	-6573.1	585.0
701	SA134	-6613.2	585.0
702	SB134	-6653.3	585.0
703	SC134	-6693.4	585.0
704	SA135	-6733.5	585.0
705	SB135	-6773.5	585.0
706	SC135	-6813.6	585.0
707	SA136	-6853.7	585.0
708	SB136	-6893.8	585.0
709	SC136	-6933.9	585.0
710	SA137	-6973.9	585.0
711	SB137	-7014.0	585.0
712	SC137	-7054.1	585.0
713	SA138	-7094.2	585.0
714	SB138	-7134.3	585.0
715	SC138	-7174.3	585.0
716	SA139	-7214.4	585.0
717	SB139	-7254.5	585.0
718	SC139	-7294.6	585.0
719	SA140	-7334.7	585.0
720	SB140	-7374.7	585.0

Pad no.	Pad Name	X-Axis	Y-Axis
721	SC140	-7414.8	585.0
722	SA141	-7454.9	585.0
723	SB141	-7495.0	585.0
724	SC141	-7535.1	585.0
725	SA142	-7575.1	585.0
726	SB142	-7615.2	585.0
727	SC142	-7655.3	585.0
728	SA143	-7695.4	585.0
729	SB143	-7735.5	585.0
730	SC143	-7775.5	585.0
731	SA144	-7815.6	585.0
732	SB144	-7855.7	585.0
733	SC144	-7895.8	585.0
734	SA145	-7935.9	585.0
735	SB145	-7975.9	585.0
736	SC145	-8016.0	585.0
737	SA146	-8056.1	585.0
738	SB146	-8096.2	585.0
739	SC146	-8136.3	585.0
740	SA147	-8176.3	585.0
741	SB147	-8216.4	585.0
742	SC147	-8256.5	585.0
743	SA148	-8296.6	585.0
744	SB148	-8336.7	585.0
745	SC148	-8376.7	585.0
746	SA149	-8416.8	585.0
747	SB149	-8456.9	585.0
748	SC149	-8497.0	585.0
749	SA150	-8537.1	585.0
750	SB150	-8577.1	585.0
751	SC150	-8617.2	585.0
752	SA151	-8657.3	585.0
753	SB151	-8697.4	585.0
754	SC151	-8737.5	585.0
755	SA152	-8777.5	585.0
756	SB152	-8817.6	585.0
757	SC152	-8857.7	585.0
758	SA153	-8897.8	585.0
759	SB153	-8937.9	585.0
760	SC153	-8977.9	585.0
761	SA154	-9018.0	585.0
762	SB154	-9058.1	585.0
763	SC154	-9098.2	585.0
764	SA155	-9138.3	585.0
765	SB155	-9178.3	585.0
766	SC155	-9218.4	585.0
767	SA156	-9258.5	585.0
768	SB156	-9298.6	585.0
769	SC156	-9338.7	585.0
770	SA157	-9378.7	585.0
771	SB157	-9418.8	585.0
772	SC157	-9458.9	585.0
773	SA158	-9499.0	585.0
774	SB158	-9539.1	585.0
775	SC158	-9579.1	585.0
776	SA159	-9619.2	585.0
777	SB159	-9659.3	585.0
778	SC159	-9699.4	585.0
779	NC	-9740.2	585.0
780	NC	-9780.2	585.0
781	NC	-10101.4	620.0
782	COM66	-10101.4	567.5
783	COM67	-10101.4	527.5
784	COM68	-10101.4	487.5
785	COM69	-10101.4	447.5
786	COM70	-10101.4	407.5
787	COM71	-10101.4	367.5
788	COM72	-10101.4	327.5
789	COM73	-10101.4	287.5
790	COM74	-10101.4	247.5
791	COM75	-10101.4	207.5
792	COM76	-10101.4	167.5
793	COM77	-10101.4	127.5
794	COM78	-10101.4	87.5
795	COM79	-10101.4	47.5
796	COM80	-10101.4	7.5
797	COM81	-10101.4	-32.5
798	COM82	-10101.4	-72.5
799	COM83	-10101.4	-112.5
800	COM84	-10101.4	-152.5

Pad no.	Pad Name	X-Axis	Y-Axis
801	COM85	-10101.4	-192.5
802	COM86	-10101.4	-232.5
803	COM87	-10101.4	-272.5
804	COM88	-10101.4	-312.5
805	COM89	-10101.4	-352.5
806	COM90	-10101.4	-392.5
807	COM91	-10101.4	-432.5
808	COM92	-10101.4	-472.5
809	COM93	-10101.4	-512.5
810	COM94	-10101.4	-552.5

Figure 5-2: SSD1335Z Alignment Mark Dimensions



6 PIN ASSIGNMRNT

6.1 SSD1353U7R1 pin assignment

Table 6-1 : SSD1353U7R1 Pin assignment

Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name	Pad No.	Pad Name
1	NC	81	COM61	161	SA148	241	SB121	321	SC94
2	VCC	82	COM59	162	SC147	242	SA121	322	SB94
3	VCOMH	83	COM57	163	SB147	243	SC120	323	SA94
4	VLSS	84	COM55	164	SA147	244	SB120	324	SC93
5	VSS	85	COM53	165	SC146	245	SA120	325	SB93
6	IREF	86	COM51	166	SB146	246	SC119	326	SA93
7	D17	87	COM49	167	SA146	247	SB119	327	SC92
8	D16	88	COM47	168	SC145	248	SA119	328	SB92
9	D15	89	COM45	169	SB145	249	SC118	329	SA92
10	D14	90	COM43	170	SA145	250	SB118	330	SC91
11	D13	91	COM41	171	SC144	251	SA118	331	SB91
12	D12	92	COM39	172	SB144	252	SC117	332	SA91
13	D11	93	COM37	173	SA144	253	SB117	333	SC90
14	D10	94	COM35	174	SC143	254	SA117	334	SB90
15	D9	95	COM33	175	SB143	255	SC116	335	SA90
16	D8	96	COM31	176	SA143	256	SB116	336	SC89
17	D7	97	COM29	177	SC142	257	SA116	337	SB89
18	D6	98	COM27	178	SB142	258	SC115	338	SA89
19	D5	99	COM25	179	SA142	259	SB115	339	SC88
20	D4	100	COM23	180	SC141	260	SA115	340	SB88
21	D3	101	COM21	181	SB141	261	SC114	341	SA88
22	D2	102	COM19	182	SA141	262	SB114	342	SC87
23	D1	103	COM17	183	SC140	263	SA114	343	SB87
24	D0	104	COM15	184	SB140	264	SC113	344	SA87
25	E	105	COM13	185	SA140	265	SB113	345	SC86
26	R/W#	106	COM11	186	SC139	266	SA113	346	SB86
27	D/C#	107	COM9	187	SB139	267	SC112	347	SA86
28	RESB	108	COM7	188	SA139	268	SB112	348	SC85
29	CSB	109	COM5	189	SC138	269	SA112	349	SB85
30	FR	110	COM3	190	SB138	270	SC111	350	SA85
31	BS3	111	COM1	191	SA138	271	SB111	351	SC84
32	BS2	112	NC	192	SC137	272	SA111	352	SB84
33	BS1	113	NC	193	SB137	273	SC110	353	SA84
34	BS0	114	NC	194	SA137	274	SB110	354	SC83
35	REGVDD	115	NC	195	SC136	275	SA110	355	SB83
36	VDDIO	116	NC	196	SB136	276	SC109	356	SA83
37	VDD	117	NC	197	SA136	277	SB109	357	SC82
38	VPP	118	NC	198	SC135	278	SA109	358	SB82
39	VCI	119	NC	199	SB135	279	SC108	359	SA82
40	VSL	120	NC	200	SA135	280	SB108	360	SC81
41	VBREF	121	NC	201	SC134	281	SA108	361	SB81
42	VSS	122	NC	202	SB134	282	SC107	362	SA81
43	VLSS	123	NC	203	SA134	283	SB107	363	SC80
44	VCOMH	124	NC	204	SC133	284	SA107	364	SB80
45	VCC	125	NC	205	SB133	285	SC106	365	SA80
46	NC	126	SC159	206	SA133	286	SB106	366	SC79
47	NC	127	SB159	207	SC132	287	SA106	367	SB79
48	COM127	128	SA159	208	SB132	288	SC105	368	SA79
49	COM125	129	SC158	209	SA132	289	SB105	369	SC78
50	COM123	130	SB158	210	SC131	290	SA105	370	SB78
51	COM121	131	SA158	211	SB131	291	SC104	371	SA78
52	COM119	132	SC157	212	SA131	292	SB104	372	SC77
53	COM117	133	SB157	213	SC130	293	SA104	373	SB77
54	COM115	134	SA157	214	SB130	294	SC103	374	SA77
55	COM113	135	SC156	215	SA130	295	SB103	375	SC76
56	COM111	136	SB156	216	SC129	296	SA103	376	SB76
57	COM109	137	SA156	217	SB129	297	SC102	377	SA76
58	COM107	138	SC155	218	SA129	298	SB102	378	SC75
59	COM105	139	SB155	219	SC128	299	SA102	379	SB75
60	COM103	140	SA155	220	SB128	300	SC101	380	SA75
61	COM101	141	SC154	221	SA128	301	SB101	381	SC74
62	COM99	142	SB154	222	SC127	302	SA101	382	SB74
63	COM97	143	SA154	223	SB127	303	SC100	383	SA74
64	COM95	144	SC153	224	SA127	304	SB100	384	SC73
65	COM93	145	SB153	225	SC126	305	SA100	385	SB73
66	COM91	146	SA153	226	SB126	306	SC99	386	SA73
67	COM89	147	SC152	227	SA126	307	SB99	387	SC72
68	COM87	148	SB152	228	SC125	308	SA99	388	SB72
69	COM85	149	SA152	229	SB125	309	SC98	389	SA72
70	COM83	150	SC151	230	SA125	310	SB98	390	SC71
71	COM81	151	SB151	231	SC124	311	SA98	391	SB71
72	COM79	152	SA151	232	SB124	312	SC97	392	SA71
73	COM77	153	SC150	233	SA124	313	SB97	393	SC70
74	COM75	154	SB150	234	SC123	314	SA97	394	SB70
75	COM73	155	SA150	235	SB123	315	SC96	395	SA70
76	COM71	156	SC149	236	SA123	316	SB96	396	SC69
77	COM69	157	SB149	237	SC122	317	SA96	397	SB69
78	COM67	158	SA149	238	SB122	318	SC95	398	SA69
79	COM65	159	SC148	239	SA122	319	SB95	399	SC68
80	COM63	160	SB148	240	SC121	320	SA95	400	SB68

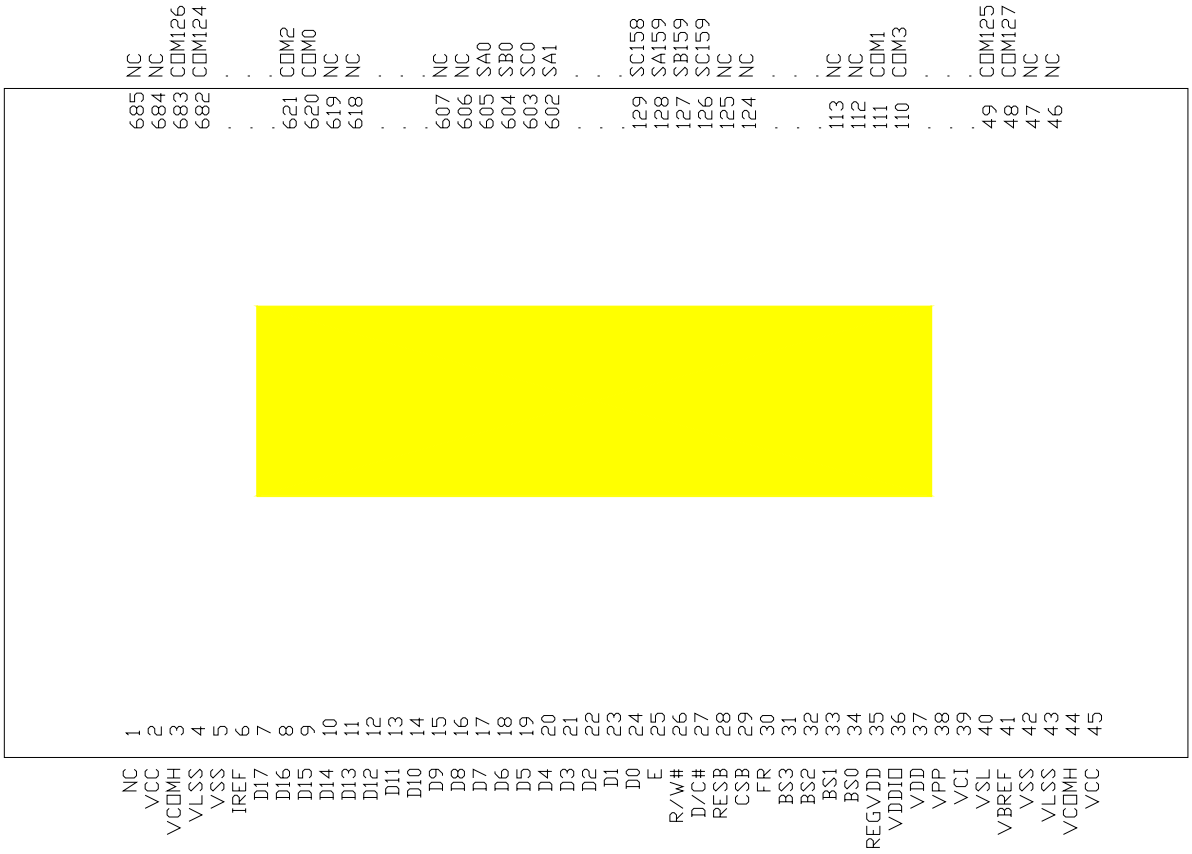
Pad No.	Pad Name
401	SA68
402	SC67
403	SB67
404	SA67
405	SC66
406	SB66
407	SA66
408	SC65
409	SB65
410	SA65
411	SC64
412	SB64
413	SA64
414	SC63
415	SB63
416	SA63
417	SC62
418	SB62
419	SA62
420	SC61
421	SB61
422	SA61
423	SC60
424	SB60
425	SA60
426	SC59
427	SB59
428	SA59
429	SC58
430	SB58
431	SA58
432	SC57
433	SB57
434	SA57
435	SC56
436	SB56
437	SA56
438	SC55
439	SB55
440	SA55
441	SC54
442	SB54
443	SA54
444	SC53
445	SB53
446	SA53
447	SC52
448	SB52
449	SA52
450	SC51
451	SB51
452	SA51
453	SC50
454	SB50
455	SA50
456	SC49
457	SB49
458	SA49
459	SC48
460	SB48
461	SA48
462	SC47
463	SB47
464	SA47
465	SC46
466	SB46
467	SA46
468	SC45
469	SB45
470	SA45
471	SC44
472	SB44
473	SA44
474	SC43
475	SB43
476	SA43
477	SC42
478	SB42
479	SA42
480	SC41

Pad No.	Pad Name
481	SB41
482	SA41
483	SC40
484	SB40
485	SA40
486	SC39
487	SB39
488	SA39
489	SC38
490	SB38
491	SA38
492	SC37
493	SB37
494	SA37
495	SC36
496	SB36
497	SA36
498	SC35
499	SB35
500	SA35
501	SC34
502	SB34
503	SA34
504	SC33
505	SB33
506	SA33
507	SC32
508	SB32
509	SA32
510	SC31
511	SB31
512	SA31
513	SC30
514	SB30
515	SA30
516	SC29
517	SB29
518	SA29
519	SC28
520	SB28
521	SA28
522	SC27
523	SB27
524	SA27
525	SC26
526	SB26
527	SA26
528	SC25
529	SB25
530	SA25
531	SC24
532	SB24
533	SA24
534	SC23
535	SB23
536	SA23
537	SC22
538	SB22
539	SA22
540	SC21
541	SB21
542	SA21
543	SC20
544	SB20
545	SA20
546	SC19
547	SB19
548	SA19
549	SC18
550	SB18
551	SA18
552	SC17
553	SB17
554	SA17
555	SC16
556	SB16
557	SA16
558	SC15
559	SB15
560	SA15

Pad No.	Pad Name
561	SC14
562	SB14
563	SA14
564	SC13
565	SB13
566	SA13
567	SC12
568	SB12
569	SA12
570	SC11
571	SB11
572	SA11
573	SC10
574	SB10
575	SA10
576	SC9
577	SB9
578	SA9
579	SC8
580	SB8
581	SA8
582	SC7
583	SB7
584	SA7
585	SC6
586	SB6
587	SA6
588	SC5
589	SB5
590	SA5
591	SC4
592	SB4
593	SA4
594	SC3
595	SB3
596	SA3
597	SC2
598	SB2
599	SA2
600	SC1
601	SB1
602	SA1
603	SC0
604	SB0
605	SA0
606	NC
607	NC
608	NC
609	NC
610	NC
611	NC
612	NC
613	NC
614	NC
615	NC
616	NC
617	NC
618	NC
619	NC
620	COM0
621	COM2
622	COM4
623	COM6
624	COM8
625	COM10
626	COM12
627	COM14
628	COM16
629	COM18
630	COM20
631	COM22
632	COM24
633	COM26
634	COM28
635	COM30
636	COM32
637	COM34
638	COM36
639	COM38
640	COM40

Pad No.	Pad Name
641	COM42
642	COM44
643	COM46
644	COM48
645	COM50
646	COM52
647	COM54
648	COM56
649	COM58
650	COM60
651	COM62
652	COM64
653	COM66
654	COM68
655	COM70
656	COM72
657	COM74
658	COM76
659	COM78
660	COM80
661	COM82
662	COM84
663	COM86
664	COM88
665	COM90
666	COM92
667	COM94
668	COM96
669	COM98
670	COM100
671	COM102
672	COM104
673	COM106
674	COM108
675	COM110
676	COM112
677	COM114
678	COM116
679	COM118
680	COM120
681	COM122
682	COM124
683	COM126
684	NC
685	NC

Figure 6-1 : SSD1353U7R1 Pin assignment



Note:
(1) COM sequence (Split) is under command setting: A0h, 60h (i.e. Bit A[5] =1 to Enable COM Split Odd Even) .

7 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
IO = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 7-1: SSD1353 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation Refer to Section 8.10 for details.
V_{DDIO}	P	Power supply for interface logic level. It should be match with the MCU interface voltage level. Refer to Section 8.10 for details.
V_{CI}	P	Low voltage power supply V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}. Refer to Section 8.10 for details.
V_{ACI}	P	Analog Low voltage power supply Connect to V_{CI}.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
V_{PP}	P	Power supply for programming OTP. In OTP programming, this pin is powered up to 7.5V. In operation mode (without programming OTP), this pin must be connected to V_{DD}.
V_{SS}	P	Ground pin
V_{LSS}	P	Analog system ground pin
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
REGVDD	I	Internal V_{DD} regulator selection pin. When this pin is pulled HIGH, internal V_{DD} regulator is enabled. When this pin is pulled LOW, external V_{DD} is used. Refer to Section 8.10 for details.
BGGND	P	This is a reserved pin. It should be connected to Ground.
PGGND	P	This is a reserved pin. It should be connected to Ground.
V_{DDB}	P	This is a reserved pin. It should be connected to V_{CI}.
V_{SSB}	P	This is a reserved pin. It should be connected to Ground
GDR	O	This is a reserved pin. It should be kept NC.
RESE	I	This is a reserved pin. It should be kept NC.
FB	I	This is a reserved pin. It should be kept NC.

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>V_{BREF}</td><td>O</td><td>This is an internal voltage reference pin. A capacitor should be connected to this pin and V_{SS}.</td></tr>
<tr><td>GPIO0</td><td>I/O</td><td>This is a reserved pin. It should be kept NC.</td></tr>
<tr><td>GPIO1</td><td>I/O</td><td>This is a reserved pin. It should be kept NC.</td></tr>
<tr><td>VSL</td><td>P</td><td>This is segment voltage reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground. (details depend on application)</td></tr>
<tr><td>BS[3:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table.
Table 7-2 : Bus Interface selection
<table><tr><th>BS[3:0]</th><th>Bus Interface Selection</th></tr><tr><td>0000</td><td>4 line SPI</td></tr><tr><td>0001</td><td>Invalid</td></tr><tr><td>0010</td><td>Invalid</td></tr><tr><td>0011</td><td>Invalid</td></tr><tr><td>0100</td><td>8-bit 6800 parallel</td></tr><tr><td>0101</td><td>16-bit 6800 parallel</td></tr><tr><td>0110</td><td>8-bit 8080 parallel</td></tr><tr><td>0111</td><td>16-bit 8080 parallel</td></tr><tr><td>1000</td><td>Invalid</td></tr><tr><td>1001</td><td>Invalid</td></tr><tr><td>1010</td><td>Invalid</td></tr><tr><td>1011</td><td>Invalid</td></tr><tr><td>1100</td><td>9-bit 6800 parallel</td></tr><tr><td>1101</td><td>18-bit 6800 parallel</td></tr><tr><td>1110</td><td>9-bit 8080 parallel</td></tr><tr><td>1111</td><td>18-bit 8080 parallel</td></tr></table>Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>I_{REF}</td><td>I</td><td>This pin is the segment output current reference pin.
A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to section 8.6 for the formula of resistor value from I_{REF}.</td></tr>
<tr><td>CL</td><td>I</td><td>External clock input pin.
When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.
When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal clock selection pin.
When this pin is pulled HIGH, internal oscillator is enabled (normal operation).
When this pin is pulled LOW, an external clock signal should be connected to CL.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
</table>

Pin Name	Pin Type	Description
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[17:0] will be interpreted as data. When the pin is pulled LOW, the content at D[17:0] will be interpreted as command.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.
D[17:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode) Refer to Section 8.1 for different bus interface connection.
PD[17:0]	I	These are reserved pins. They should be connected to Ground.
PDEN	I	This is a reserved pin. It should be connected to Ground.
VSYNC	I	This is a reserved pin. It should be connected to Ground.
HSYNC	I	This is a reserved pin. It should be connected to Ground.
DOTCLK	I	This is a reserved pin. It should be connected to Ground.
FR	O	Ram Write Synchronization output Details refer to section 8.5.2
SA[159:0] SB[159:0] SC[159:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF. The 480 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
COM[131:0]	I/O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface

SSD1353 MCU interface consist of 18 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[3:0] pins (refer to Table 7-2 for BS[3:0] pins setting)

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data / Command Interface																Control Signal				
	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8b / 8080	Tie Low										D[7:0]								RD#	WR#	CS#	D/C#	RES#
8b / 6800	Tie Low										D[7:0]								E	R/W#	CS#	D/C#	RES#
9b / 8080	Tie Low										D[8:0]								RD#	WR#	CS#	D/C#	RES#
9b / 6800	Tie Low										D[8:0]								E	R/W#	CS#	D/C#	RES#
16b / 8080	Tie Low										D[15:0]								RD#	WR#	CS#	D/C#	RES#
16b / 6800	Tie Low										D[15:0]								E	R/W#	CS#	D/C#	RES#
18b / 8080	D[17:0]																		RD#	WR#	CS#	D/C#	RES#
18b / 6800	D[17:0]																		E	R/W#	CS#	D/C#	RES#
SPI	Tie Low															NC	SDIN	SCLK	Tie Low		CS#	D/C#	RES#

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

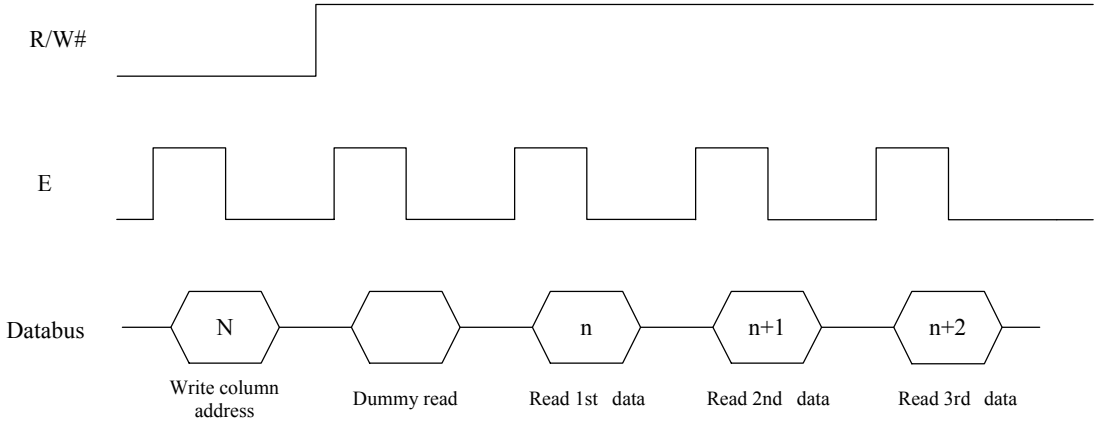
Table 8-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

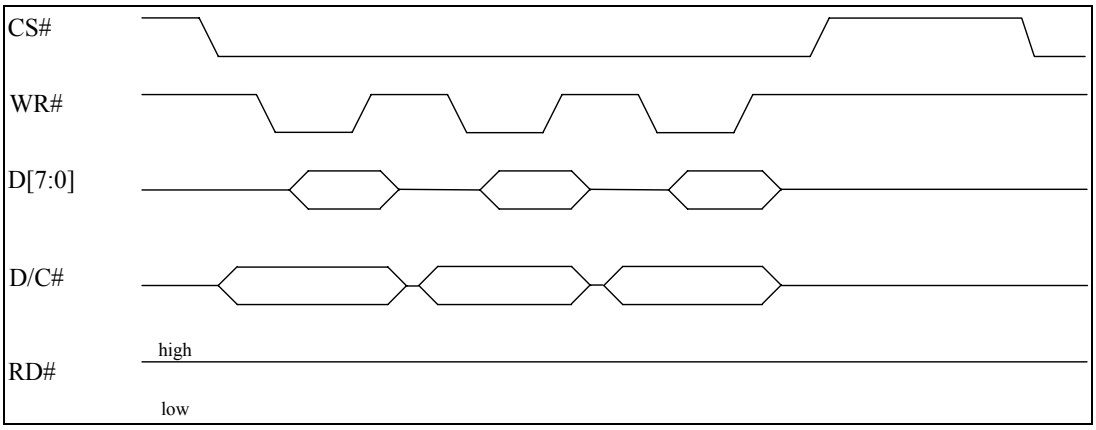


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

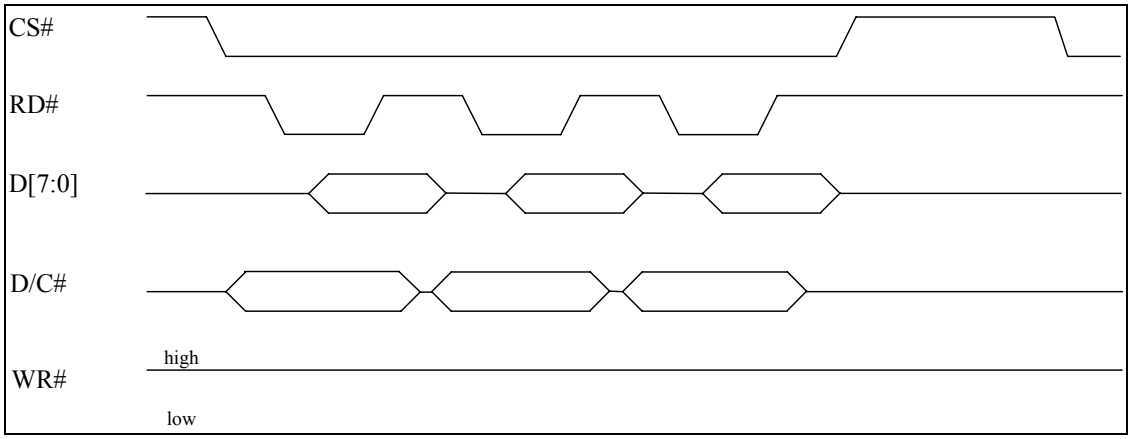


Table 8-3 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

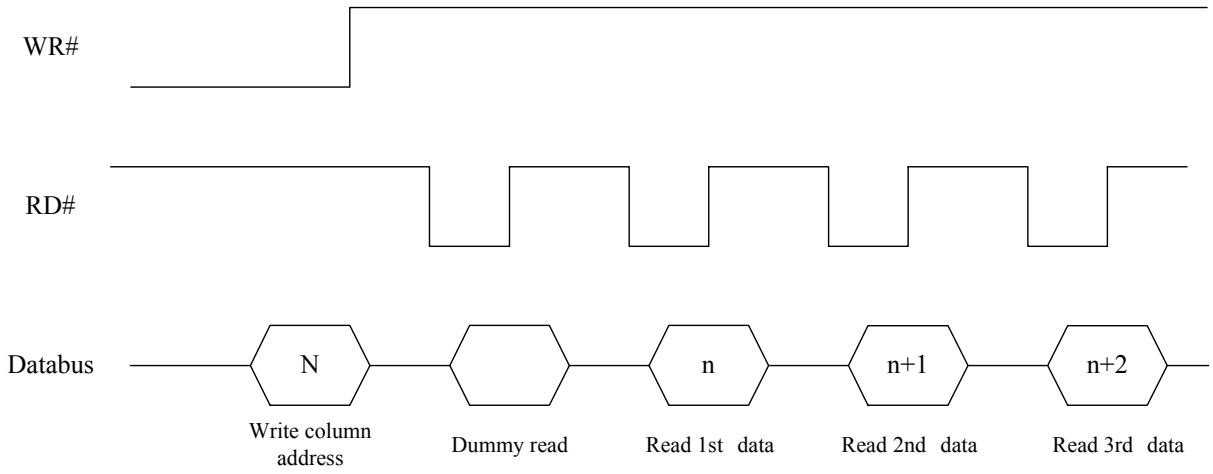
Table 8-4 : Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal
(4) Refer to Figure 13-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D17, E and R/W# can be connected to an external ground.

Table 8-5 : Control pins of Serial interface

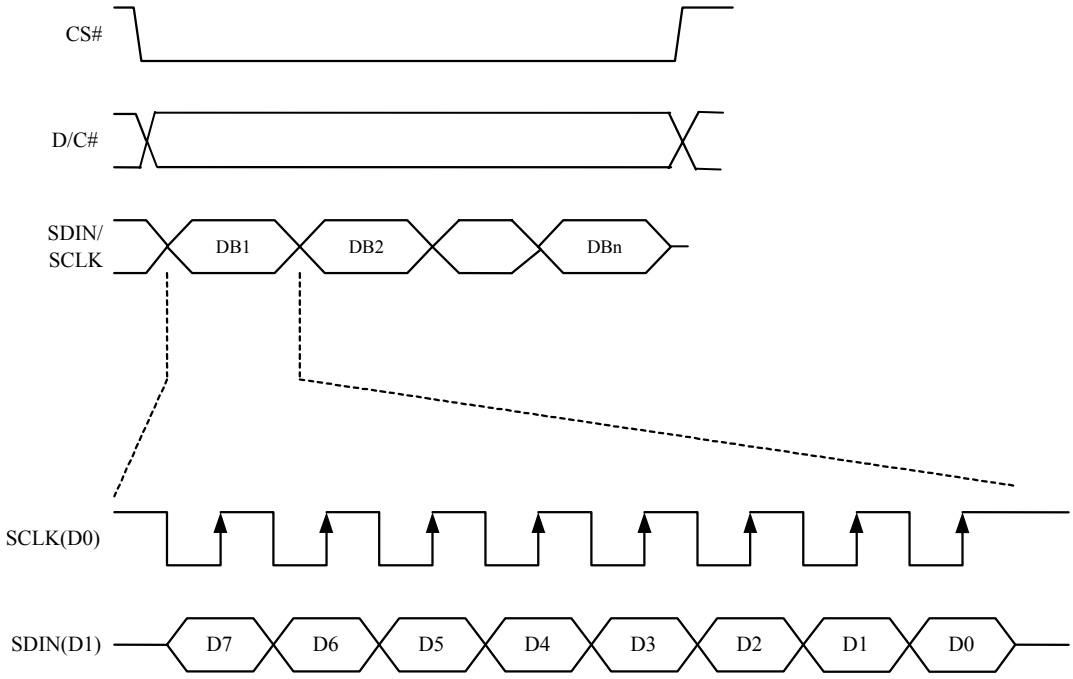
Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	Tie LOW	L	L
Write data	Tie LOW	Tie LOW	L	H

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in SPI mode



8.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 132 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Individual contrast control registers of color A, B, and C are set at 80h

8.3 GDDRAM

8.3.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 160 x 132 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown in Table 8-6

Table 8-6 : 262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	158	159			
	Remapped	159			158			157	.....	.....	1	0			
Color		A	B	C	A	B	C	A	.....	.....	C	A	B	C	
Data Format		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5	
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3	
Common Address		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2	
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0	Common
Normal	Remapped														output
0	131	6	6	6	6	6	6	6	.....	.....	6	6	6	6	COM0
1	130	6	6	6					.....	.....					COM1
2	129								.....	.....					COM2
3	128								.....	.....					COM3
4	127								.....	.....					COM4
5	126								.....	.....					COM5
6	125			no of bits in this cell					.....	.....					COM6
7	124								.....	.....					COM7
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:	
127	4								.....	.....					
128	3								.....	.....					COM128
129	2								.....	.....					COM129
130	1								.....	.....					COM130
131	0								.....	.....					COM131

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC158	SA159	SB159	SC159

8.3.2 Data bus to RAM mapping under different input mode

Table 8-7 : Data bus usage under different bus width and color depth mode

			Data bus																
Bus width	Color Depth	Input order	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	256		X	X	X	X	X	X	X	X	X	X	C_2	C_1	C_0	B_2	B_1	B_0	A_1	A_0
16 bits	65k		X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits	65k	1st	X	X	X	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits	262k	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	X	X	X	X	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0
		3rd	X	X	X	X	X	X	X	X	X	X	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 1	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 2	1st	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$
		3rd	X	X	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$
9 bits	262k	1st	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0
18 bits	262k		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

8.3.3 RAM mapping and Different color depth mode

At 262k color depth mode, color A, B, C are directly mapped to the RAM content. At 256 and 65k color mode, the RAM content will be filled up to 262k format.

Table 8-8 : 256 and 65k color mode mapping

	SCn						SBn						SAn					
262k color	C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0
65k color	C_4	C_3	C_2	C_1	C_0	$*C_4$	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0	$*A_4$
256 color	C_2	C_1	C_0	$*C_2$	$*C_2$	$*C_2$	B_2	B_1	B_0	$*B_2$	$*B_2$	$*B_2$	A_1	A_0	$*A_1$	$*A_1$	$*A_1$	$*A_1$

Note
(1) n = 0 ~ 159d
(2) bits with * are copied from corresponding bits in order to fill up 262K format.

8.4 Command Decoder

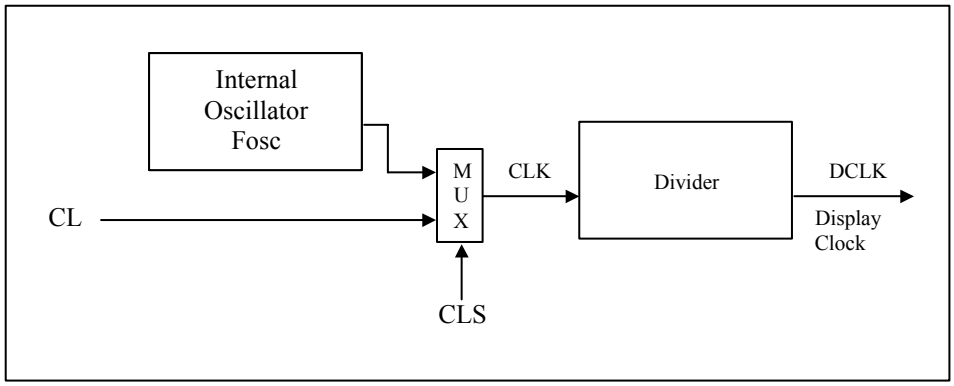
This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D17 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.5 Oscillator & Timing Generator

8.5.1 Oscillator

Figure 8-6 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 8-6). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

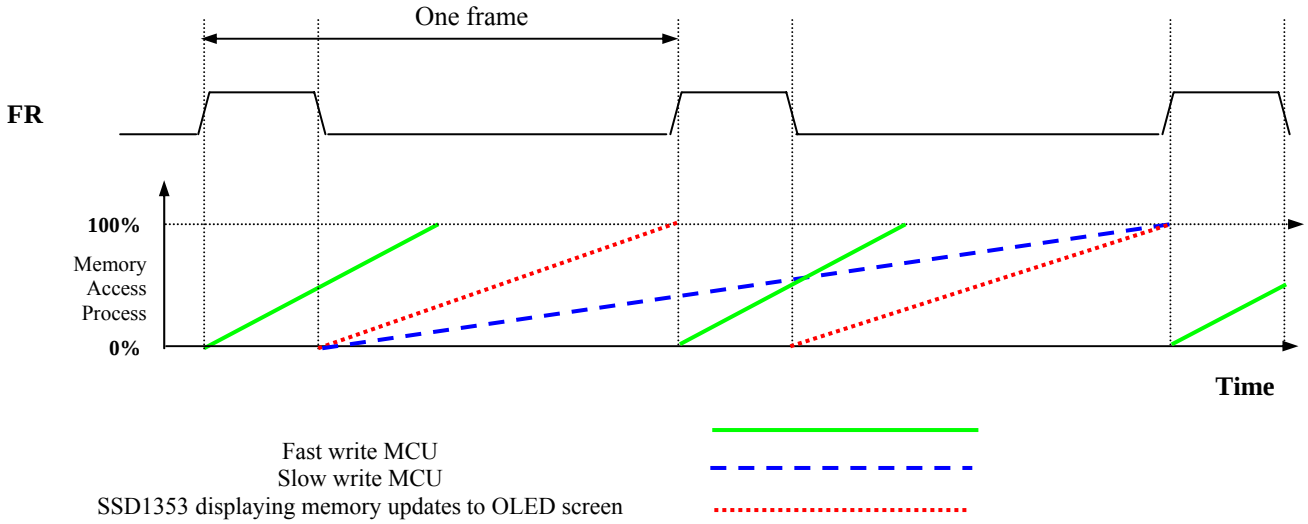
where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period +Phase 2 period + 98
  = 9 +7 +98 =114 (reset)
- Number of multiplex ratio is set by command A8h. The reset value is 131 (i.e. 132MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.5.2 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

8.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

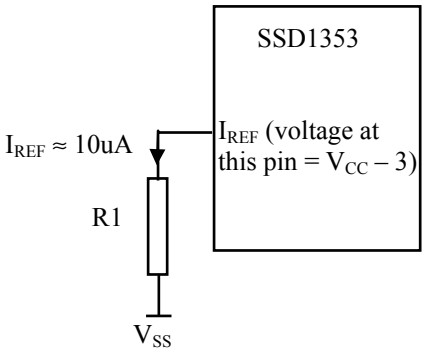
  I_{SEG} = Contrast / 256 * I_{REF} * scale factor

  in which
  the contrast (0~255) is set by Set Contrast command (81h,82h,83h); and
  the scale factor (1 ~ 16) is set by Master Current Control command (87h).

  For example, in order to achieve I_{SEG} = 160uA at maximum contrast 255, I_{REF} is set to around 10uA. This current value is obtained by connecting an appropriate resistor from IREF pin to V_{SS} as shown in Figure 8-7.

  Recommended I_{REF} = 10uA

Figure 8-7 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below:

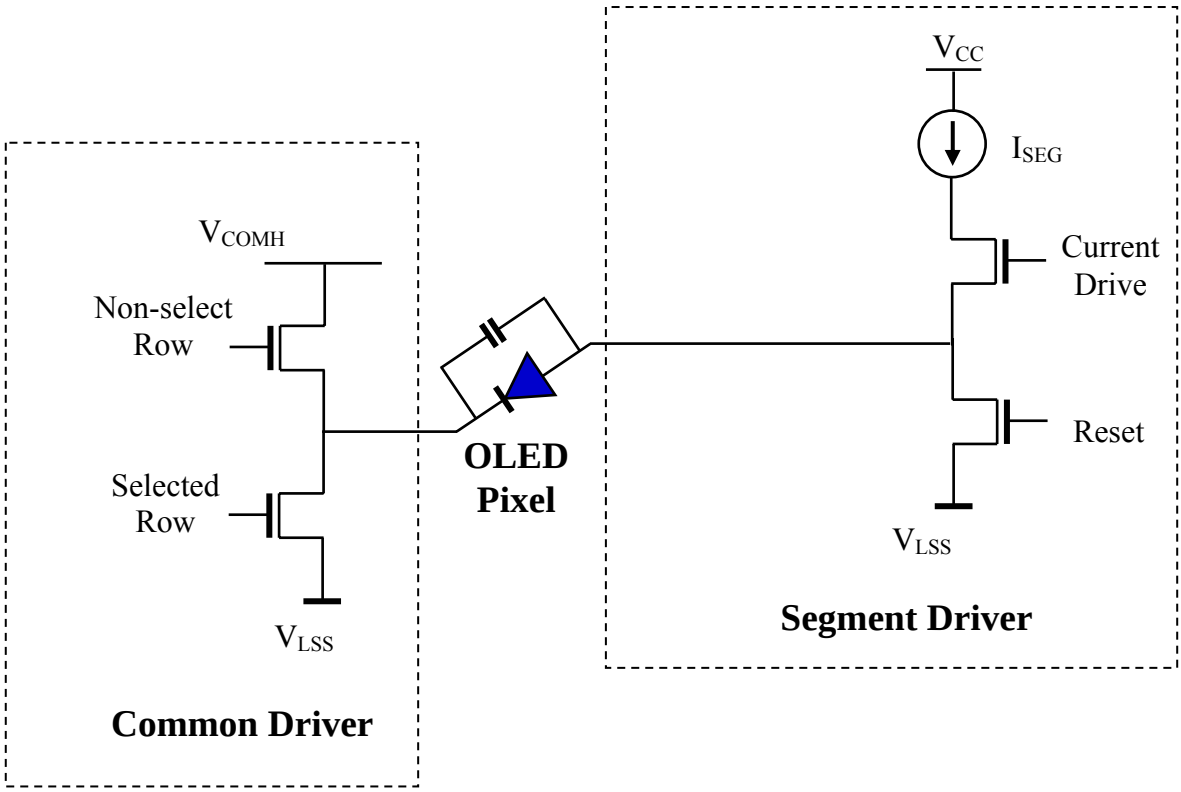
For I_{REF} =10uA, V_{CC} =18V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
= (18 – 3) / 10uA
= ≈ 1.5M Ω

8.7 SEG / COM Driver

Segment drivers consist of 480 (160 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 160uA with 256 steps by contrast setting command (81h, 82h, 83h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

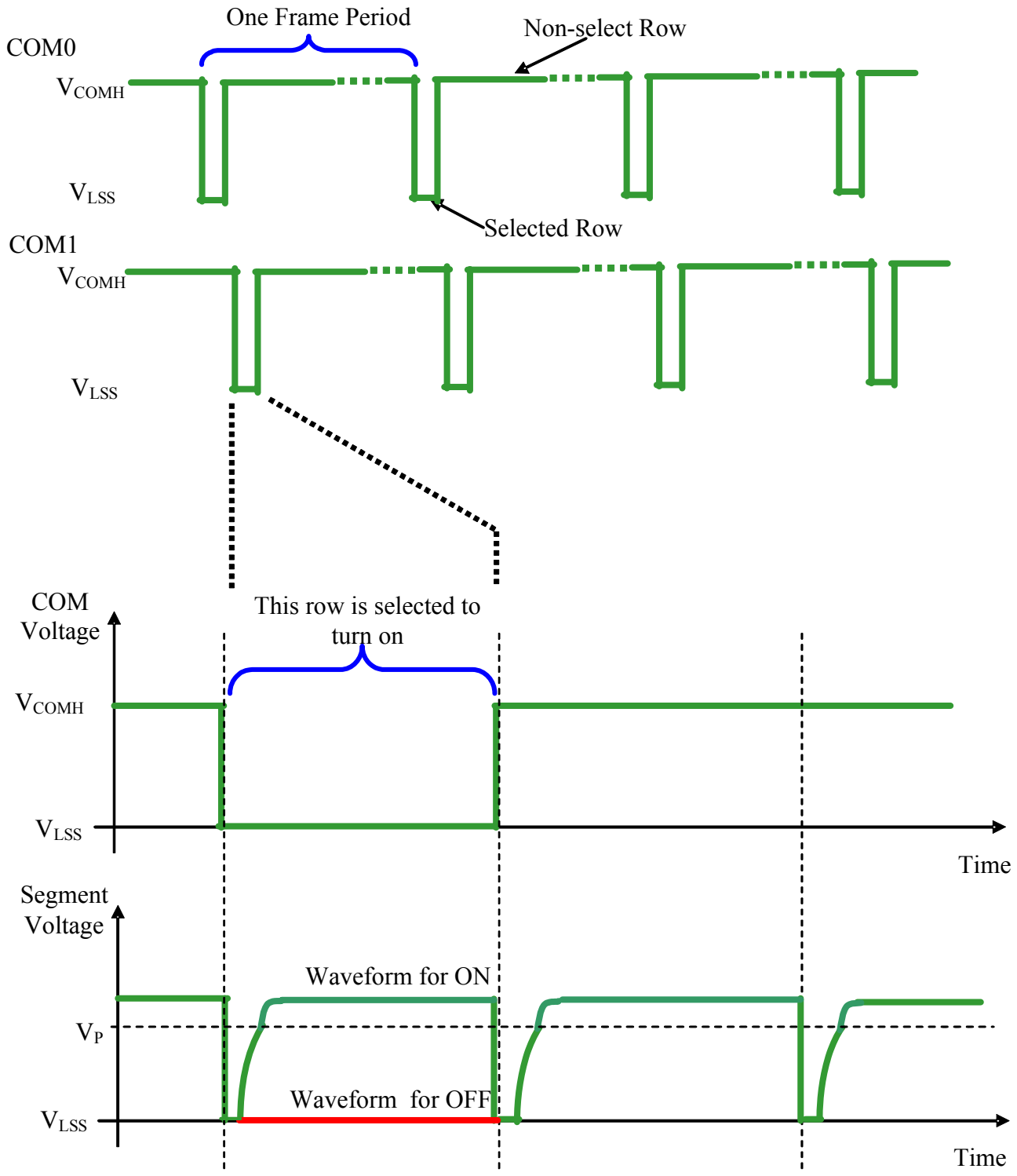
Figure 8-8 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-9.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-9 : Segment and Common Driver Signal Waveform



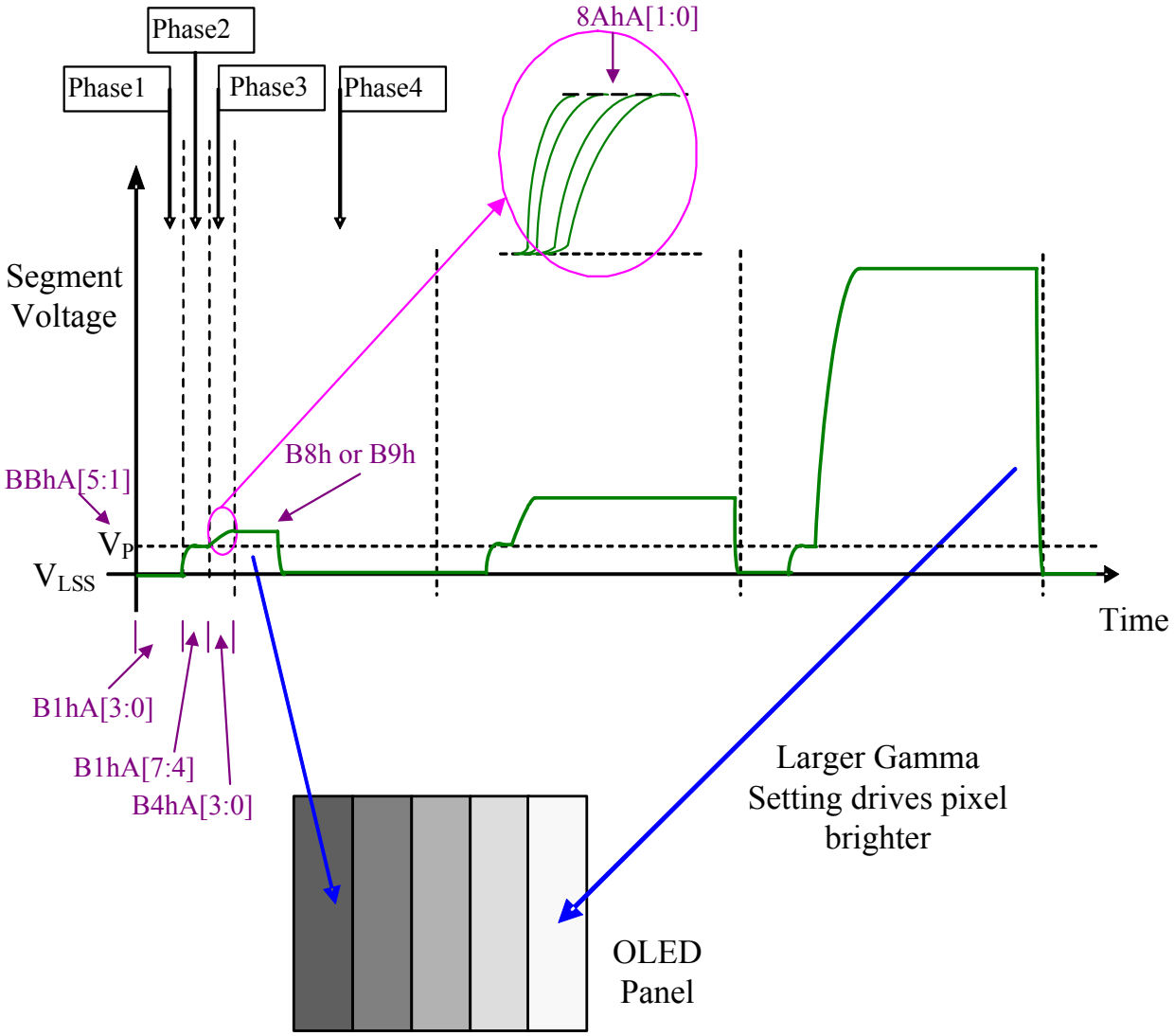
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B4h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PAM+PWM (Pulse Area Modulation + Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 8.8). This is shown in the following figure.

Figure 8-10: Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the segment current in current drive phase. The segment current is controlled by the Gamma Settings (Setting 0~ Setting 128). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding Gamma Setting of the 64 gray scale levels (GS0~GS63) through the software commands B8h or B9h. A single Gray Scale Table supports all the three colors A, B and C.

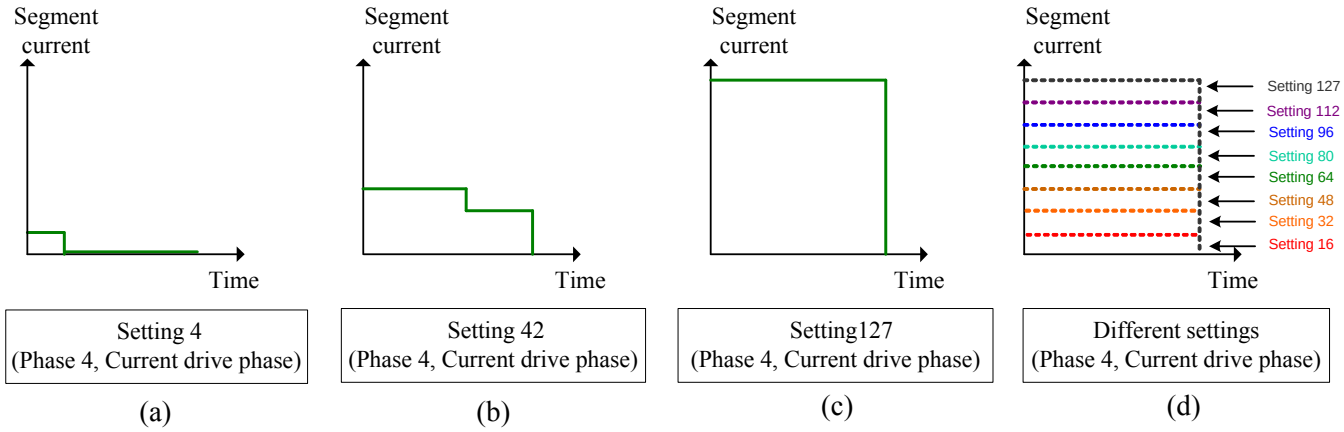
As shown in Figure 8-11, color A, B, C sub-pixel RAM data has 6 bits, represent the 64 gray scale level from GS0 to GS63.

Figure 8-11 : Relation between GDDRAM content and Gray Scale table entry for three colors in 262K color mode (under command B9h Enable Linear Gray Scale Table)

Color A,B ,C GDDRAM data (6 bits)	Gray Scale Table	Default Gamma Setting (Command B9h)
000000	GS0	Setting 0
000001	GS1	Setting 2
000010	GS2	Setting 4
000011	GS3	Setting 6
000100	GS4	Setting 8
:	:	:
011111	GS31	Setting 62
100000	GS32	Setting 65
100001	GS33	Setting 67
:	:	:
111100	GS60	Setting 121
111101	GS61	Setting 123
111110	GS62	Setting 125
111111	GS63	Setting 127

The Gray Scale Table can be programmed into different Gamma setting by command B8h. For example, if GS2 is programmed into Gamma setting 4, and the color A, B or C of GDDRAM is set as “000010b”, then the current drive phase will be similar to the illustration in Figure 8-12(a).

Figure 8-12 : Illustration of current drive phase (phase 4) under different Gamma Settings.



There are total 128 Gamma Settings (Setting 0 to Setting 127) available for the Gray Scale table. GS0 has no pre-charge and current drive stages so it is in Gamma Setting 0.

When setting the Gray Scale Table, the rules below must follow:

1) The gray scale is defined in incremental way, with reference to the length of previous table entry:
   0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63.
2) Different GSs should be set within the maximum Gamma Setting as follow:

Table 8-9 : Maximum Gamma setting in different Gray Scale ranges

Gary Scale Range	Maximum Gamma Setting allowed
GS0	Setting 0
GS1 ~ G7	Setting 15
GS8 ~ GS15	Setting 31
GS16 ~ GS31	Setting 63
GS32 ~ GS63	Setting 127

It should be notice that, the brightness under the following pairs of Gamma Setting will be the same:

Table 8-10 : Gamma Settings with identical brightness in current drive phase

Setting 15 & Setting 16	Setting 63 & Setting 64	Setting 111 & Setting 112
Setting 31 & Setting 32	Setting 79 & Setting 80	
Setting 47 & Setting 48	Setting 95 & Setting 96	

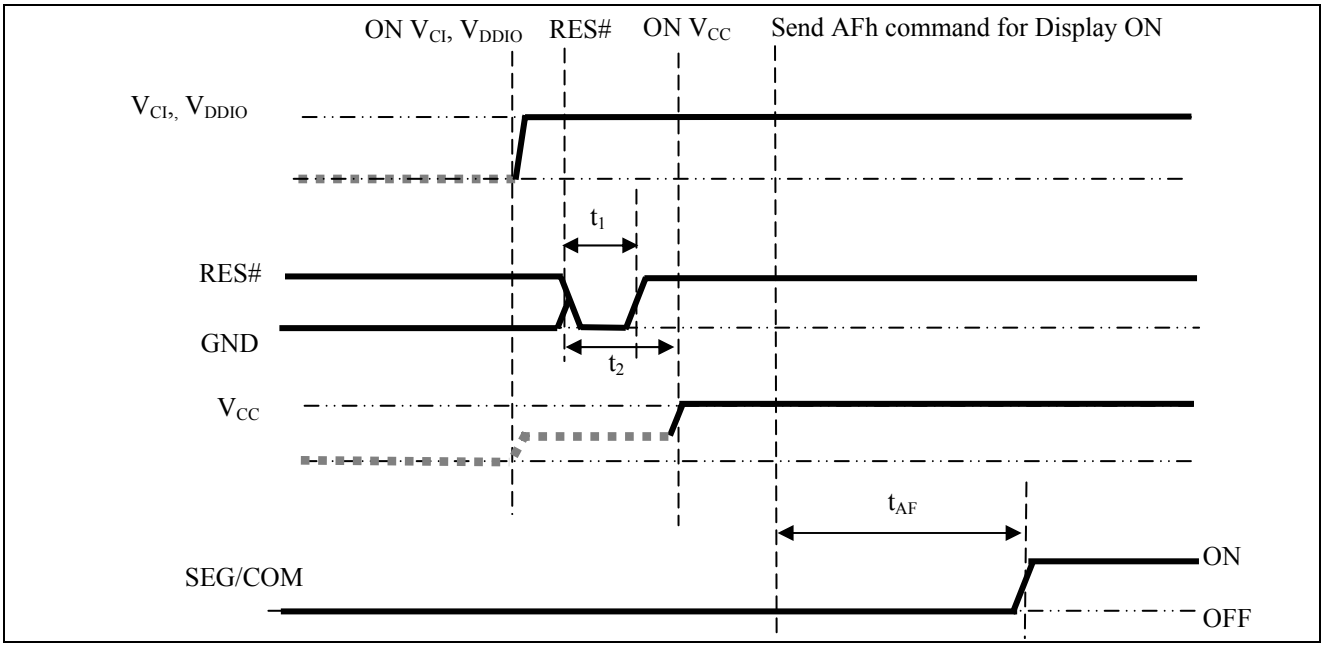
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1353 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON $V_{CI,}$ $V_{DDIO.}$
2. After V_{CI}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 100us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON $V_{CC.}$ [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).

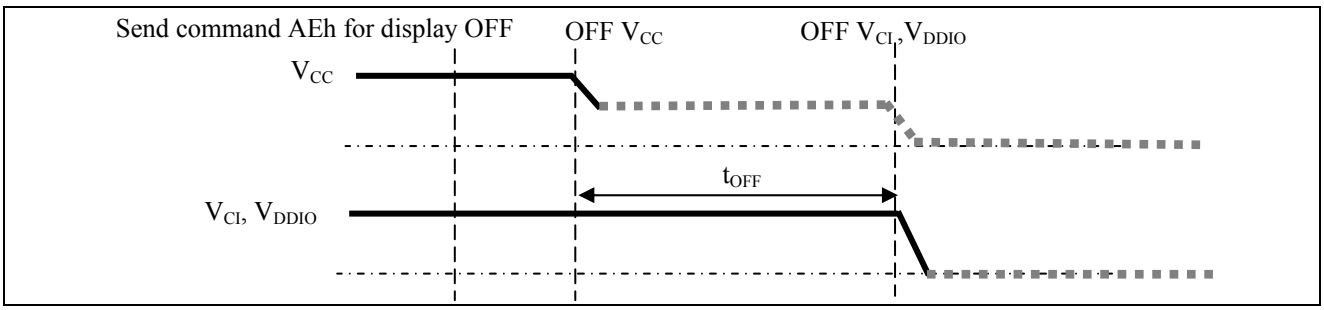
Figure 8-13: The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC.}$ [1], [2]
3. Wait for t_{OFF}. Power OFF $V_{CI,}$ $V_{DDIO.}$ (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 8-14: The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever $V_{CI,}$ V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-13 and Figure 8-14.

[2] V_{CC} should be kept float when it is OFF.

8.10 V_{DD} Regulator

In SSD1353, the power supply pin for core logic operation: V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

When the Internal V_{DD} regulator selections pin: REGVDD is pulled HIGH (i.e. connect to V_{DDIO}), the internal V_{DD} regulator is enabled. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

When the Internal V_{DD} regulator selection pin: REGVDD is pulled LOW (i.e. connect to Ground), external V_{DD} should be used. (external V_{DD} range : 2.4V~2.6V)

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated, V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-15 V_{CI} > 2.6V, V_{DD} regulator enable pin connection scheme

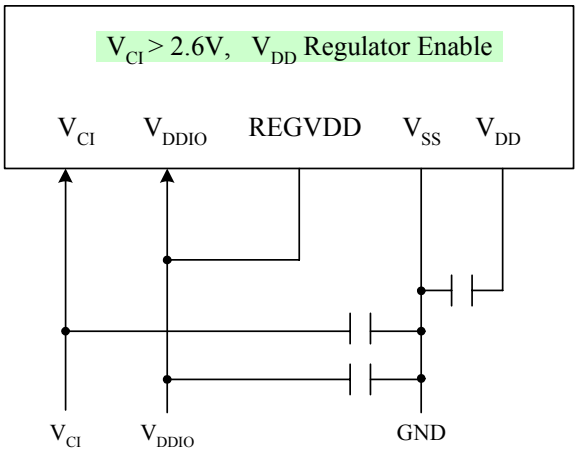
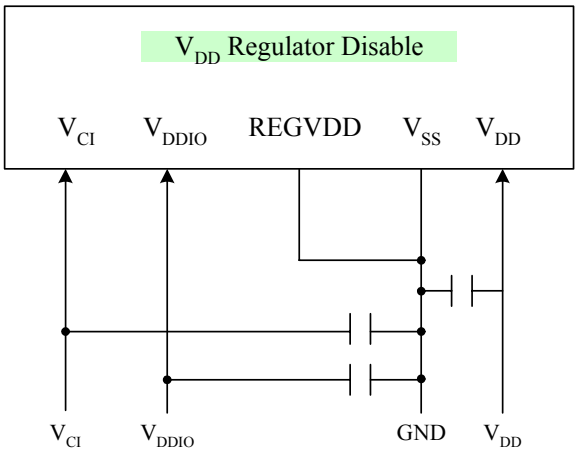


Figure 8-16 V_{DD} regulator disable pin connection scheme



9 COMMAND TABLE

Table 9-1 : Command table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1	15 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Set Column start and end address A[7:0]: Set start column address from 00d-159d [reset= 0d (00h)] B[7:0]: Set end column address from 00d-159d [reset= 159d (9Fh)]
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[7:0] B[7:0]	0 A_7 B_7	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Set Row start and end address A[7:0]: Set start row address from 00d-131d [reset= 0d (00h)] B[7:0]: Set end row address from 00d-131d [reset= 131d (83h)]
0 1	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast for Color "A"	Set contrast for all color "A" segment (Pins :SA0 – SA159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Contrast for Color "B"	Set contrast for all color "B" segment (Pins :SB0 – SB159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	83 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Contrast for Color "C"	Set contrast for all color "C" segment (Pins :SC0 – SC159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	87 A[3:0]	1 *	0 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Current Control	Set master current attenuation factor A[3:0] can be set from 00d to 15d corresponding to 1/16, 2/16… to 16/16 attenuation. [reset= 15d (0Fh)]

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	8A A[1:0]	1 0	0 0	0 0	0 0	1 0	0 0	1 A_1	0 A_0	Set Second Pre-charge speed	Set Second Pre-charge speed A[1:0]= 00b, Second Pre-charge speed =slowest A[1:0]= 01b, Second Pre-charge speed =slow A[1:0]= 10b, Second Pre-charge speed =normal [reset] A[1:0]= 11b, Second Pre-charge speed =Fast
0 1	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Remap & Color Depth setting	Set driver remap and color depth A[0]=0, Horizontal address increment [reset] A[0]=1, Vertical address increment A[1]=0, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 0 to 159 [reset] A[1]=1, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 159 to 0 A[2]=0, normal order SA,SB,SC (e.g. RGB) [reset] A[2]=1, reverse order SC,SB,SA (e.g. BGR) A[3]=0, Disable left-right swapping on COM [reset] A[3]=1, Set left-right swapping on COM A[4]=0, Scan from COM0 to COM[N –1] [reset] A[4]=1, Scan from COM[N-1] to COM0. Where N is the multiplex ratio. A[5]=0, Disable COM Split Odd Even [reset] A[5]=1, Enable COM Split Odd Even Refer to Figure 10-5 for details. A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format [RESET] A[7:6] = 10; 256k color format A[7:6] = 11; 256k color 16-bit format 2 If 9-/18-bit mode is selected, color depth will be fixed to 256k regardless of the setting. Refer to Table 8-7 for details.
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display start line register by Row A[7:0]: from 00d to 131d [reset = 0d (00h)] **Note** (1) A[7:0] must be set to 0 when using A3h command.
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical offset by COM A[7:0]: from 00d to 131d [reset = 0d (00h)]
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4h=Normal Display [reset] A5h=Entire Display ON, all pixels turn ON at GS63 A6h=Entire Display OFF, all pixels turn OFF A7h=Inverse Display

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[7:0] from 15d to 131d (i.e.16MUX -132 MUX) A[7:0] from 00d to 14d are invalid entry [reset= 131d (83h)]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	AB	1	0	1	0	1	0	1	1	Dim Mode setting	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Pre-charge voltage setting, valid range 0 to 31d.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[4:0]	*	*	*	E_4	E_3	E_2	E_1	E_0		
0	AC	1	0	1	0	1	1	0	0	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) [reset] AFh = Display ON in normal mode Refer to Figure 10-12 for transitions between different modes
0	AE	1	0	1	0	1	1	1	0		
0	AF	1	0	1	0	1	1	1	1		
0	B1	1	0	1	1	0	0	0	1	Phase 1 and 2 period adjustment	A[3:0] : Phase 1 period in N DCLKs. 3~31 DCLKs allowed as follow: A[3:0] = 0000 invalid; 0001 3 DCLKs; 0010 5 DCLKs; 0011 7 DCLKs; 0100 9 DCLKs [reset]; : :; 1111 31 DCLKs A[7:4] : Phase 2 period in N DCLKs. 2~15 DCLKs allowed. A[7:4] = 0000 invalid; 0001 invalid; 0010 2 DCLKs; 0011 3 DCLKs; : :; 0111 7 DCLKs[reset]; : :; 1111 15 DCLKs
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Display Clock Divider / Oscillator Frequency	A[3:0] Divider DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) [reset=0000b] A[7:4] Fosc frequency Frequency increases as setting value increases [reset=1100b]
0 1	B4 A[3:0]	1 *	0 *	1 *	1 *	0 A_3	1 A_2	0 A_1	0 A_0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b 0 DCLKS 0001b 1 DCLKS 0010b 2 DCLKS .... 0111 7 DCLKS [reset] .... 1111 15 DCLKS
0 1 1 1 1 1 1 1 1 1 1 1	B8 A1[3:0] : A7[3:0] A8[4:0] : A15[4:0] A16[5:0] : A31[5:0] A32[6:0] : A63[6:0]	1 * : * * : * * : * * : *	0 * : * * : * * : * $A32_6$: $A63_6$	1 * : * * : * $A16_5$: $A31_5$ $A32_5$: $A63_5$	1 * : * $A8_4$: $A15_4$ $A16_4$: $A31_4$ $A32_4$: $A63_4$	1 $A1_3$: $A7_3$ $A8_3$: $A15_3$ $A16_3$: $A31_3$ $A32_3$: $A63_3$	0 $A1_2$: $A7_2$ $A2_2$: $A15_2$ $A16_2$: $A31_2$ $A32_2$: $A63_2$	0 $A1_1$: $A7_1$ $A8_1$: $A15_1$ $A16_1$: $A31_1$ $A32_1$: $A63_1$	0 $A1_0$: $A7_0$ $A8_0$: $A15_0$ $A16_0$: $A31_0$ $A31_0$: $A63_0$	Set Gray Scale Table	These 63 parameters define Gray Scale (GS) Table in terms of Gamma Setting A1[3:0]: Gamma Setting for GS1, A2[3:0]: Gamma Setting for GS2, : A62[6:0]: Gamma Setting for GS62, A63[6:0]: Gamma Setting for GS63. **Note** (1) Input 1d for Gamma Setting 1, 2d for Gamma setting 2, ... ,127d for Gamma Setting127 (2) 0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63 Refer to Section 8.8 for details.
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in Linear Gray Scale table GS0 = Gamma Setting 0; GS1 = Gamma Setting 2 GS2 = Gamma Setting 4; GS3 = Gamma Setting 6; : GS31 = Gamma Setting 62 GS32 = Gamma Setting 65; GS33 = Gamma Setting 67; : GS62 = Gamma Setting 125; GS63 = Gamma Setting 127; Refer to Section 8.8 for details.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge level	Set pre-charge voltage level. All three colors share the same pre-charge voltage. [RESET =3Eh]
1	A[5:1]	0	0	A_5	A_4	A_3	A_2	A_1	0		

A[5:1]	Hex code	pre-charge voltage
00000	00h	0.10 x V_{CC}
:	:	:
11111	3Eh	0.55 x V_{CC}

0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	Set COM deselect voltage level [reset =3Ch] A[5:2] =
1	A[5:2]	0	0	A_5	A_4	A_3	A_2	0	0		

A[5:2]	Hex code	V_{COMH}
0000	00h	0.51 x V_{CC}
0001	04h	0.53 x V_{CC}
..	..	..
1101	34h	0.79 x V_{CC}
1110	38h	0.81 x V_{CC}
1111	3Ch	0.84 x V_{CC}

0	C0	1	1	0	0	0	0	0	0	OTP Write	Program data from MCU to OTP for color co-ordinate tuning. Details refer to section 10.1.22 "OTP Write (C0h)".
1		CBTR3	CBTR2	CBTR1	CBTR0	CATR3	CATR2	CATR1	CATR0		
1		*	*	*	*	CCTR3	CCTR2	CCTR1	CCTR0		
0	E2	1	1	1	0	0	0	1	0	Software Reset	Reset display circuit and stop Graphic Acceleration operations.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation.
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status [RESET = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [RESET] A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
1	A[2]	0	0	0	1	0	A_2	1	0		

Note
(1) "*" stands for "Don't care".

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	21	0	0	1	0	0	0	0	1	Draw Line	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] and G[5:0] , despite of the color format setting in command A0h
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[5:0]	*	*	G_5	G_4	G_3	G_2	G_1	G_0		
0	22	0	0	1	0	0	0	1	0	Drawing Rectangle	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line H[5:0] : Color C of the fill area I[5:0] : Color B of the fill area J[5:0] : Color A of the fill area **Note** (1) Please enter all 6 bits for Color setting: E[5:0], F[5:0] , G[5:0], H[5:0]. I[5:0] and J[5:0] , despite of the color format setting in command A0h (2) 0<A[7:0] < C[7:0] <159 (3) 0<B[7:0] < D[7:0]<131
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
1	G[5:0]	*	*	G_5	G_4	G_3	G_2	G_1	G_0		
1	H[5:0]	*	*	H_5	H_4	H_3	H_2	H_1	H_0		
1	I[5:0]	*	*	I_5	I_4	I_3	I_2	I_1	I_0		
1	J[5:0]	*	*	J_5	J_4	J_3	J_2	J_1	J_0		
0	23	0	0	1	0	0	0	1	1	Copy	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Column Address of New Start F[7:0] : Row Address of New Start
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
1	F[7:0]	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0		
0	24	0	0	1	0	0	1	0	0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1 1 1	25 A[7:0] B[7:0] C[7:0] D[7:0]	0 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	1 A_5 B_5 C_5 D_5	0 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	1 A_2 B_2 C_2 D_2	0 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End
0 1	26 A[4:0]	0 *	0 *	1 *	0 A_4	0 0	1 0	1 0	0 A_0	Fill Enable / Disable	A[0] : 0b = Disable Fill for Draw Rectangle Command [reset] 1b = Enable Fill for Draw Rectangle Command A[3:1] : 000 (Reserved values) A[4] : 0b = Disable reverse copy (reset) 1b = Enable reverse during copy command.
0 1 1 1 1 1	27 A[7:0] B[7:0] C[7:0] D[7:0] E[1:0]	0 A_7 B_7 C_7 D_7 *	0 A_6 B_6 C_6 D_6 *	1 A_5 B_5 C_5 D_5 *	0 A_4 B_4 C_4 D_4 *	0 A_3 B_3 C_3 D_3 *	1 A_2 B_2 C_2 D_2 *	1 A_1 B_1 C_1 D_1 E_1	1 A_0 B_0 C_0 D_0 E_0	Continuous Horizontal & Vertical Scrolling Setup	A[7:0]: Set number of column as horizontal scroll offset Range: 0d-131d (no horizontal scroll if equals to 0 B[7:0]: Define start row address C[7:0]: Set number of rows to be horizontal scrolled B[7:0]+C[7:0] <=132 D[7:0]: Set number of row as vertical scroll offset Range: 0d-131d (no vertical scroll if equals to 0) E[1:0]: Set time interval between each scroll step 00b 3 frames 01b 5 frames 10b 50 frames 11b 100 frames **Note**: (1) Vertical scroll run with command A3h Set Vertical Scroll Area (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Deactivate horizontal scrolling. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

Graphic Acceleration Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Activate horizontal scrolling. This command activates the scrolling function according to the setting done by command 27h Continuous Horizontal & Vertical Scrolling Setup
0 1 1	A3 A[7:0] B[7:0]	1 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[7:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[7:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 132] **Note** (1) A[7:0]+B[7:0] <= MUX ratio (2) B[7:0] <= MUX ratio (3) Set Display Start Line (A1h) must be set to 0 when using A3h command. (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 132d MUX display A[7:0] = 0, B[7:0]=132 : whole area scrolls A[7:0]= 0, B[7:0] < 132 : top area scrolls A[7:0] + B[7:0] < 132 : central area scrolls A[7:0] + B[7:0] = 132 : bottom area scrolls Refer to Figure 10-20 for details.

10 COMMAND DESCRIPTIONS

10.1 Fundamental Command

10.1.1 Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

10.1.2 Write RAM Command (5Ch)

After this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

10.1.3 Read RAM Command (5Dh)

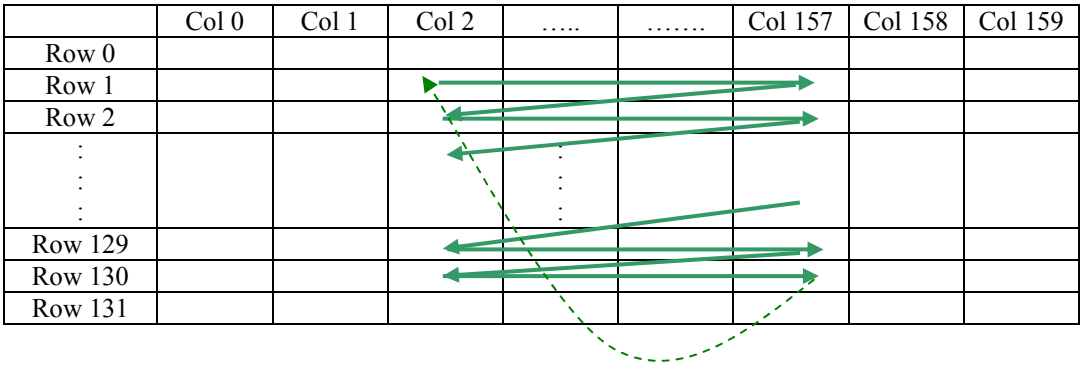
After this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

10.1.4 Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The figure below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 157, row start address is set to 1 and row end address is set to 130. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 157 and from row 1 to row 130 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation *(solid line in Figure 10-1*). Whenever the column address pointer finishes accessing the end column 157, it is reset back to column 2 and row address is automatically increased by 1 *(solid line in Figure 10-1*). While the end row 130 and end column 157 RAM location is accessed, the row address is reset back to 1 *(dotted line in Figure 10-1*).

Figure 10-1 : Example of Column and Row Address Pointer Movement



10.1.5 Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases with the contrast step, which results in brighter of the color.

10.1.6 Master Current Control (87h)

This command is to control the segment output current by a scaling factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000b] to 16 [1111b]. Reset is 16 [1111b]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA.

10.1.7 Set Second Pre-charge speed (8Ah)

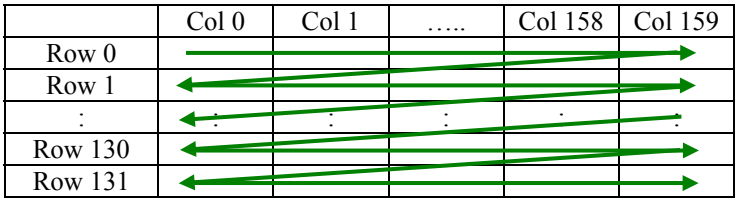
This command is used to set the speed of second pre-charge in phase 3. Please refer to Table 9-1 for the details of setting.

10.1.8 Set Re-map & Data Format (A0h)

This command has multiple configurations and each bit setting is described as follows.

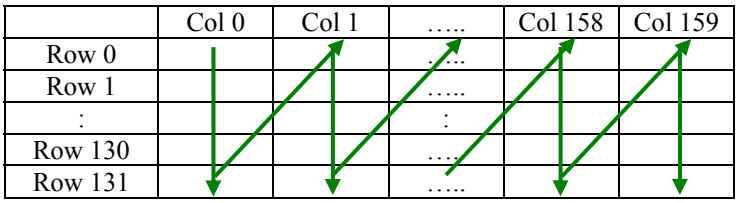
- Address increment mode (A[0])
  When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-2.

Figure 10-2 : Address Pointer Movement of Horizontal Address Increment Mode



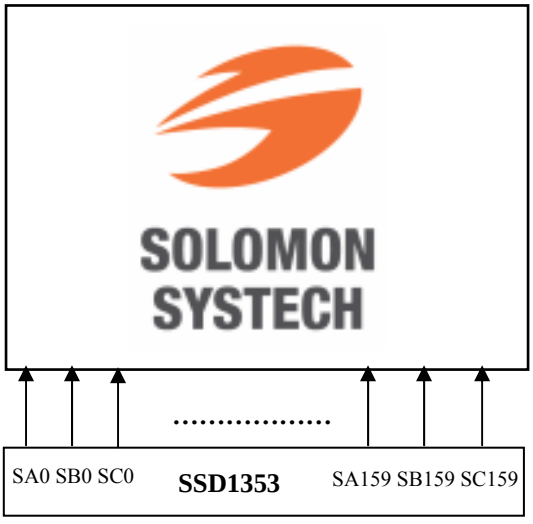
When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-3.

Figure 10-3 : Address Pointer Movement of Vertical Address Increment Mode

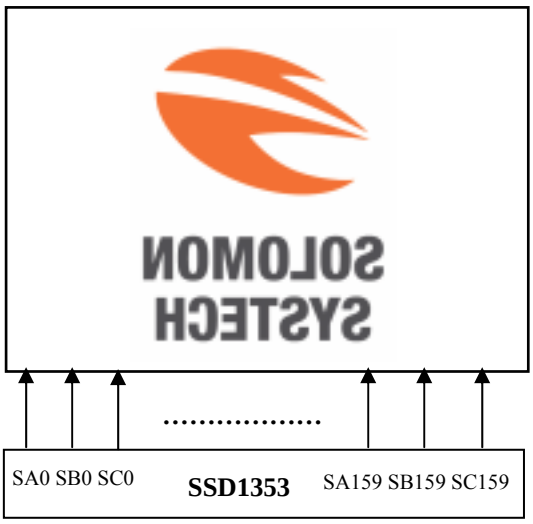


- Column Address Mapping (A[1])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa. The display direction is either mapping display data RAM column 0 to SEG0 pin (A[1] = 0), or mapping display data RAM column 159 to SEG0 pin (A[1] = 1). The effects of both are shown in Figure 10-4.

Figure 10-4 : Example of Column Address Mapping



Column 0 maps to SEG0 pin



Column 159 maps to SEG0 pin

- RGB Mapping (A[2])
  This command bit is made for flexible layout of segment signals in OLED module to match filter design.

- COM Left / Right Remap (A[3])
  This command bit is made for flexible layout of common signals in OLED module with common 0 arranged on either left or right side. Details of pin arrangement can be found in Figure 10-5.

- COM scan direction Remap (A[4])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa. Details of pin arrangement can be found in Figure 10-5.

- Odd even split of COM pins (A[5])
  This bit can set the odd even arrangement of COM pins.
  A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
  COM131 COM130 .... COM 67 COM66..SC159...SA0..COM0 COM1.... COM64 COM65
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM131 COM129.... COM3 COM1..SC159..SA0..COM0 COM2.... COM128 COM130
  Details of pin arrangement can be found in Figure 10-5.

- Display color mode (A[7:6])
  Select either 65k or 256 color mode. The display RAM data format in different mode is described in section 8.3.

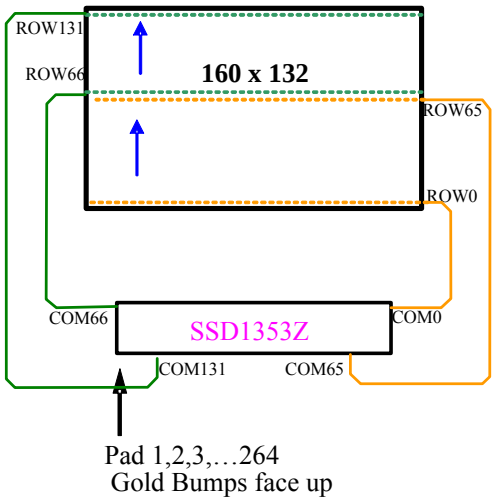
Figure 10-5 : COM Pins Hardware Configuration (MUX ratio: 132)

Case and Conditions	COM pins Configurations

A

A[5] =0	A[4]=0	A[3]=0
Disable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Disable COM Left / Right Remap

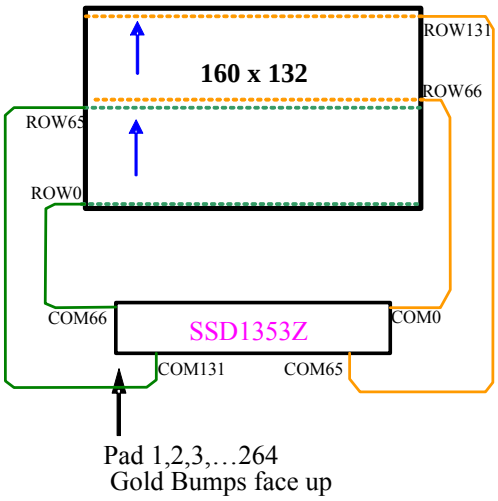
Pin name	Panel
COM 0	Row 0
COM 1	Row 1
COM 2	Row 2
… …	… …
COM 64	Row 64
COM 65	Row 65
COM 66	Row 66
COM 67	Row 67
…	… …
COM 129	Row 129
COM 130	Row 130
COM 131	Row 131



B

A[5] =0	A[4]=0	A[3]=1
Disable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Enable COM Left / Right Remap

Pin name	Panel
COM 0	Row 66
COM 1	Row 67
COM 2	Row 68
… …	… …
COM 64	Row 130
COM 65	Row 131
COM 66	Row 0
COM 67	Row 1
…	… …
COM 129	Row 63
COM 130	Row 64
COM 131	Row 65

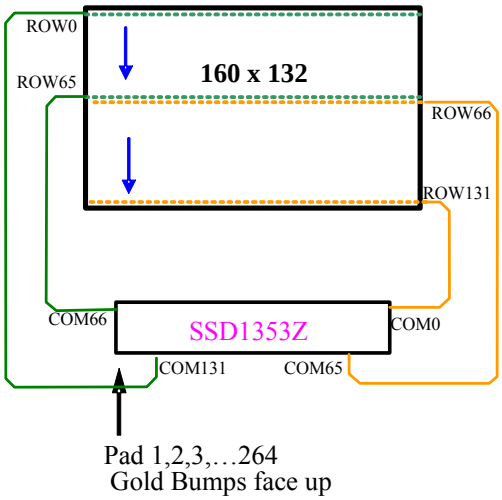


Case and Conditions	COM pins Configurations

C

A[5] =0	A[4]=1	A[3]=0
Disable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Disable COM Left / Right Remap

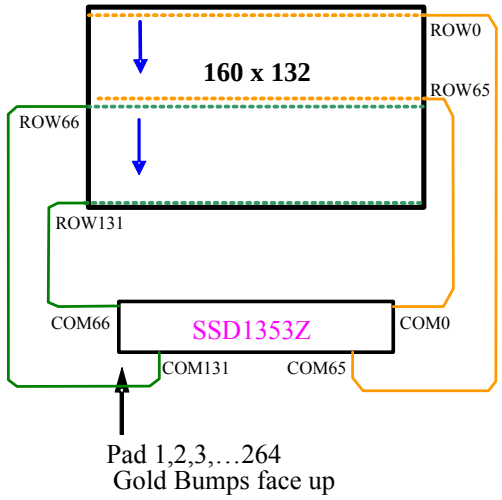
Pin name	Panel
COM 0	Row 131
COM 1	Row 130
COM 2	Row 129
… …	… …
COM 64	Row 67
COM 65	Row 66
COM 66	Row 65
COM 67	Row 64
…	… …
COM 129	Row 2
COM 130	Row 1
COM 131	Row 0



D

A[5] =0	A[4]=1	A[3]=1
Disable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Enable COM Left / Right Remap

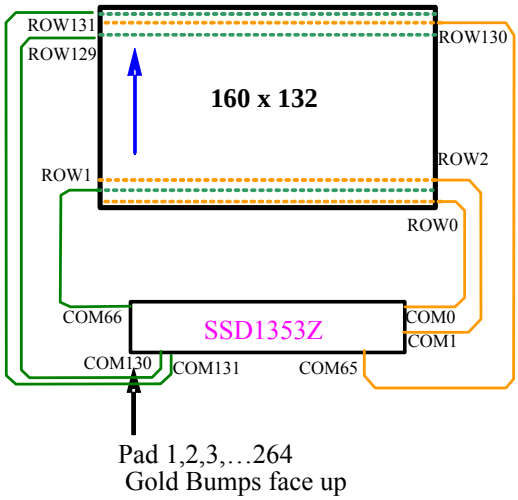
Pin name	Panel
COM 0	Row 65
COM 1	Row 64
COM 2	Row 63
… …	… …
COM 64	Row 1
COM 65	Row 0
COM 66	Row 131
COM 67	Row 130
…	… …
COM 129	Row 68
COM 130	Row 67
COM 131	Row 66



E

A[5] =1	A[4]=0	A[3]=0
Enable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Disable COM Left / Right Remap

Pin name	Panel
COM 0	Row 0
COM 1	Row 2
COM 2	Row 4
… …	… …
COM 64	Row 128
COM 65	Row 130
COM 66	Row 1
COM 67	Row 3
…	… …
COM 129	Row 127
COM 130	Row 129
COM 131	Row 131

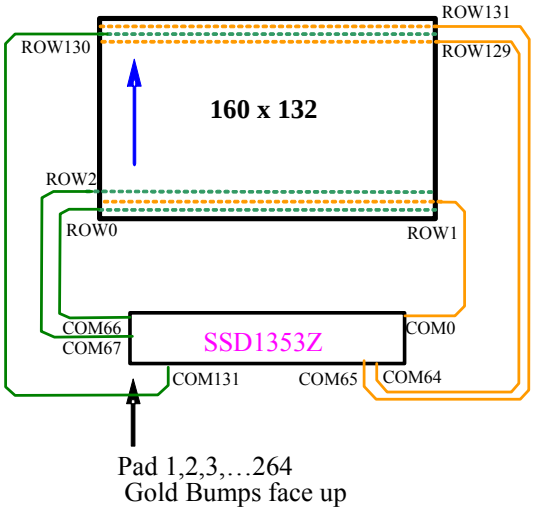


Case and Conditions	COM pins Configurations

F

A[5] =1	A[4]=0	A[3]=1
Enable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM131	Enable COM Left / Right Remap

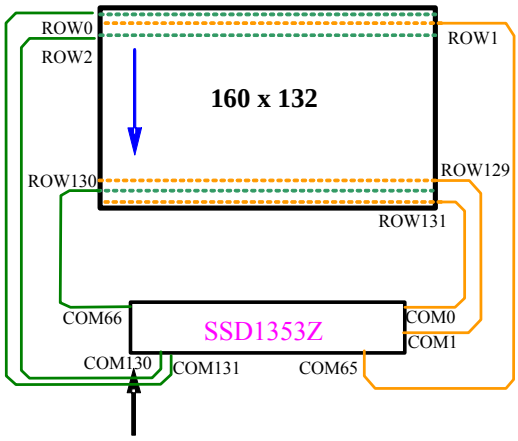
Pin name	Panel
COM 0	Row 1
COM 1	Row 3
COM 2	Row 5
… …	… …
COM 64	Row 129
COM 65	Row 131
COM 66	Row 0
COM 67	Row 2
…	… …
COM 129	Row 126
COM 130	Row 128
COM 131	Row 130



G

A[5] =1	A[4]=1	A[3]=0
Enable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Disable COM Left / Right Remap

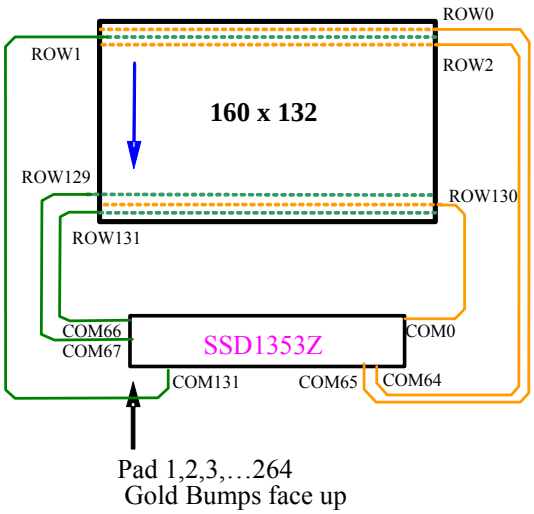
Pin name	Panel
COM 0	Row 131
COM 1	Row 129
COM 2	Row 127
… …	… …
COM 64	Row 3
COM 65	Row 1
COM 66	Row 130
COM 67	Row 128
…	… …
COM 129	Row 4
COM 130	Row 2
COM 131	Row 0



H

A[5] =1	A[4]=1	A[3]=1
Enable Odd Even Split of COM pins	COM Scan Direction : from COM131 to COM0	Enable COM Left / Right Remap

Pin name	Panel
COM 0	Row 130
COM 1	Row 128
COM 2	Row 126
… …	… …
COM 64	Row 2
COM 65	Row 0
COM 66	Row 131
COM 67	Row 129
…	… …
COM 129	Row 5
COM 130	Row 3
COM 131	Row 1



10.1.9 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 131. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 10-6 : Example of Set Display Start Line with no Remap

	132	132	100	100	MUX ratio (A8h)
COM Pin	0	32	0	32	Display start line (A1h)
COM0	Row0	Row32	Row0	Row32	
COM1	Row1	Row33	Row1	Row33	
COM2	Row2	Row34	Row2	Row34	
COM3	Row3	Row35	Row3	Row35	
COM4	Row4	Row36	Row4	Row36	
COM5	Row5	Row37	Row5	Row37	
COM6	Row6	Row38	Row6	Row38	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
COM95	Row95	Row127	Row95	Row128	
COM96	Row96	Row128	Row96	Row129	
COM97	Row97	Row129	Row97	Row130	
COM98	Row98	Row130	Row98	Row131	
COM99	Row99	Row131	Row99	Row0	
COM100	Row100	Row0	-	-	
COM101	Row101	Row1	-	-	
COM102	Row102	Row2	-	-	
COM103	Row103	Row3	-	-	
COM104	Row104	Row4	-	-	
COM105	Row105	Row5	-	-	
COM106	Row106	Row6	-	-	
COM107	Row107	Row7	-	-	
COM108	Row108	Row8	-	-	
COM109	Row109	Row9	-	-	
COM110	Row110	Row10	-	-	
COM111	Row111	Row11	-	-	
COM112	Row112	Row12	-	-	
COM113	Row113	Row13	-	-	
COM114	Row114	Row14	-	-	
COM115	Row115	Row15	-	-	
COM116	Row116	Row16	-	-	
COM117	Row117	Row17	-	-	
COM118	Row118	Row18	-	-	
COM119	Row119	Row19	-	-	
COM120	Row120	Row20	-	-	
COM121	Row121	Row21	-	-	
COM122	Row122	Row22	-	-	
COM123	Row123	Row23	-	-	
COM124	Row124	Row24	-	-	
COM125	Row125	Row25	-	-	
COM126	Row126	Row26	-	-	
COM127	Row127	Row27	-	-	
COM128	Row128	Row28	-	-	
COM129	Row129	Row29	-	-	
COM130	Row130	Row30	-	-	
COM131	Row131	Row31	-	-	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)	

10.1.10 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-131. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 10-7 : Example of Set Display Offset with no Remap

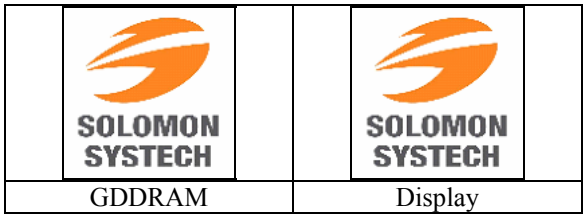
	132	132	100	100	MUX ratio (A8h)
COM Pin	0	32	0	32	Display offset (A2h)
COM0	Row0	Row32	Row0	Row32	
COM1	Row1	Row33	Row1	Row33	
COM2	Row2	Row34	Row2	Row34	
COM3	Row3	Row35	Row3	Row35	
COM4	Row4	Row36	Row4	Row36	
COM5	Row5	Row37	Row5	Row37	
COM6	Row6	Row38	Row6	Row38	
:	:	:	:	:	
:	:	:	:	:	
COM66	Row66	Row98	Row66	Row98	
COM67	Row67	Row99	Row67	Row99	
:	:	:	:	:	
:	:	:	:	:	
COM95	Row95	Row127	Row95	-	
COM96	Row96	Row128	Row96	-	
COM97	Row97	Row129	Row97	-	
COM98	Row98	Row130	Row98	-	
COM99	Row99	Row131	Row99	Row0	
COM100	Row100	Row0	-	Row1	
COM101	Row101	Row1	-	Row2	
COM102	Row102	Row2	-	Row3	
COM103	Row103	Row3	-	Row4	
COM104	Row104	Row4	-	Row5	
COM105	Row105	Row5	-	Row6	
COM106	Row106	Row6	-	Row7	
COM107	Row107	Row7	-	Row8	
COM108	Row108	Row8	-	Row9	
COM109	Row109	Row9	-	Row10	
COM110	Row110	Row10	-	Row11	
COM111	Row111	Row11	-	Row12	
COM112	Row112	Row12	-	Row13	
COM113	Row113	Row13	-	Row14	
COM114	Row114	Row14	-	Row15	
COM115	Row115	Row15	-	Row16	
COM116	Row116	Row16	-	Row17	
COM117	Row117	Row17	-	Row18	
COM118	Row118	Row18	-	Row19	
COM119	Row119	Row19	-	Row21	
COM120	Row120	Row20	-	Row20	
COM121	Row121	Row21	-	Row22	
COM122	Row122	Row22	-	Row23	
COM123	Row123	Row23	-	Row22	
COM124	Row124	Row24	-	Row24	
COM125	Row125	Row25	-	Row25	
COM126	Row126	Row26	-	Row26	
COM127	Row127	Row27	-	Row27	
COM128	Row128	Row28	-	Row28	
COM129	Row129	Row29	-	Row29	
COM130	Row130	Row30	-	Row30	
COM131	Row131	Row31	-	Row31	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)

10.1.11Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

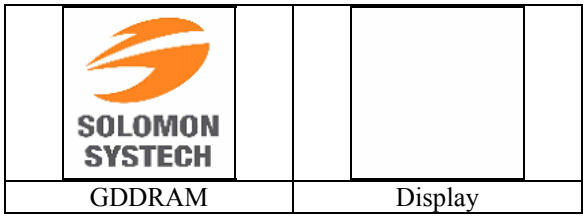
- Normal Display (A4h)
  Reset the above effect and turn the data to ON at the corresponding gray level. Figure 10-8 shows an example of Normal Display.

Figure 10-8 : Example of Normal Display



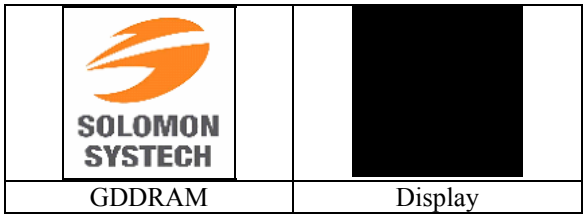
- Set Entire Display ON (A5h)
  Forces the entire display to be at "GS63" regardless of the contents of the display data RAM as shown in Figure 10-9.

Figure 10-9 : Example of Entire Display ON



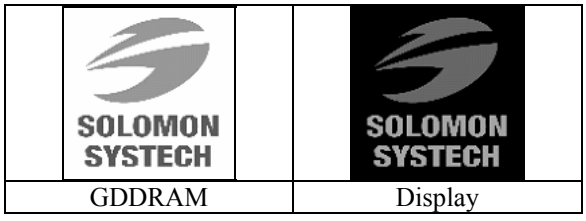
- Set Entire Display OFF (A6h)
  Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM as shown in Figure 10-10.

Figure 10-10 : Example of Entire Display OFF



- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", …..
  Figure 10-11 shows an example of inverse display.

Figure 10-11 : Example of Inverse Display



10.1.12Set Multiplex Ratio (A8h)

This command switches default 1:132 multiplex mode to any multiplex mode from 16 to 132. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h. Figure 10-6 and Figure 10-7 show examples of setting the multiplex ratio through command A8h.

10.1.13 Dim mode setting (ABh)

This command contains multiple bits to configure the dim mode display parameters.
Contrast setting of color A, B, C and precharge voltage can be set different to normal mode (AFh).

10.1.14 Set Display ON/OFF (ACh / AEh / AFh)

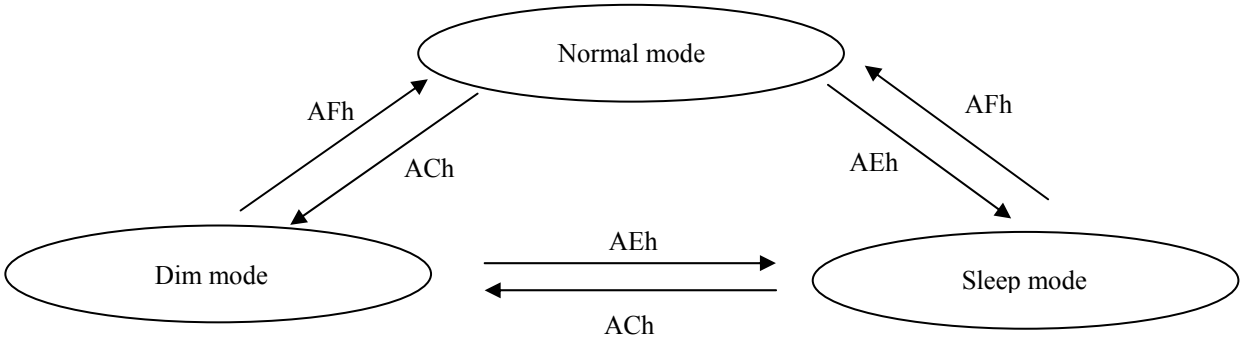
These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned off , the segment is in V_{SS} state and common is in high impedance state.

These commands set the display to one of the three states:

- ACh : Dim Mode Display ON
- AEh : Display OFF
- AFh : Normal Brightness Display ON

where the dim mode settings are controlled by command ABh.

Figure 10-12 : Transition between different modes



10.1.15 Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 3 to 31 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 2 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P for color A, B and C.

10.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to section 8.5.1 for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency setting available.

10.1.17 Set Second Pre-charge period (B4h)

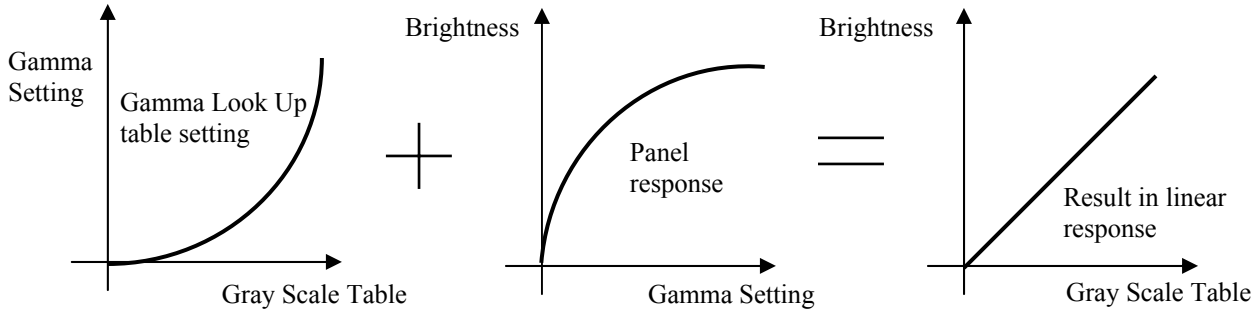
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B4h and it is ranged from 0 to 15 DCLK's. Please refer to Table 9-1 for the details of setting.

10.1.18 Set Gray Scale Table (B8h)

This command is used to set the Gray Scale (GS) table for the display. Except GS0, which is zero as it has no pre-charge and current drive, each entry GS level is programmed in the Gamma Setting. The larger value of Gamma Setting, the brighter is the OLED pixel when it's turned ON. Following the command B8h, the user has to set the Gamma Setting for GS1, GS2, GS3, …, GS61, GS62, GS63 one by one in sequence. Refer to Section 8.8 for details.

The setting of Gray Scale entry can perform Gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate Gray Scale table setting like example below can compensate this effect.

Figure 10-13 : Example of Gamma correction by Gamma Look Up table setting



10.1.19 Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear Gray Scale table as GS0 =Gamma Setting 0, GS1 = Gamma Setting 2, GS2 = Gamma Setting 4, ..., GS31=Gamma Setting 62, GS32=Gamma Setting 65, GS33=Gamma Setting 67, …., GS62 = Gamma Setting 125, GS63 = Gamma Setting 127. Refer to Section 8.8 for details.

10.1.20 Set Pre- charge voltage (BBh)

This command sets the pre-charge voltage level of segment pins, The level of pre-charge is programmed with reference to V_{CC}.

10.1.21 Set V_{COMH} Voltage (BEh)

This command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}.

10.1.22 OTP Write (C0h)

In SSD1353, the command C0h is used to program data from MCU to OTP. The following is the way to use the C0h command:

Stage 1 OTP offset Finding

[1]. Hardware Reset (sending an active low reset pulse to RES# pin)
[2]. Send original initialization routines
[3]. Set and display any test patterns
[4]. Adjust the color coordinate value through command C0h until there is the best visual performance

Table 10-1 : Command table of Colour Coordination Tuning (C0h)

CO H	RGBCOORT (Colour Coordination Tuning)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	0	CBTR3	CBTR2	CBTR1	CBTR0	CATR3	CATR2	CATR1	CATR0	xx
2nd Parameter	1	1	0	xx	xx	xx	xx	CCTR3	CCTR2	CCTR1	CCTR0	xx
Description	This command is used for testing and emulation of the color co-ordinate tuning.											

CATR [3:0], CBTR [3:0], CATR [3:0]	Tuning
0000	0
0001	1/32
0010	2/32
0011	3/32
0100	4/32
0101	5/32
0110	6/32
0111	7/32
1000	- 8/32
1001	- 7/32
1010	- 6/32
1011	- 5/32
1100	- 4/32
1101	- 3/32
1110	- 2/32
1111	- 1/32

[5]. Record down fine-tuned color coordinate value for stage 2.

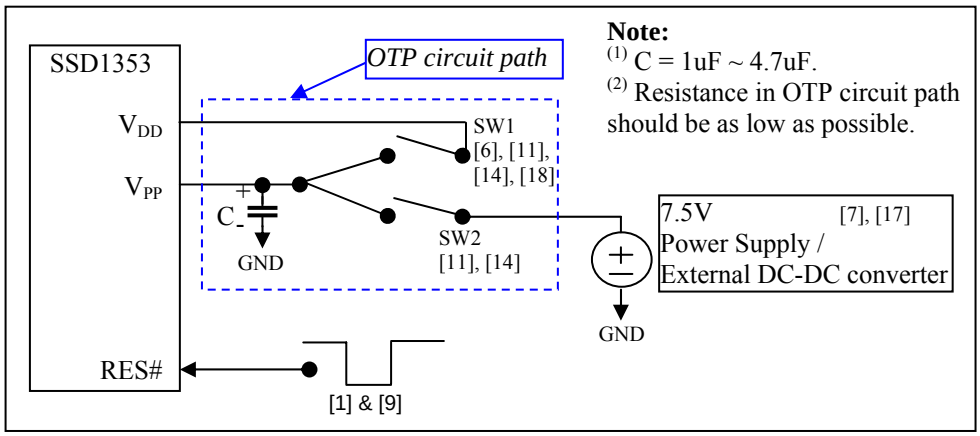
Stage 2 OTP programming

[6]. Connect V_{PP} externally by closing SW1 (see Figure 10-14 below)
[7]. Power ON V_{PP} and wait for 500 us
[8]. Power ON V_{DD} (regulated internally or supplied externally)and wait for 500 us
[9]. Hardware Reset (sending an active low reset pulse to RES# pin)
[10]. Send command C0h OTP Write and wait for 10ns
[11]. Open SW1 and then close SW2
[12]. Send 2 bytes data (from step [5] in stage 1) at frequency ~10KHz (9.5KHz ~10.5KHz) as follow:

Data byte	Content	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1st byte	Color coordinate value from step [5] in stage 1	CBTR3	CBTR2	CBTR1	CBTR0	CATR3	CATR2	CATR1	CATR0
2nd byte		xx	xx	xx	xx	CCTR3	CCTR2	CCTR1	CCTR0

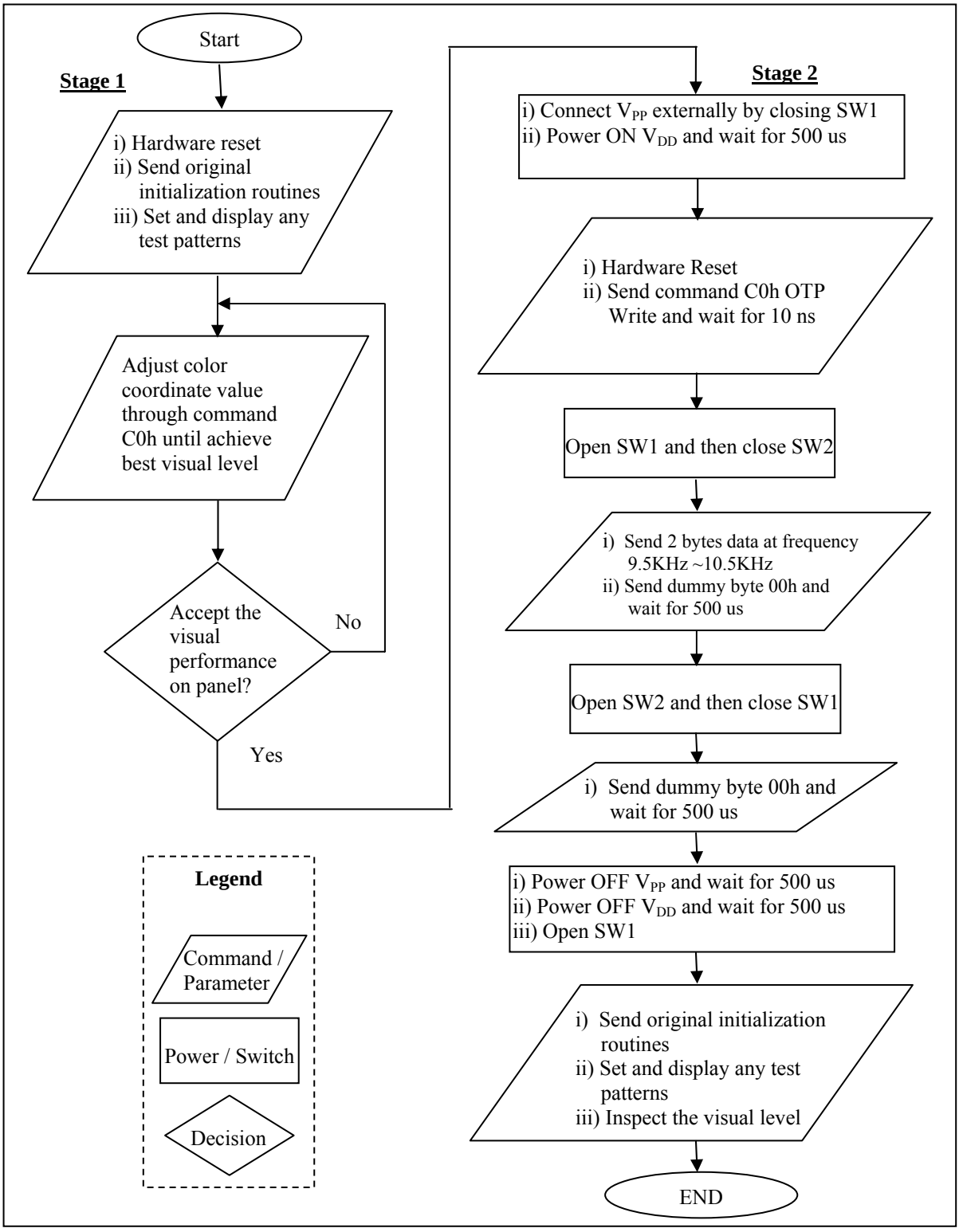
[13]. Send dummy byte 00h and wait for 500 us
[14]. Open SW2 and then close SW1
[15]. Send dummy byte 00h and wait for 500 us
[16]. Power OFF V_{DD} and wait for 500 us
[17]. Power OFF V_{PP} and wait for 500 us
[18]. Open SW1
[19]. Verify the result by repeating Stage 1. [2] – [3]

Figure 10-14 : OTP programming circuitry



Note
(1) In operation mode (without programming OTP), V_{PP} must be connected to V_{DD}.

Figure 10-15 - Flow chart of OTP programming Procedure



10.1.23 Software Reset (E2h)

This command resets the display circuit and stops the Graphic Acceleration operations by generating an internal reset pulse.

10.1.24 NOP (E3h)

This is the no operation command.

10.1.25 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

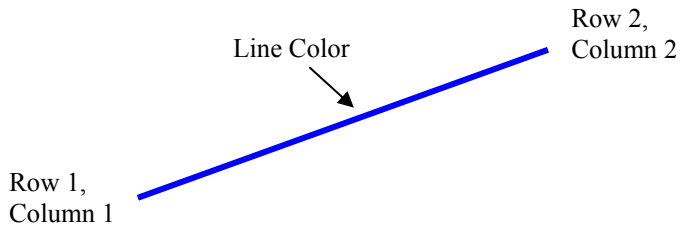
Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

10.2 Graphic Acceleration Command

10.2.1 Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

Figure 10-16 : Example of Draw Line Command



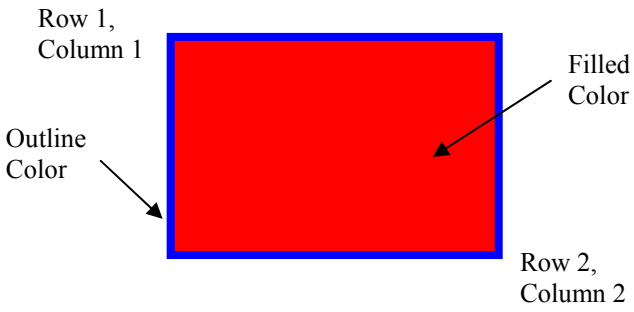
For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = (3Fh, 0h, 0h)

10.2.2 Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled (refer to command 26h Fill Enable/Disable), the enclosed area will not be filled.

Figure 10-17 : Example of Draw Rectangle Command



The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 22h
2. Set the starting column coordinates, Column 1, for example = 03h
3. Set the starting row coordinates, Row 1, for example = 02h
4. Set the finishing column coordinates, Column 2, for example = 12h
5. Set the finishing row coordinates, Row 2, for example = 15h
6. Set the outline color C, B and A, for example = (63d, 0d, 0d)
7. Set the filled color C, B and A, for example = (0d, 0d, 63d)

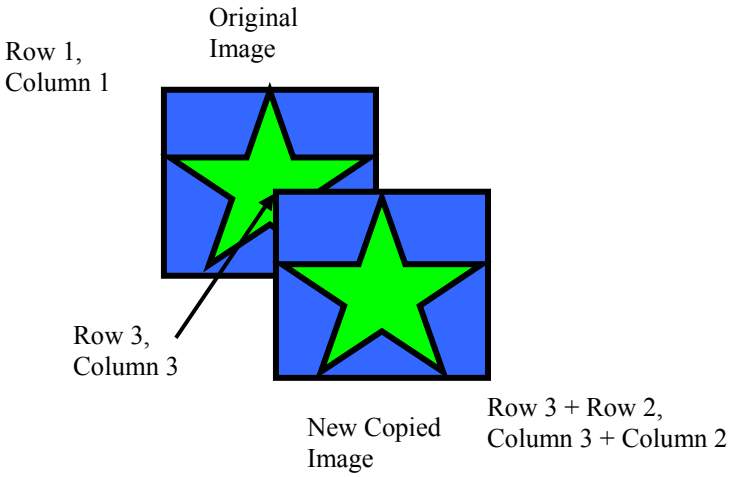
10.2.3 Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1, for example = 00h.
3. Set the starting row coordinates, Row 1, for example = 00h.
4. Set the finishing column coordinates, Column 2, for example = 05h
5. Set the finishing row coordinates, Row 2, for example = 05h
6. Set the new column coordinates, Column 3, for example = 03h
7. Set the new row coordinates, Row 3, for example = 03h

Figure 10-18 : Example of Copy Command



10.2.4 Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 10-2 : Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

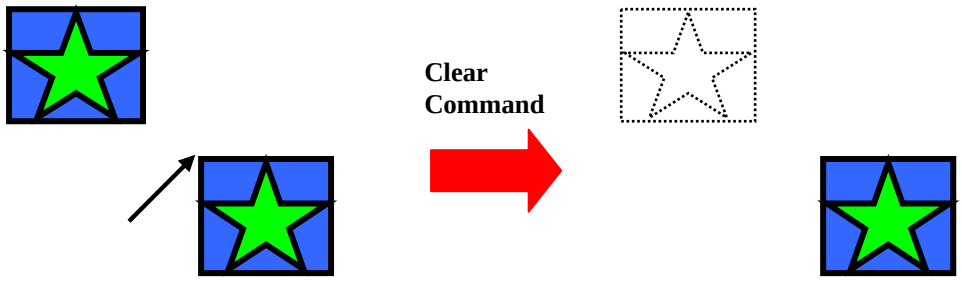
10.2.5 Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1, for example = 00h.
3. Set the starting row coordinates, Row 1, for example = 00h.
4. Set the finishing column coordinates, Column 2, for example = 05h
5. Set the finishing row coordinates, Row 2, for example 05h
6. Set the new column coordinates, Column 3, for example = 06h
7. Set the new row coordinates, Row 3, for example = 06h
8. Enter the "clear mode" by execute the command 24h
9. Set the starting column coordinates, Column 1, for example = 00h.
10. Set the starting row coordinates, Row 1, for example = 00h.
11. Set the finishing column coordinates, Column 2, for example = 05h
12. Set the finishing row coordinates, Row 2, for example = 05h

Figure 10-19 : Example of Copy + Clear = Move Command



10.2.6 Fill Enable/Disable (26h)

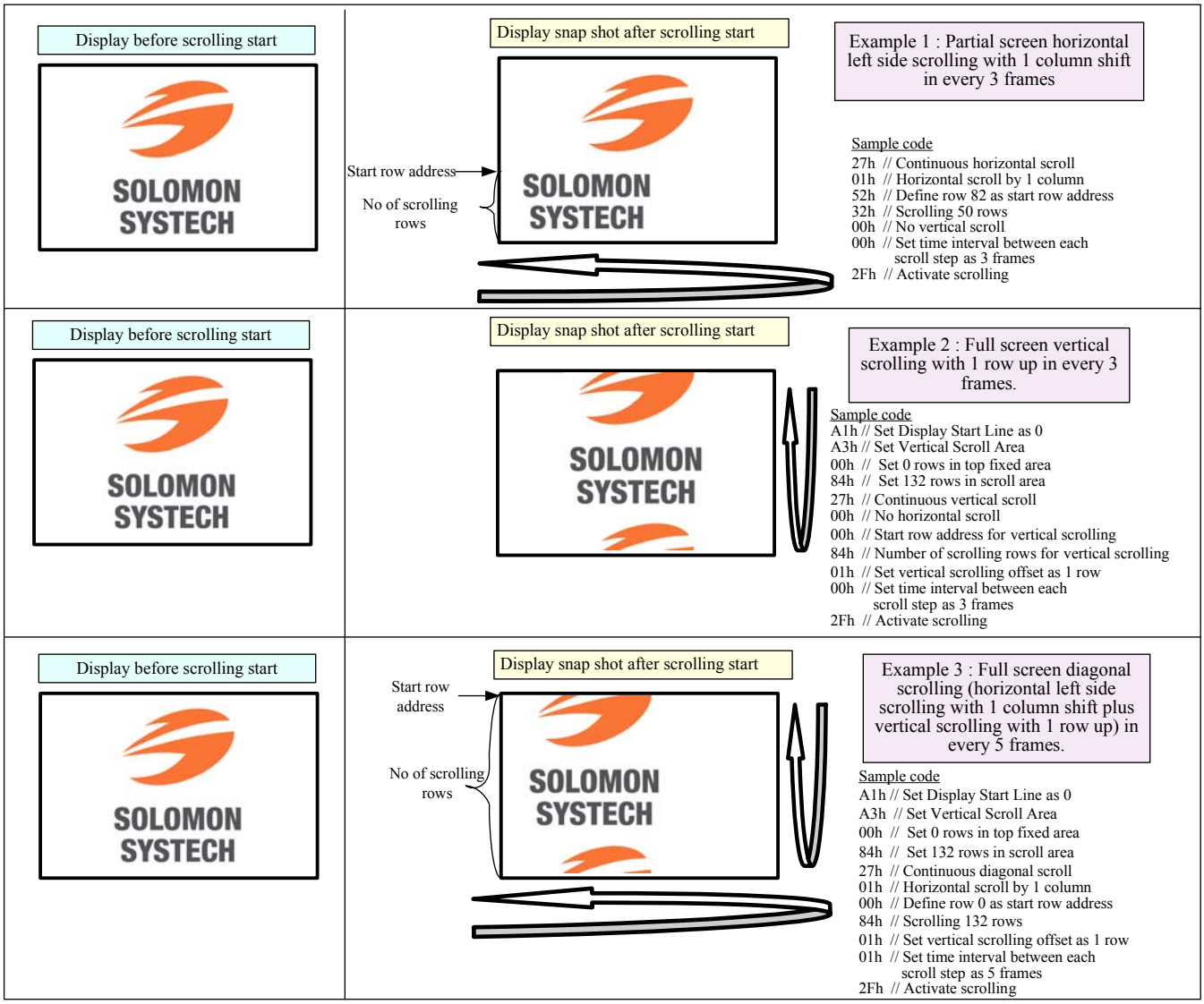
This command has two functions.

- Enable/Disable fill (A[0])
  0 = Disable filling of color into rectangle in draw rectangle command. (reset)
  1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
  0 = Disable reverse copy (reset)
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….

10.2.7 Horizontal Scroll Setup (27h)

This command setup the parameters required for horizontal and vertical scrolling. The parameters should not be changed after scrolling is activated

Figure 10-20 : Examples of Continuous Horizontal and Vertical Scrolling command setup



10.2.8 Deactivate Horizontal Scroll (2Eh)

This command deactivates the scrolling function. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.9 Activate Horizontal Scroll (2Fh)

This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

10.2.10 Set Vertical Scroll Area(A3h)

This command consists of 3 consecutive bytes to set up the vertical scroll area. For details please refer to Table 9-1.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to 2.75	V
V_{CC}		-0.5 to 22.0	V
V_{DDIO}		-0.5 to V_{CI}	V
V_{CI}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	Vss-0.3 to V_{DDIO}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD} = 2.4 to 2.6V
V_{CI} = 2.4 to 3.5V (V_{CI} must be larger than or equal to V_{DD})
T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-		10	-	21	V
V_{DD}	Logic Supply Voltage	-		2.4	-	2.6	V
V_{CI}	Low voltage power supply	-		2.4	-	3.5	V
V_{DDIO}	Power Supply for I/O pins	-		1.6	-	V_{CI}	V
V_{OH}	High Logic Output Level	Iout =100uA		0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	Iout =100uA		0	-	0.1*V_{DDIO}	V
V_{IH}	High Logic Input Level	-		0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-		0	-	0.2*V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached		-	-	15	uA
I_{SLP_VDDIO}	V_{DDIO} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached		-	-	15	uA
I_{SLP_VCI}	V_{CI} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached		-	-	15	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CI} = 3.3V, V_{DDIO} = V_{DD}(external) = 2.5V, Display OFF, No panel attached		-	-	15	uA
I_{DD}	V_{DD} Supply Current	V_{CI} = 3.3V, V_{CC} = 21V, V_{DDIO} =2.5V, External V_{DD} = 2.5V, Display ON, No panel attached, contrast = FF		-	950	1050	uA
I_{DDIO}	V_{DDIO} Supply Current	V_{CI} = 3.3V, V_{CC} = 21V, V_{DDIO} =2.5V, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	0.5	15	uA
			Internal V_{DD} = 2.5V	-	0.5	15	uA
I_{CI}	V_{CI} Supply Current	V_{CI} = 3.3V, V_{CC} = 21V, V_{DDIO} =2.5V, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	-110	-90	uA
			Internal V_{DD} = 2.5V	-	890	980	uA
I_{CC}	V_{CC} Supply Current	V_{CI} = 3.3V, V_{CC} = 21V, V_{DDIO} =2.5V, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	9.5	10.8	mA
			Internal V_{DD} = 2.5V	-	8.9	10	mA
I_{SEG}	Segment Output Current Setting V_{CC}=18V, I_{REF}=10uA	Contrast = FF , GS=127		-	160	175	uA
		Contrast = 7F, GS=127		-	80	-	uA
		Contrast = 7F, GS= 63		-	40	-	uA
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} = Segment current at contrast FF		-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])		-2	-	2	%

13 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD}=2.4 to2.6V
T_A = 25°C

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.5V	1.32	1.64	1.76	MHz
F_{FRM}	Frame Frequency for 132 MUX Mode	160x132 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*132) (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	100	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

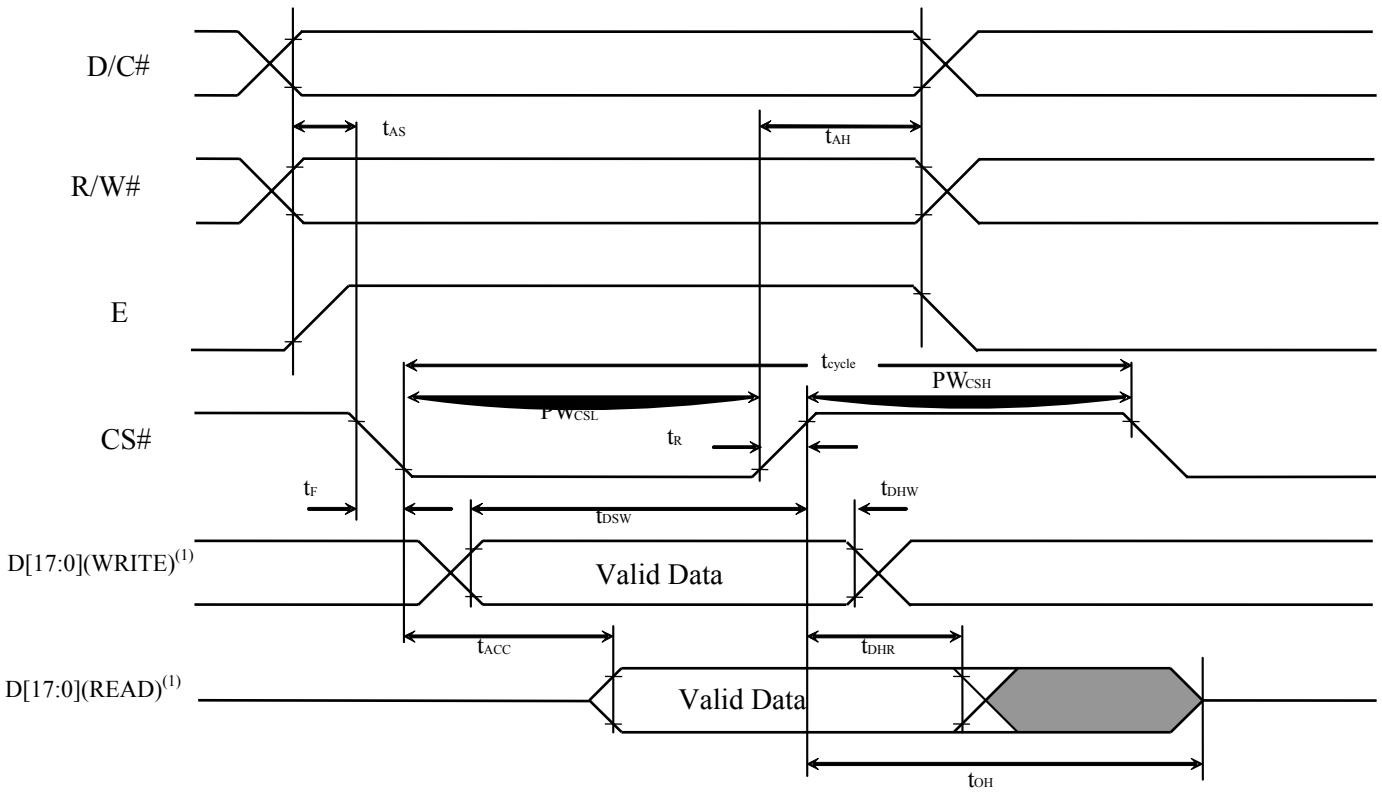
(2) D: divide ratio
K: Phase 1 period +Phase 2 period + 98

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series MCU parallel interface characteristics (Form 1)

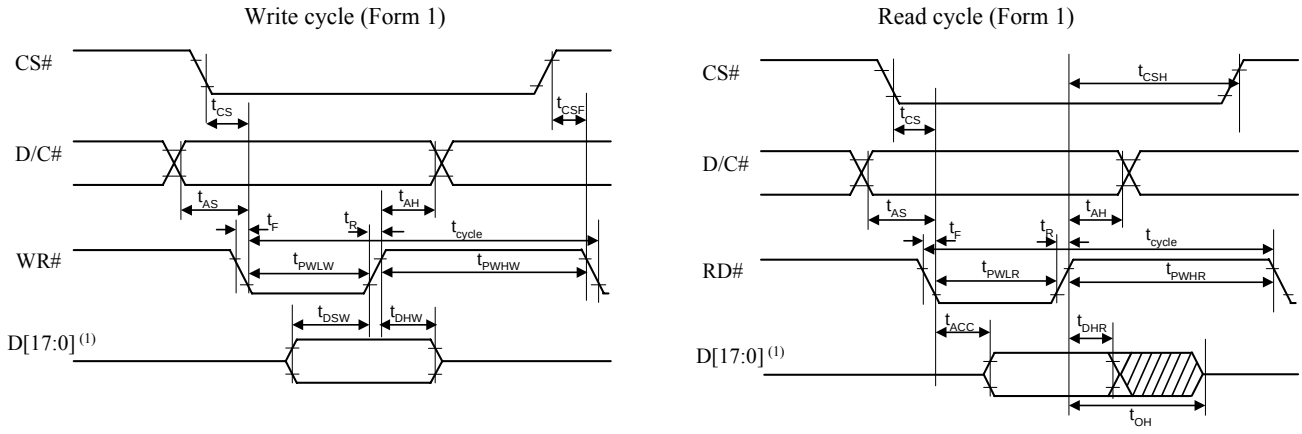
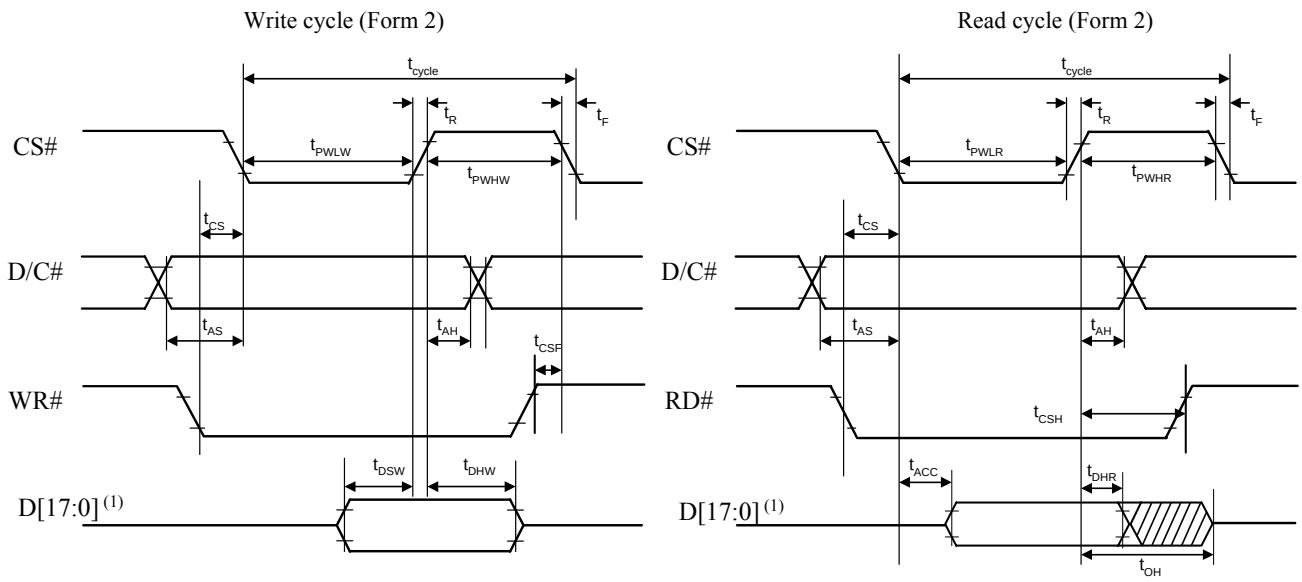


Figure 13-3 : 8080-series MCU parallel interface characteristics (Form 2)



Note

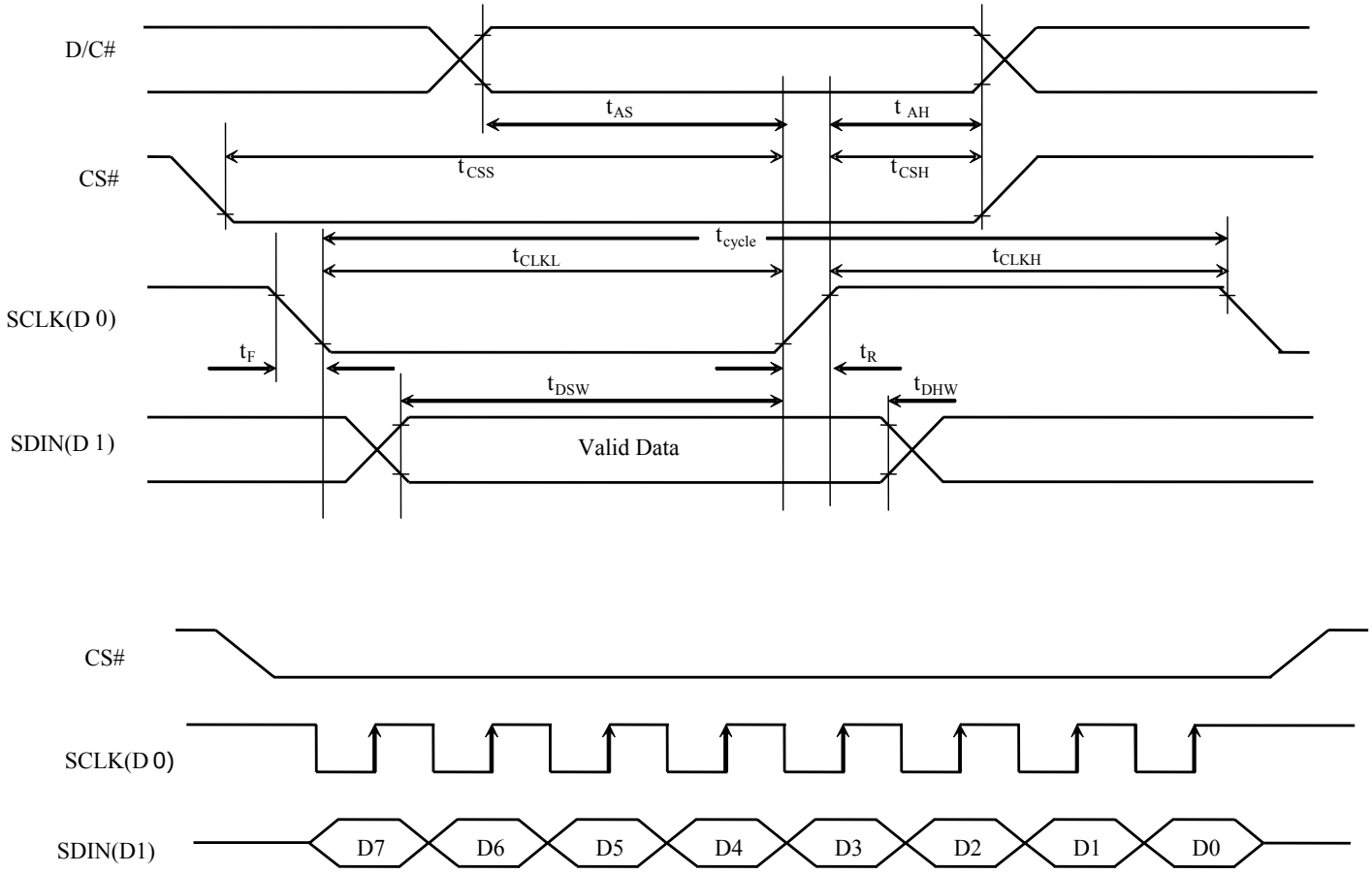
(1) when 8 bit used: D[7:0] instead; when 9 bit used: D[8:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 13-4 : Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

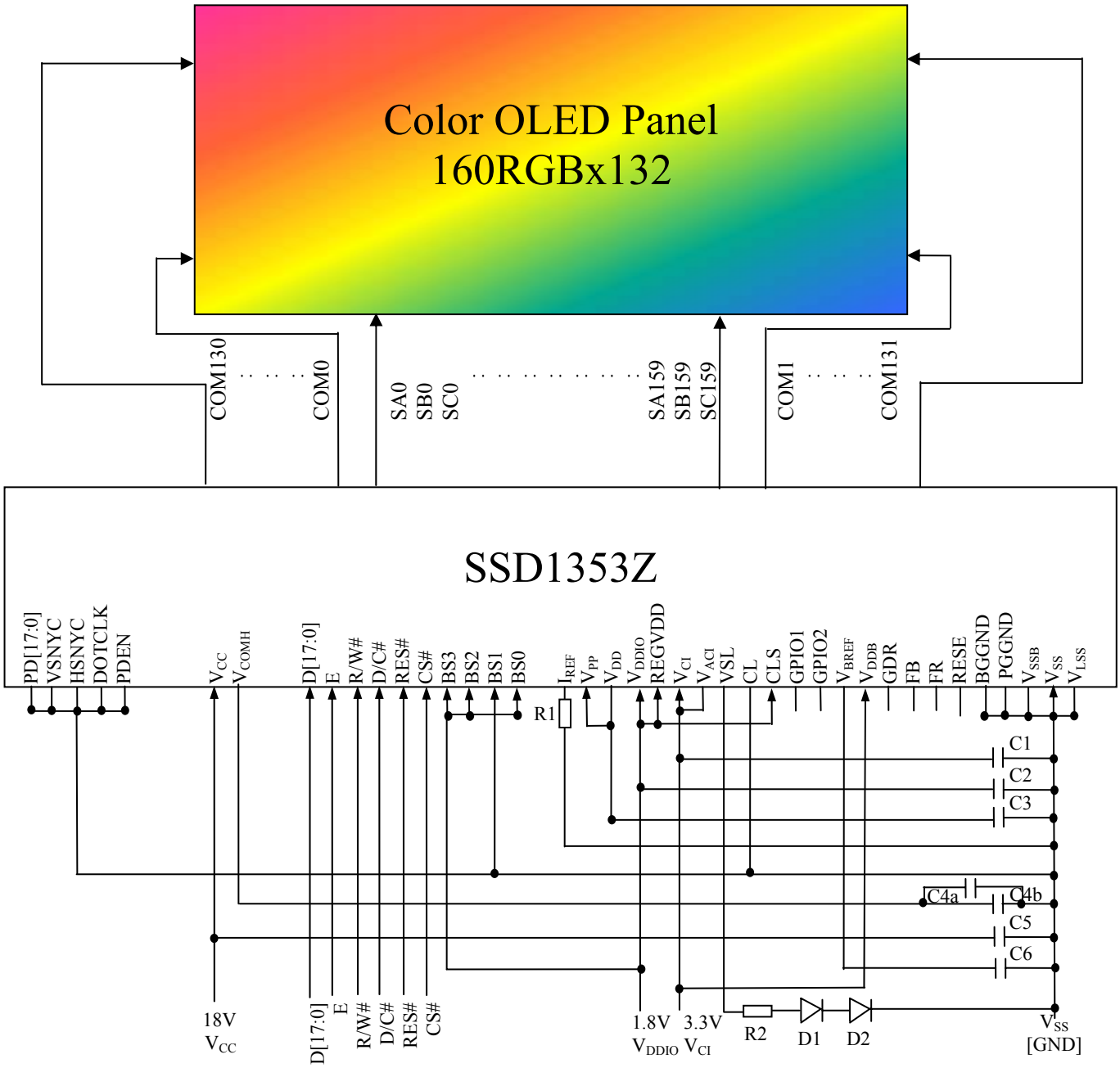
Figure 13-4 : Serial interface characteristics



14 APPLICATION EXAMPLE

Figure 14-1 : SSD1353 application example for 18-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 18-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} =3.3V(V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} =1.8V, external V_{CC} = 18V, I_{REF} = 10uA)

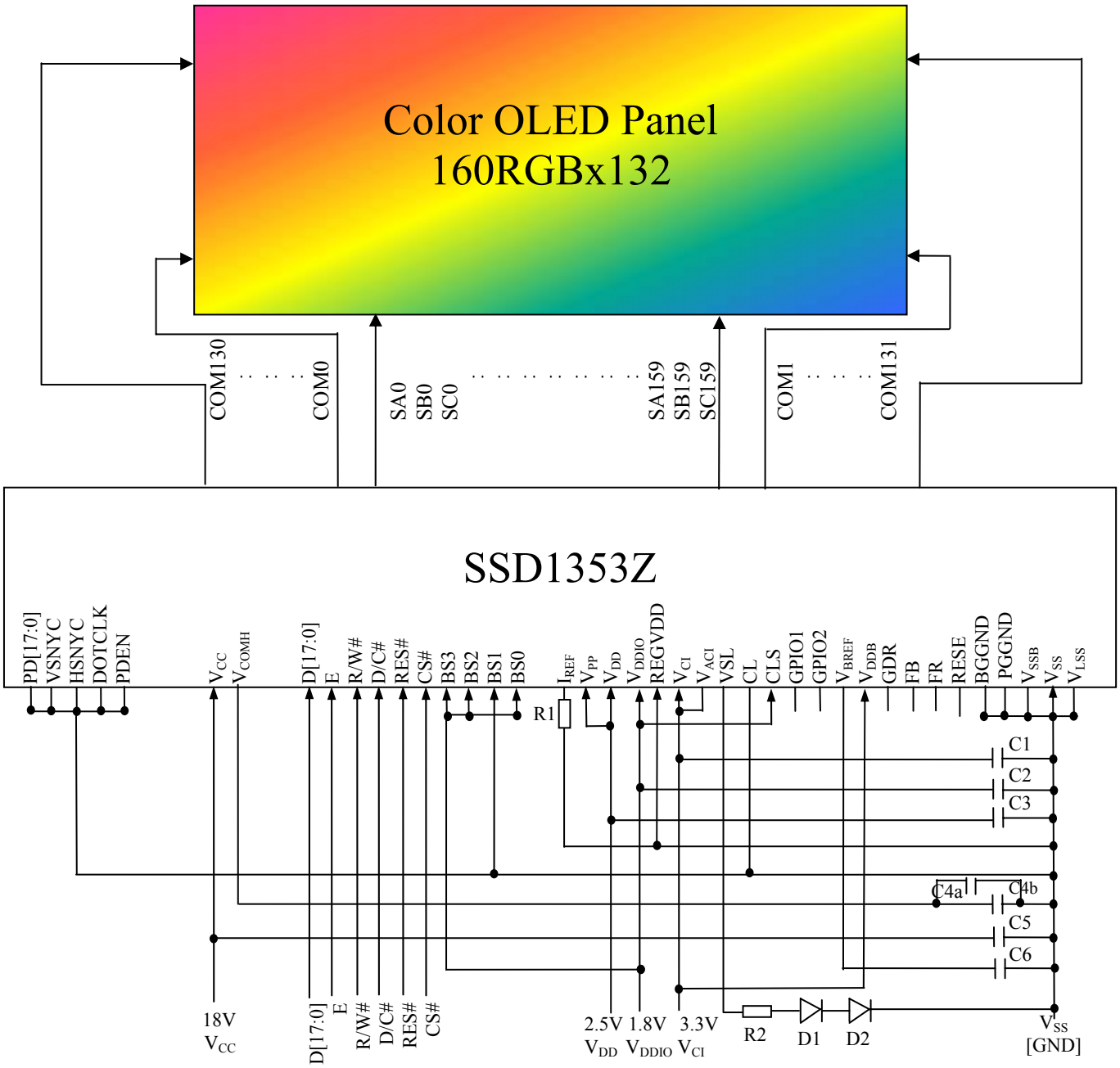


Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 18V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (18-3)/10u
= 1.5MΩ
R2 = 50Ω, 1/8W (1)
D1-D2= V_{th}=0.7V, 1N4148 (1)
C1-C3: 1uF, C4a,C5: 4.7uF, C4b: 0.1uF, C6 : 68nF (1)

Note
(1) The value is recommended value. Select appropriate value against module application.

Figure 14-2 : SSD1353 application example for 18-bit 6800-parallel interface mode (External V_{DD})

The configuration for 18-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} =3.3V (2.4V < V_{CI} <3.5V), External V_{DD} = 2.5V, V_{DDIO} =1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



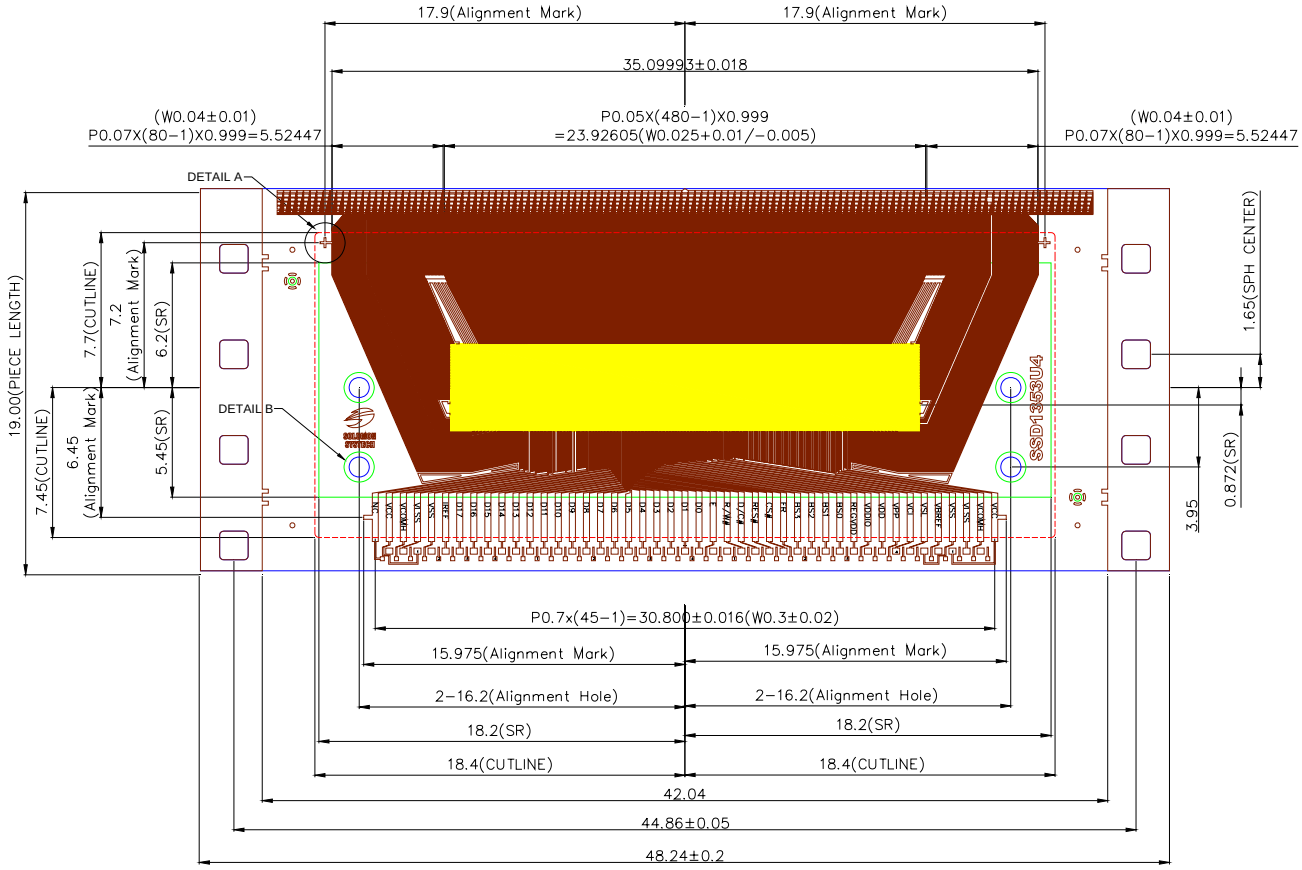
Voltage at I_{REF} = V_{CC} – 3V. For V_{CC} = 18V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (18-3)/10u
= 1.5MΩ
R2 = 50Ω, 1/8W (1)
D1-D2= V_{th}=0.7V, 1N4148 (1)
C1-C3: 1uF, C4a,C5: 4.7uF , C4b=0.1uF, C6 : 68nF (1)

Note
(1) The value is recommended value. Select appropriate value against module application.

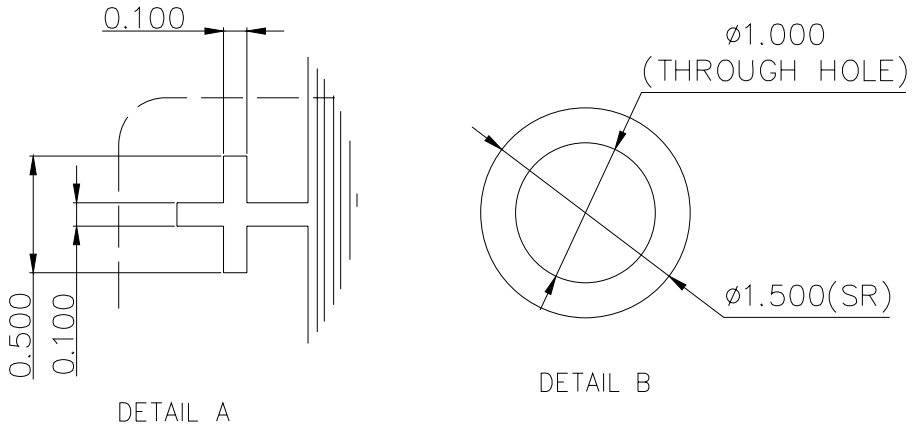
15 PACKAGE DIMENSION

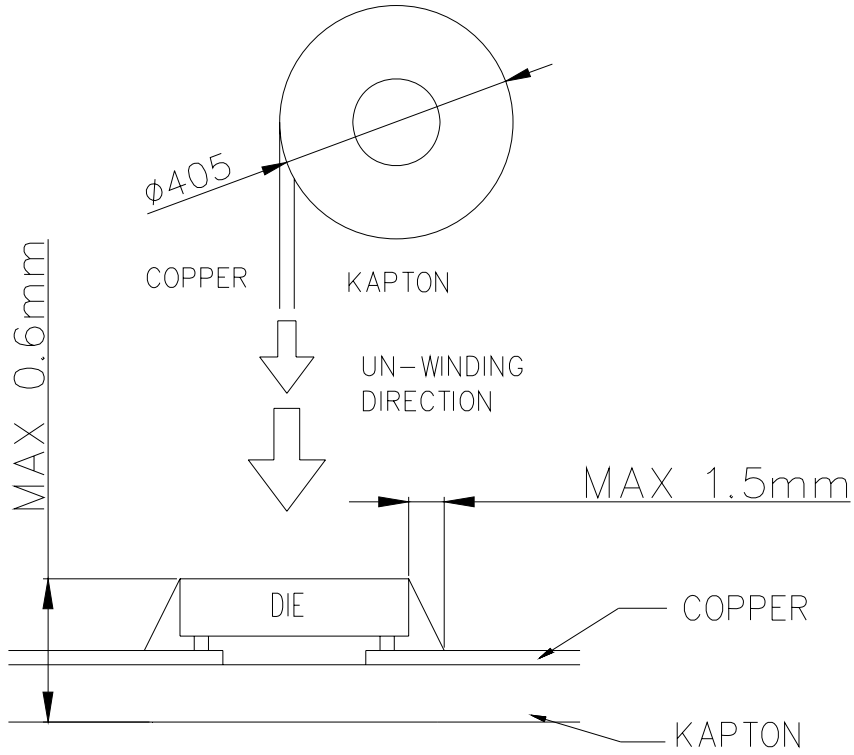
15.1 SSD1353U7R1 Detail Dimension

Figure 15-1: SSD1353U7R1 detail dimension



NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
   (OTHER TOLERANCE: ±0.200mm)
3. Sn PLATING 0.23±0.050mm
4. TAPSITE: 4 SPH, 19mm

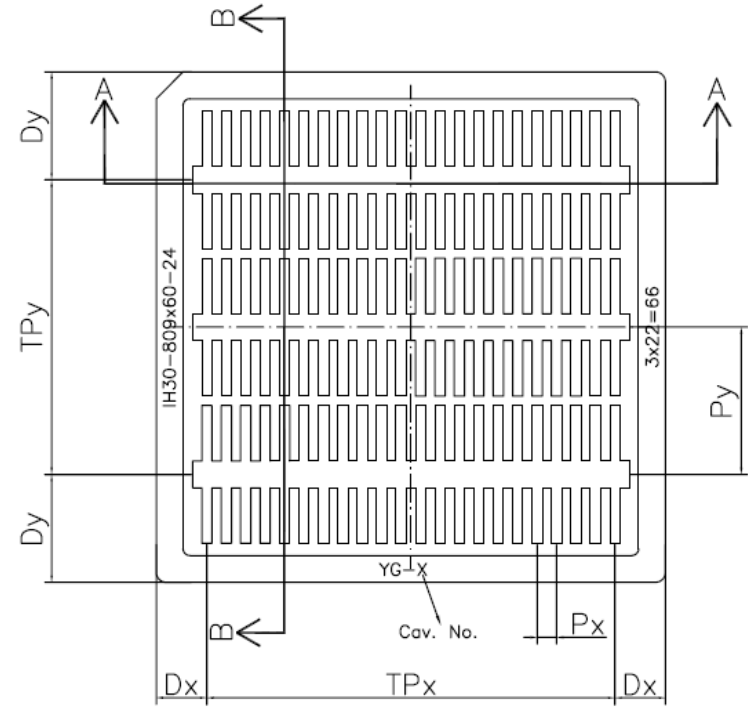


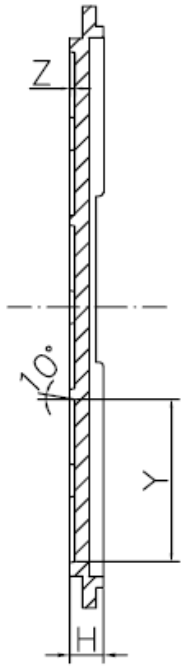


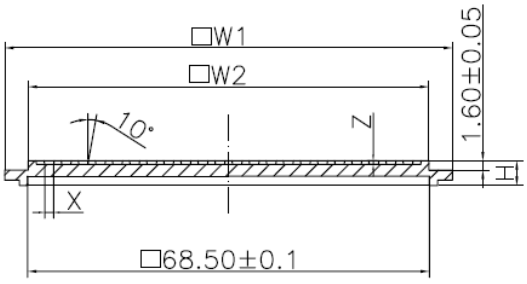
MIRROR DESIGN

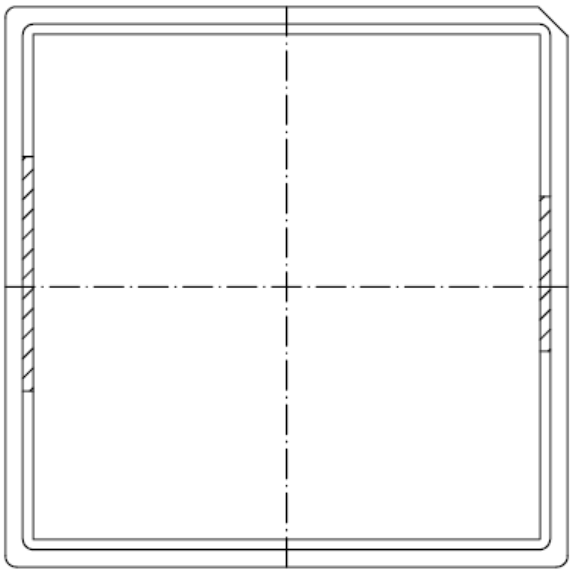
15.2 SSD1353Z Die Tray Information

Figure 15-2: SSD1353Z die tray dimension









	Spec
	mm (mil)
W1	76.00±0.10(2992)
W2	68.00±0.10(2677)
H	4.20±0.10 (165)
Dx	7.55±0.10 (297)
TPx	60.90±0.10(2398)
Dy	16.07±0.10 (633)
TPy	43.86±0.10(1727)
Px	2.90±0.05 (114)
Py	21.93±0.05 (863)
X	1.52±0.05 (60)
Y	20.55±0.05 (809)
Z	0.61±0.05 (24)
N	66(pocket number)

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol  . Hazardous Substances test report is available upon requested.