Dual Channel PWM Controller with Integrated Driver for IMVP8 CPU CORE Power Supply

General Description

The RT3607BC is an IMVP8 compliant CPU power controller which includes two voltage rails : a 4/3/2 phase synchronous Buck controller, the CORE VR and a 2 phase synchronous Buck controller, the AXG VR. The RT3607BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3607BC also features a quick response mechanism for optimized AVP performance during load transient. The RT3607BC supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT3607BC to communicate with Intel IMVP8 compliant CPU. The RT3607BC supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3607BC varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT3607BC integrates a high accuracy ADC for platform setting functions, such as quick response trigger level or over-current level. Besides, the setting function also supports this two rails address exchange. The RT3607BC provides VR ready output signals. It also features complete fault protection functions including over-voltage (OV), negative voltage (NV), over-current (OC) and under-voltage lockout (UVLO). The RT3607BC is available in the WQFN-60L 7x7 small foot print package.

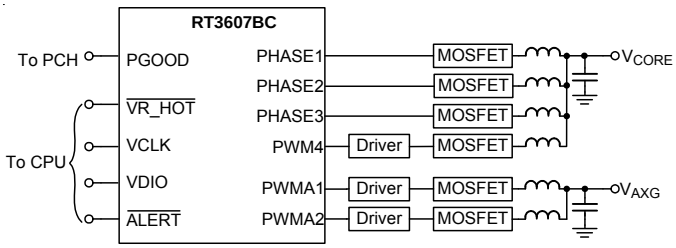
Features

- **Intel IMVP8 Serial VID Interface Compatible Power Management States**
- **4/3/2 Phase (CORE VR) + 2 Phase (AXG VR) PWM Controller**
- **3 Embedded MOSFET Drivers at the CORE VR**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Single Phase Operation**
- **Fast Transient Response**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **OVP, OCP, NVP, UVLO**
- **Slew Rate Setting/Address Flip Function**
- **Rail Address Flexibility**
- **DVID Enhancement**

Applications

- IMVP8 Intel CORE Supply
- Desktop Computer/ Servers Multi-phase CPU CORE Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT3607BC□□

Package Type
QW : WQFN-60L 7x7 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

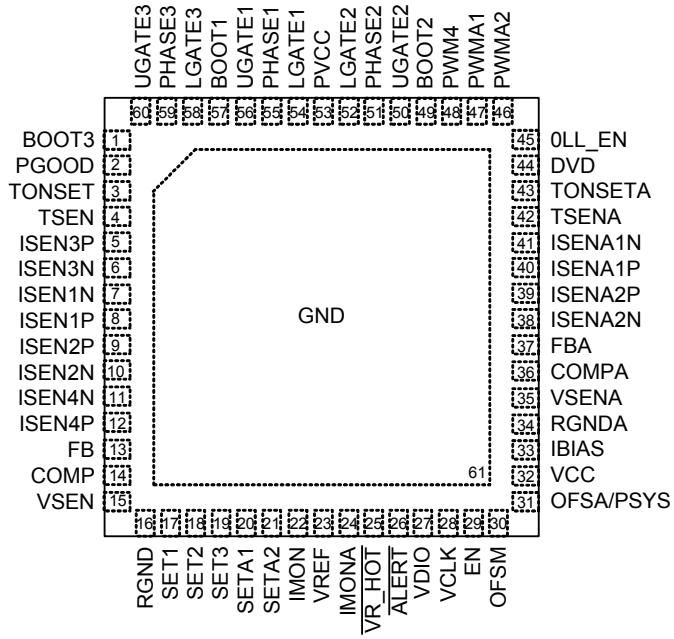
Marking Information

RT3607BCGQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-60L 7x7

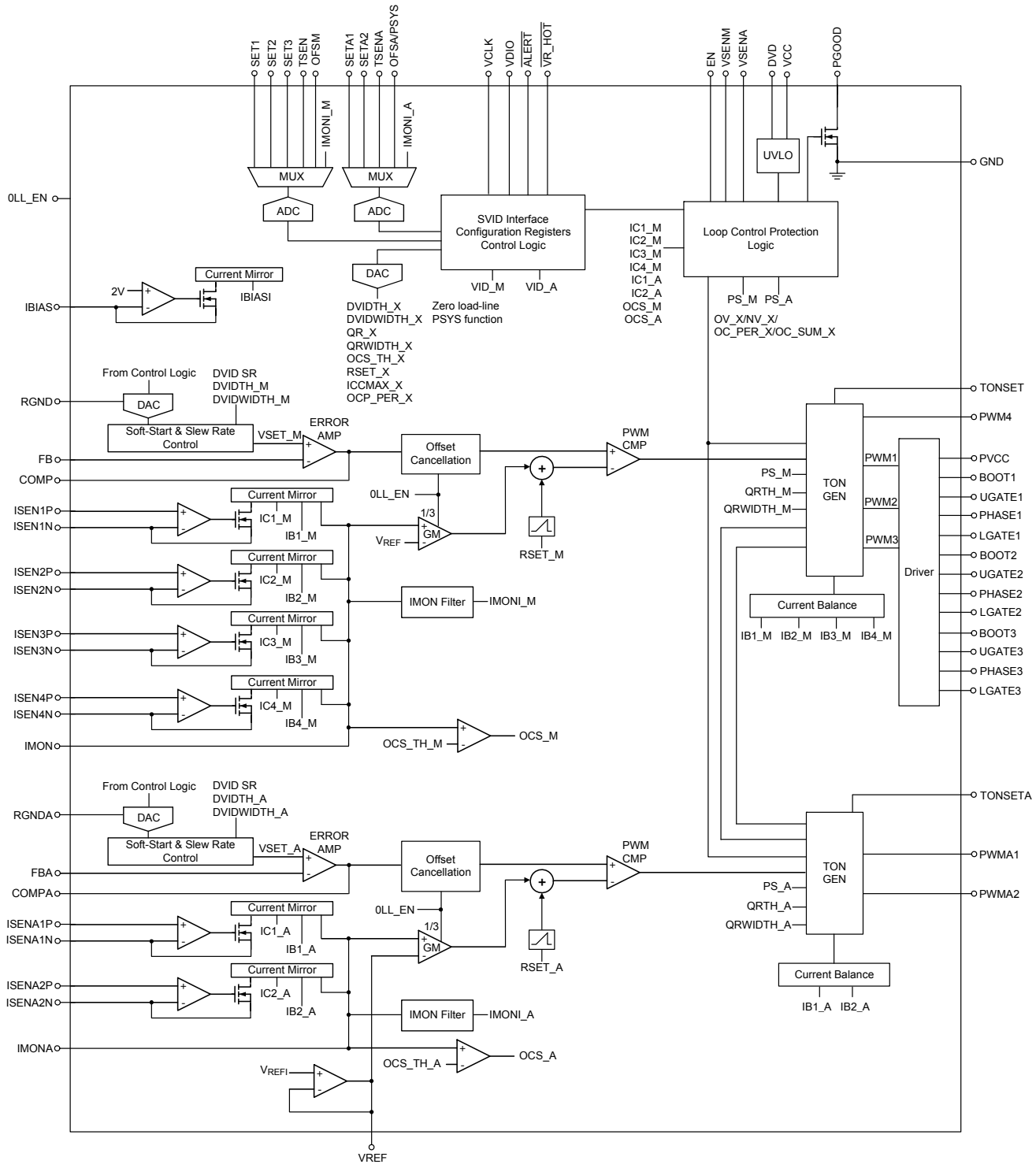
Functional Pin Description

Pin No	Pin Name	Pin Function
2	PGOOD	VR ready indicator.
3	TONSET	CORE rail VR on-time setting. An on-time setting resistor is connected from this pin to input voltage.
4	TSEN	Thermal sense input for CORE rail VR.
8, 9, 5, 12	ISEN[1:4]P	Positive current sense inputs of multi-phase CORE rail VR channel 1, 2, 3 and 4.
7, 10, 6, 11	ISEN[1:4]N	Negative current sense inputs of multi-phase CORE rail VR channel 1, 2, 3 and 4.
13	FB	Negative input of the error amplifier. This pin is for CORE rail VR output voltage feedback to controller.
14	COMP	CORE rail VR compensation. This pin is the error amplifier output pin.
15	VSEN	CORE rail VR voltage sense input. This pin is connected to the terminal of CORE rail VR output voltage.
16	RGND	Return ground for CORE rail VR. This pin is the negative node of the differential remote voltage sensing.
17	SET1	1st platform setting. Platform can use this pin to set Enable Zero load-line, DVID threshold and ICCMAX for CORE VR.
18	SET2	2nd platform setting. Platform can use this pin to set Ramp Setting, QRTH, and OCS for CORE VR. Moreover, SET2 pin features a special function for users to confirm the soldering condition of the controller under zero VBOOT condition. Connect the SET2 pin to 5V and turn on the EN pin, if the soldering is good, both rails output 0.8V.

Pin No	Pin Name	Pin Function
19	SET3	3rd platform setting. Platform can use this pin to set DVID width, QRWIDTH and Enable PSYS function for Main VR and AXG VR.
20	SETA1	1st platform setting. Platform can use this pin to set DVID threshold and ICCMAX for AXG rail VR.
21	SETA2	2nd platform setting. Platform can use this pin to set Ramp Setting, QRTH, and OCS for AXG rail VR.
22	IMON	CORE rail VR current monitor output. This pin outputs a voltage proportional to the loading current.
23	VREF	Fixed 0.6V output reference voltage. This voltage is only used to offset the output voltage of IMON pin. Between this pin and GND must be placed a RC circuit with R = 3.9Ω and C = 0.47μF.
24	IMONA	AXG rail VR current monitor output. This pin outputs a voltage proportional to the loading current.
25	$\overline{\text{VR\_HOT}}$	Thermal monitor output. This pin is active low.
26	$\overline{\text{ALERT}}$	SVID alert. (Active low)
27	VDIO	VR and CPU data transmission interface.
28	VCLK	Synchronous clock from the CPU.
29	EN	VR enable control input.
30	OFSM	Output voltage offset setting for CORE rail VR.
31	OFSA/PSYS	Output voltage offset setting for AXG rail VR and system input power monitor. Place the PSYS resistor as close to the IC as possible. User can disable PSYS function by simply connecting PSYS pin to GND and SET3 pin setting disable PSYS function.
32	VCC	Controller power supply. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor is placed as close to VR controller as possible.
33	IBIAS	Internal bias current setting. Connect a 100kΩ resistor from this pin tied to GND to set the internal current. Don't connect a bypass pass capacitor from this pin to GND.
34	RGNDA	Return ground for AXG rail VR. This pin is the negative node of the differential remote voltage sensing.
35	VSENA	AXG rail VR voltage sense input. This pin is connected to the terminal of AXG rail VR output voltage.
36	COMPA	AXG rail VR COMPENSATION. This pin is the error amplifier output pin.
37	FBA	Negative input of the error amplifier. This pin is for AXG rail VR output voltage feedback to controller.
40, 39	ISENA[1:2]P	Positive current sense input of multi-phase AXG rail VR channel 1, 2.
41, 38	ISENA[1:2]N	Negative current sense input of multi-phase AXG rail VR channel 1, 2.
42	TSENA	Thermal sense input for AXG rail VR.
43	TONSETA	AXG rail VR on-time setting. An on-time setting resistor is connected from this pin to input voltage.
44	DVD	Divided input voltage detection of power stage. Connect this pin to a voltage divider from input voltage of power stage to detect input voltage.

Pin No	Pin Name	Pin Function
45	0LL_EN	Zero load-line function setting. Connect this pin to 5V can enable zero load-line function. Connect this pin to GND can disable zero load-line function.
46	PWMA2	PWM output for AXG rail VR channel 2.
47	PWMA1	PWM output for AXG rail VR channel 1.
48	PWM4	PWM output for CORE rail VR channel 4.
53	PVCC	Driver power supply input. Connect this pin to GND by a minimum 2.2μF ceramic Capacitor.
54, 52 ,58	LGATE[1:3]	Low-side driver output for CORE rail VR. This pin drives the gate of low-side MOSFET.
55, 51, 59	PHASE[1:3]	Switch node of high-side driver for CORE rail VR. Connect the pin to high-side MOSFET source together with the low-side MOSFET drain and inductor.
56, 50, 60	UGATE[1:3]	High-side drive outputs for CORE rail VR. Connect the pin to the gate of high-side MOSFET.
57, 49, 1	BOOT[1:3]	Bootstrap supply for high-side gate MOSFET driver for CORE rail VR.
61 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT3607BC adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, the RT3607BC generates an on-time width to achieve PWM modulation.

TON GEN/Driver Interface

Generate the PWM1 to PWM4 sequentially according to the phase control signal from the Loop Control/Protection Logic. Pulse width is determined by current balance result and TONSET pin setting. Once quick response mechanism is triggered, VR allows all PWM to turn on at the same time. PWM status is also controlled by Protection Logic. Different protections may cause different PWM status (Both High-Z or LG turn-on).

SVID Interface/Configuration Registers/Control Logic

The interface receives the SVID signal from CPU and sends the relative signals to Loop Control/Protection Logic for loop control to execute the action by CPU. The registers save the pin setting data from ADC output. The Control Logic controls the ADC timing and generates the digital code of the VID for VSEN voltage.

Loop Control/Protection Logic

It controls the power on sequence, the protection behavior, and the operational phase number.

MUX and ADC

The MUX supports the inputs from SET1, SET2, SET3, SETA1, SETA2, IMONI_M, IMONI_A, TSEN or TSENA. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the DVD and VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of DAC according to the SetVID fast or SetVID slow.

Error Amp

Error amplifier generates COMP/COMPA signal by the difference between VSEN/VSENA and FB/FBA.

RSET/RSETA

The Ramp generator is designed to improve noise immunity and reduce jitter.

PWM CMP

The PWM comparator compares COMP signal and current feedback signal to generate a signal for TON trigger.

IMON Filter

IMON Filter is used to average sum current signal by analog RC filter.

Table 1. IMVP8 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	0	0	0	0	0	1	01	0.25
0	0	0	0	0	0	1	0	02	0.255
0	0	0	0	0	0	1	1	03	0.26
0	0	0	0	0	1	0	0	04	0.265
0	0	0	0	0	1	0	1	05	0.27
0	0	0	0	0	1	1	0	06	0.275
0	0	0	0	0	1	1	1	07	0.28
0	0	0	0	1	0	0	0	08	0.285
0	0	0	0	1	0	0	1	09	0.29
0	0	0	0	1	0	1	0	0A	0.295
0	0	0	0	1	0	1	1	0B	0.3
0	0	0	0	1	1	0	0	0C	0.305
0	0	0	0	1	1	0	1	0D	0.31
0	0	0	0	1	1	1	0	0E	0.315
0	0	0	0	1	1	1	1	0F	0.32
0	0	0	1	0	0	0	0	10	0.325
0	0	0	1	0	0	0	1	11	0.33
0	0	0	1	0	0	1	0	12	0.335
0	0	0	1	0	0	1	1	13	0.34
0	0	0	1	0	1	0	0	14	0.345
0	0	0	1	0	1	0	1	15	0.35
0	0	0	1	0	1	1	0	16	0.355
0	0	0	1	0	1	1	1	17	0.36
0	0	0	1	1	0	0	0	18	0.365
0	0	0	1	1	0	0	1	19	0.37
0	0	0	1	1	0	1	0	1A	0.375
0	0	0	1	1	0	1	1	1B	0.38
0	0	0	1	1	1	0	0	1C	0.385
0	0	0	1	1	1	0	1	1D	0.39
0	0	0	1	1	1	1	0	1E	0.395
0	0	0	1	1	1	1	1	1F	0.4
0	0	1	0	0	0	0	0	20	0.405
0	0	1	0	0	0	0	1	21	0.41
0	0	1	0	0	0	1	0	22	0.415
0	0	1	0	0	0	1	1	23	0.42
0	0	1	0	0	1	0	0	24	0.425

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	0	1	0	0	1	0	1	25	0.43
0	0	1	0	0	1	1	0	26	0.435
0	0	1	0	0	1	1	1	27	0.44
0	0	1	0	1	0	0	0	28	0.445
0	0	1	0	1	0	0	1	29	0.45
0	0	1	0	1	0	1	0	2A	0.455
0	0	1	0	1	0	1	1	2B	0.46
0	0	1	0	1	1	0	0	2C	0.465
0	0	1	0	1	1	0	1	2D	0.47
0	0	1	0	1	1	1	0	2E	0.475
0	0	1	0	1	1	1	1	2F	0.48
0	0	1	1	0	0	0	0	30	0.485
0	0	1	1	0	0	0	1	31	0.49
0	0	1	1	0	0	1	0	32	0.495
0	0	1	1	0	0	1	1	33	0.5
0	0	1	1	0	1	0	0	34	0.505
0	0	1	1	0	1	0	1	35	0.51
0	0	1	1	0	1	1	0	36	0.515
0	0	1	1	0	1	1	1	37	0.52
0	0	1	1	1	0	0	0	38	0.525
0	0	1	1	1	0	0	1	39	0.53
0	0	1	1	1	0	1	0	3A	0.535
0	0	1	1	1	0	1	1	3B	0.54
0	0	1	1	1	1	0	0	3C	0.545
0	0	1	1	1	1	0	1	3D	0.55
0	0	1	1	1	1	1	0	3E	0.555
0	0	1	1	1	1	1	1	3F	0.56
0	1	0	0	0	0	0	0	40	0.565
0	1	0	0	0	0	0	1	41	0.57
0	1	0	0	0	0	1	0	42	0.575
0	1	0	0	0	0	1	1	43	0.58
0	1	0	0	0	1	0	0	44	0.585
0	1	0	0	0	1	0	1	45	0.59
0	1	0	0	0	1	1	0	46	0.595
0	1	0	0	0	1	1	1	47	0.6
0	1	0	0	1	0	0	0	48	0.605
0	1	0	0	1	0	0	1	49	0.61

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	0	0	1	0	1	0	4A	0.615
0	1	0	0	1	0	1	1	4B	0.62
0	1	0	0	1	1	0	0	4C	0.625
0	1	0	0	1	1	0	1	4D	0.63
0	1	0	0	1	1	1	0	4E	0.635
0	1	0	0	1	1	1	1	4F	0.64
0	1	0	1	0	0	0	0	50	0.645
0	1	0	1	0	0	0	1	51	0.65
0	1	0	1	0	0	1	0	52	0.655
0	1	0	1	0	0	1	1	53	0.66
0	1	0	1	0	1	0	0	54	0.665
0	1	0	1	0	1	0	1	55	0.67
0	1	0	1	0	1	1	0	56	0.675
0	1	0	1	0	1	1	1	57	0.68
0	1	0	1	1	0	0	0	58	0.685
0	1	0	1	1	0	0	1	59	0.69
0	1	0	1	1	0	1	0	5A	0.695
0	1	0	1	1	0	1	1	5B	0.7
0	1	0	1	1	1	0	0	5C	0.705
0	1	0	1	1	1	0	1	5D	0.71
0	1	0	1	1	1	1	0	5E	0.715
0	1	0	1	1	1	1	1	5F	0.72
0	1	1	0	0	0	0	0	60	0.725
0	1	1	0	0	0	0	1	61	0.73
0	1	1	0	0	0	1	0	62	0.735
0	1	1	0	0	0	1	1	63	0.74
0	1	1	0	0	1	0	0	64	0.745
0	1	1	0	0	1	0	1	65	0.75
0	1	1	0	0	1	1	0	66	0.755
0	1	1	0	0	1	1	1	67	0.76
0	1	1	0	1	0	0	0	68	0.765
0	1	1	0	1	0	0	1	69	0.77
0	1	1	0	1	0	1	0	6A	0.775
0	1	1	0	1	0	1	1	6B	0.78
0	1	1	0	1	1	0	0	6C	0.785
0	1	1	0	1	1	0	1	6D	0.79
0	1	1	0	1	1	1	0	6E	0.795

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
0	1	1	0	1	1	1	1	6F	0.8
0	1	1	1	0	0	0	0	70	0.805
0	1	1	1	0	0	0	1	71	0.81
0	1	1	1	0	0	1	0	72	0.815
0	1	1	1	0	0	1	1	73	0.82
0	1	1	1	0	1	0	0	74	0.825
0	1	1	1	0	1	0	1	75	0.83
0	1	1	1	0	1	1	0	76	0.835
0	1	1	1	0	1	1	1	77	0.84
0	1	1	1	1	0	0	0	78	0.845
0	1	1	1	1	0	0	1	79	0.85
0	1	1	1	1	0	1	0	7A	0.855
0	1	1	1	1	0	1	1	7B	0.86
0	1	1	1	1	1	0	0	7C	0.865
0	1	1	1	1	1	0	1	7D	0.87
0	1	1	1	1	1	1	0	7E	0.875
0	1	1	1	1	1	1	1	7F	0.88
1	0	0	0	0	0	0	0	80	0.885
1	0	0	0	0	0	0	1	81	0.89
1	0	0	0	0	0	1	0	82	0.895
1	0	0	0	0	0	1	1	83	0.9
1	0	0	0	0	1	0	0	84	0.905
1	0	0	0	0	1	0	1	85	0.91
1	0	0	0	0	1	1	0	86	0.915
1	0	0	0	0	1	1	1	87	0.92
1	0	0	0	1	0	0	0	88	0.925
1	0	0	0	1	0	0	1	89	0.93
1	0	0	0	1	0	1	0	8A	0.935
1	0	0	0	1	0	1	1	8B	0.94
1	0	0	0	1	1	0	0	8C	0.945
1	0	0	0	1	1	0	1	8D	0.95
1	0	0	0	1	1	1	0	8E	0.955
1	0	0	0	1	1	1	1	8F	0.96
1	0	0	1	0	0	0	0	90	0.965
1	0	0	1	0	0	0	1	91	0.97
1	0	0	1	0	0	1	0	92	0.975
1	0	0	1	0	0	1	1	93	0.98

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	0	1	0	1	0	0	94	0.985
1	0	0	1	0	1	0	1	95	0.99
1	0	0	1	0	1	1	0	96	0.995
1	0	0	1	0	1	1	1	97	1
1	0	0	1	1	0	0	0	98	1.005
1	0	0	1	1	0	0	1	99	1.01
1	0	0	1	1	0	1	0	9A	1.015
1	0	0	1	1	0	1	1	9B	1.02
1	0	0	1	1	1	0	0	9C	1.025
1	0	0	1	1	1	0	1	9D	1.03
1	0	0	1	1	1	1	0	9E	1.035
1	0	0	1	1	1	1	1	9F	1.04
1	0	1	0	0	0	0	0	A0	1.045
1	0	1	0	0	0	0	1	A1	1.05
1	0	1	0	0	0	1	0	A2	1.055
1	0	1	0	0	0	1	1	A3	1.06
1	0	1	0	0	1	0	0	A4	1.065
1	0	1	0	0	1	0	1	A5	1.07
1	0	1	0	0	1	1	0	A6	1.075
1	0	1	0	0	1	1	1	A7	1.08
1	0	1	0	1	0	0	0	A8	1.085
1	0	1	0	1	0	0	1	A9	1.09
1	0	1	0	1	0	1	0	AA	1.095
1	0	1	0	1	0	1	1	AB	1.1
1	0	1	0	1	1	0	0	AC	1.105
1	0	1	0	1	1	0	1	AD	1.11
1	0	1	0	1	1	1	0	AE	1.115
1	0	1	0	1	1	1	1	AF	1.12
1	0	1	1	0	0	0	0	B0	1.125
1	0	1	1	0	0	0	1	B1	1.13
1	0	1	1	0	0	1	0	B2	1.135
1	0	1	1	0	0	1	1	B3	1.14
1	0	1	1	0	1	0	0	B4	1.145
1	0	1	1	0	1	0	1	B5	1.15
1	0	1	1	0	1	1	0	B6	1.155
1	0	1	1	0	1	1	1	B7	1.16
1	0	1	1	1	0	0	0	B8	1.165

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	0	1	1	1	0	0	1	B9	1.17
1	0	1	1	1	0	1	0	BA	1.175
1	0	1	1	1	0	1	1	BB	1.18
1	0	1	1	1	1	0	0	BC	1.185
1	0	1	1	1	1	0	1	BD	1.19
1	0	1	1	1	1	1	0	BE	1.195
1	0	1	1	1	1	1	1	BF	1.2
1	1	0	0	0	0	0	0	C0	1.205
1	1	0	0	0	0	0	1	C1	1.21
1	1	0	0	0	0	1	0	C2	1.215
1	1	0	0	0	0	1	1	C3	1.22
1	1	0	0	0	1	0	0	C4	1.225
1	1	0	0	0	1	0	1	C5	1.23
1	1	0	0	0	1	1	0	C6	1.235
1	1	0	0	0	1	1	1	C7	1.24
1	1	0	0	1	0	0	0	C8	1.245
1	1	0	0	1	0	0	1	C9	1.25
1	1	0	0	1	0	1	0	CA	1.255
1	1	0	0	1	0	1	1	CB	1.26
1	1	0	0	1	1	0	0	CC	1.265
1	1	0	0	1	1	0	1	CD	1.27
1	1	0	0	1	1	1	0	CE	1.275
1	1	0	0	1	1	1	1	CF	1.28
1	1	0	1	0	0	0	0	D0	1.285
1	1	0	1	0	0	0	1	D1	1.29
1	1	0	1	0	0	1	0	D2	1.295
1	1	0	1	0	0	1	1	D3	1.3
1	1	0	1	0	1	0	0	D4	1.305
1	1	0	1	0	1	0	1	D5	1.31
1	1	0	1	0	1	1	0	D6	1.315
1	1	0	1	0	1	1	1	D7	1.32
1	1	0	1	1	0	0	0	D8	1.325
1	1	0	1	1	0	0	1	D9	1.33
1	1	0	1	1	0	1	0	DA	1.335
1	1	0	1	1	0	1	1	DB	1.34
1	1	0	1	1	1	0	0	DC	1.345
1	1	0	1	1	1	0	1	DD	1.35

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Voltage (V)
1	1	0	1	1	1	1	0	DE	1.355
1	1	0	1	1	1	1	1	DF	1.36
1	1	1	0	0	0	0	0	E0	1.365
1	1	1	0	0	0	0	1	E1	1.37
1	1	1	0	0	0	1	0	E2	1.375
1	1	1	0	0	0	1	1	E3	1.38
1	1	1	0	0	1	0	0	E4	1.385
1	1	1	0	0	1	0	1	E5	1.39
1	1	1	0	0	1	1	0	E6	1.395
1	1	1	0	0	1	1	1	E7	1.4
1	1	1	0	1	0	0	0	E8	1.405
1	1	1	0	1	0	0	1	E9	1.41
1	1	1	0	1	0	1	0	EA	1.415
1	1	1	0	1	0	1	1	EB	1.42
1	1	1	0	1	1	0	0	EC	1.425
1	1	1	0	1	1	0	1	ED	1.43
1	1	1	0	1	1	1	0	EE	1.435
1	1	1	0	1	1	1	1	EF	1.44
1	1	1	1	0	0	0	0	F0	1.445
1	1	1	1	0	0	0	1	F1	1.45
1	1	1	1	0	0	1	0	F2	1.455
1	1	1	1	0	0	1	1	F3	1.46
1	1	1	1	0	1	0	0	F4	1.465
1	1	1	1	0	1	0	1	F5	1.47
1	1	1	1	0	1	1	0	F6	1.475
1	1	1	1	0	1	1	1	F7	1.48
1	1	1	1	1	0	0	0	F8	1.485
1	1	1	1	1	0	0	1	F9	1.49
1	1	1	1	1	0	1	0	FA	1.495
1	1	1	1	1	0	1	1	FB	1.5
1	1	1	1	1	1	0	0	FC	1.505
1	1	1	1	1	1	0	1	FD	1.51
1	1	1	1	1	1	1	0	FE	1.515
1	1	1	1	1	1	1	1	FF	1.52

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 15V
- RGND to GND ---------- –0.3V to 0.3V
- TONSET to GND ---------- –0.3V to 28
- BOOTx to PHASEx ---------- –0.3V to 15V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –10V to 35V
- LGATEx to GND
  - DC ---------- –0.3V to (VCC + 0.3V)
  - <20ns ---------- –2V to (VCC + 0.3V)
- UGATEx to GND
  - DC ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - <20ns ---------- (V_{PHASE} – 2V) to (V_{BOOT} + 0.3V)
- Other Pins ---------- –0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-60L 7x7 ---------- 3.92W
- Package Thermal Resistance (Note 2)
  - WQFN-60L 7x7, θ_{JA} ---------- 25.5°C/W
  - WQFN-60L 7x7, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{VCC}	V_{EN} = H, no switching	--	13	--	mA
Supply Current at PS4	I_{VCC_PS4}	V_{EN} = H, no switching	--	0.1	--	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Reference and DAC						
DAC Accuracy	V_{FB}	VDAC = 0.75V – 1.52V	–0.5%	0	0.5%	% of VID
		VDAC = 0.5V – 0.745V	–8	0	8	mV
		VDAC = 0.25V – 0.495V	–10	0	10	
Slew Rate						
Dynamic VID Slew Rate	SR (S Line)	Set VID fast	--	11.25	--	mV/μs
		Set VID slow	--	5.625	--	
EA						
DC Gain	EAGAIN	R_L = 47kΩ	70	--	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	5	--	MHz
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
Max Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	5	--	mA
Load Line Current Gain Amplifier						
Input Offset Voltage	V_{ILOFS}	V_{IMON} = 1V	–5	--	5	mV
Current Gain	AILGAIN	V_{IMON} – V_{VREF} = 1V V_{FB} = V_{COMP} = 1V	--	1/3	--	A/A
Current Sensing Amplifier						
Input Offset Voltage	V_{OSCS}		–0.5	--	0.5	mV
Impedance at Positive Input	RISENxP		1	--	--	MΩ
Current Mirror Gain	AMIRROR	Current Mirror Gain = IIMON/IISENx IISENx = Current through Rcs (680Ω)	0.97	1	1.03	A/A
TON Setting						
TON Pin Voltage	V_{TON}	I_{RTON} = 26.8μA, VDAC = 1V	0.9	1	1.1	V
On-Time Setting	t_{ON}	I_{RTON} = 26.8μA, VDAC = 1V	189	210	231	ns
Input Current Range	I_{RTON}	VDAC = 1V	6	--	70	μA
Minimum Off-Time	t_{OFF}	VDAC = 1V	--	180	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 100kΩ	1.9	2	2.1	V
Protections						
Under-Voltage Lockout Threshold	V_{UVLO}	Falling edge	3.95	4.05	4.15	V
	ΔV_{UVLO}	Rising edge hysteresis	--	190	--	mV
Over-Voltage Protection Threshold	V_{OV}	Respect to VID voltage	VID + 300	VID + 350	VID + 400	mV
		VID < 1V, OVP threshold is fixed to 1.35V	1300	1350	1400	mV
Negative Voltage Protection Threshold	V_{NV}		−100	−70	--	mV
EN and VR_READY						
EN Input Voltage	V_{IH}		0.7	--	--	V
	V_{IL}		--	--	0.3	V
Leakage Current of EN			−1	--	1	μA
PGOOD Pull Low Voltage	V_{PGOOD}	I_{VR_Ready} = 10mA	--	--	0.13	V
OLL_EN						
OLL_EN Input Voltage	V_{IH}		4.35	--	--	V
	V_{IL}		--		1	
DVD (Note 5)						
DVD Input High Voltage	V_{IH}	V_{DVD} = 2V or above, VR judge VIN high	2	--	--	V
DVD Input Low Voltage	V_{IL}	V_{DVD} = 1.3V or below, VR judge VIN low	--	--	1.3	V
Serial VID and $\overline{\text{VR\_HOT}}$						
VCLK, VDIO	V_{IH}	Respect to INTEL Spec. with 50mV hysteresis	0.65	--	--	V
	V_{IL}		--	--	0.45	
Leakage Current of VCLK, VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR\_HOT}}$	I_{LEAK_IN}		−1	--	1	μA
VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR\_HOT}}$ Pull Low Voltage		I_{VDIO} = 10mA	--	--	0.13	V
		$I_{\overline{ALERT}}$ = 10mA				
		$I_{\overline{VR\_HOT}}$ = 10mA				
VREF						
VREF Voltage	V_{REF}		0.55	0.6	0.65	V
ADC						
Digital IMON Setting	V_{IMON}	V_{IMON} – V_{IMON_INI} = 1.6V	--	255	--	Decimal
		V_{IMON} – V_{IMON_INI} = 0.8V	--	128	--	Decimal
		V_{IMON} – V_{IMON_INI} = 0V	--	0	--	Decimal

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PSYS						
Digital PSYS Setting	V_{PSYS}	V_{PSYS} = 3.2V	--	255	--	Decimal
		V_{PSYS} = 1.6V	--	128	--	
		V_{PSYS} = 0V	--	0	--	
Update Period	t_{IMON}		--	125	--	μs
TSEN Threshold for Tmp_Zone[7] Transition	V_{TSEN}	100°C	--	1.092	--	V
TSEN Threshold for Tmp_Zone[6] Transition		97°C	--	1.132	--	
TSEN Threshold for Tmp_Zone[5] Transition		94°C	--	1.176	--	
TSEN Threshold for Tmp_Zone[4] Transition		91°C	--	1.226	--	
TSEN Threshold for Tmp_Zone[3] Transition		88°C	--	1.283	--	
TSEN Threshold for Tmp_Zone[2] Transition		85°C	--	1.346	--	
TSEN Threshold for Tmp_Zone[1] Transition		82°C	--	1.418	--	
TSEN Threshold for Tmp_Zone[0] Transition		75°C	--	1.624	--	
Update Period	t_{TSEN}		--	100	--	μs
Digital Code of ICCMAX	CICCMAX1	V_{REF} = 3.2V, V_{SETI} = 0.404V, V_{SETA1} = 0.404V	61	64	67	Decimal
	CICCMAX2	V_{REF} = 3.2V, V_{SETI} = 0.804V, V_{SETA1} = 0.804V	125	128	131	Decimal
	CICCMAX3	V_{REF} = 3.2V, V_{SETI} = 1.592V, V_{SETA1} = 1.592V	251	254	255	Decimal
Timing						
UGATEx Rising Time	t_{UGATEr}	3nF load	--	25	--	ns
UGATEx Falling Time	t_{UGATEf}	3nF load	--	12	--	ns
LGATEx Rising Time	t_{LGATEr}	3nF load	--	24	--	ns
LGATEx Falling Time	t_{LGATEf}	3nF load	--	10	--	ns
Propagation Delay	$t_{UGATEpgh}$	$V_{BOOTx} - V_{PHASEx}$ = 12V See Timing Diagram	--	60	--	ns
	$t_{UGATEpdl}$		--	22	--	
	$t_{LGATEpdh}$	See Timing Diagram	--	30	--	ns
	$t_{LGATEpdl}$		--	8	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output						
UGATEx Drive Source	$R_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 12V, I_{Source} = 100mA	--	1.7	--	Ω
UGATEx Drive Sink	$R_{UGATEsk}$	V_{BOOT} – V_{PHASE} = 12V, I_{Sink} = 100mA	--	1.4	--	Ω
LGATEx Drive Source	$R_{LGATEsr}$	I_{Source} = 100mA	--	1.6	--	Ω
LGATEx Drive Sink	$R_{LGATEsk}$	I_{Sink} = 100mA	--	1.1	--	Ω
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

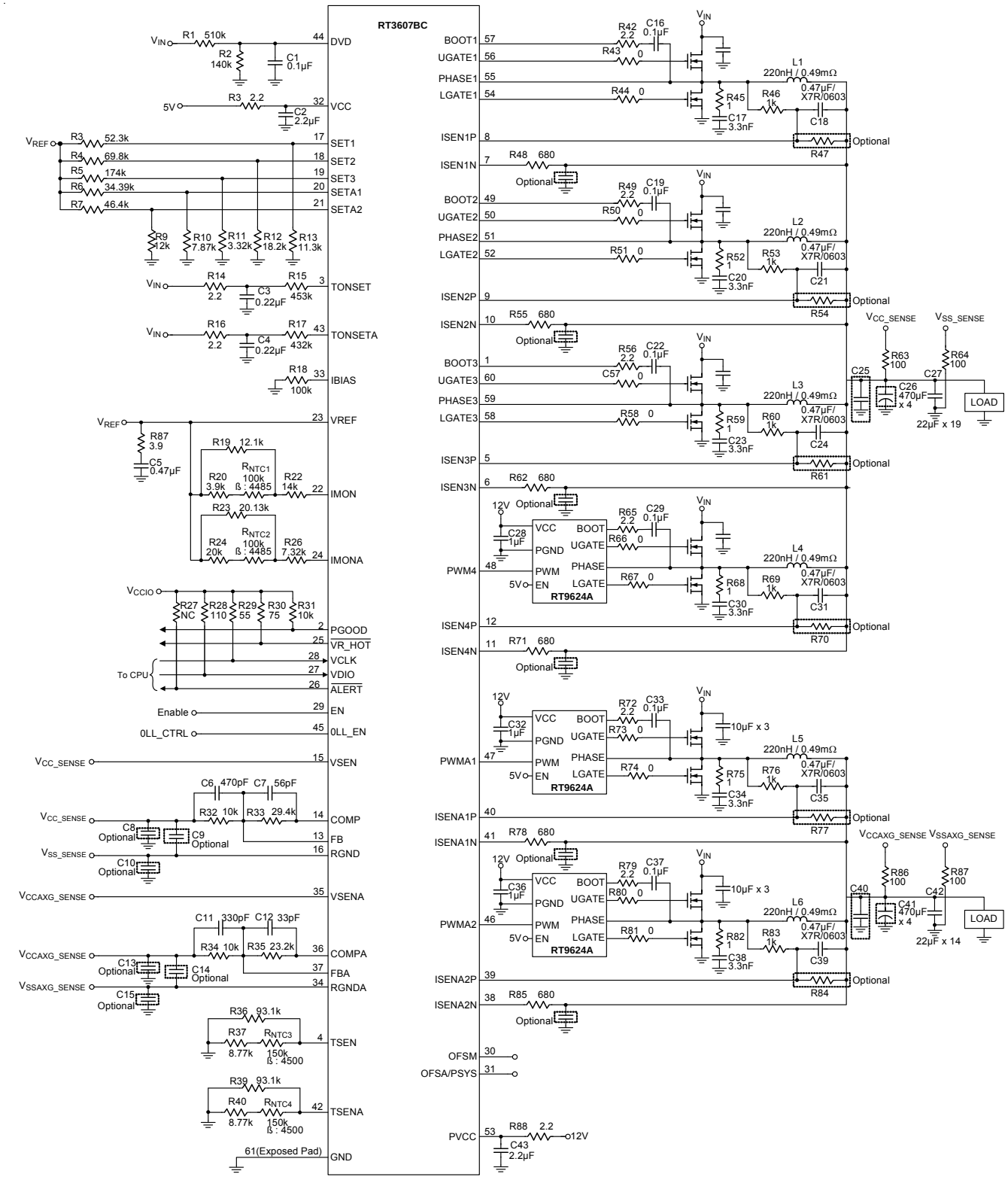
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5.(1) DVD Input High Voltage: DVD pin is an input pin of VR. VR always identify high level while the voltage given at DVD pin >= 2V. The high-low transition is within 1.3V ~2V.

(2) DVD Input low Voltage: DVD pin is an input pin of VR. VR always identify low level while the voltage given at DVD pin <= 1.3V. The high-low transition is within 1.3V ~2V.

Typical Application Circuit

Discrete MOS



Applications Information

The RT3607BC includes two voltage rails : a 4/3/2 multiphase synchronous buck controller, the CORE VR, and a 2 multiphase synchronous buck controller, the AXG VR, designed to meet Intel IMVP8 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all the kinds of settings to save total pin number for easy use and increasing PCB space utilization. The RT3607BC is used in desktop computers and servers.

General Loop Function

G-NAVP™ Control Mode

The RT3607BC adopts the G-NAVP™ controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches comp signal, the RT3607BC generates an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms in continuous conduction mode (CCM).

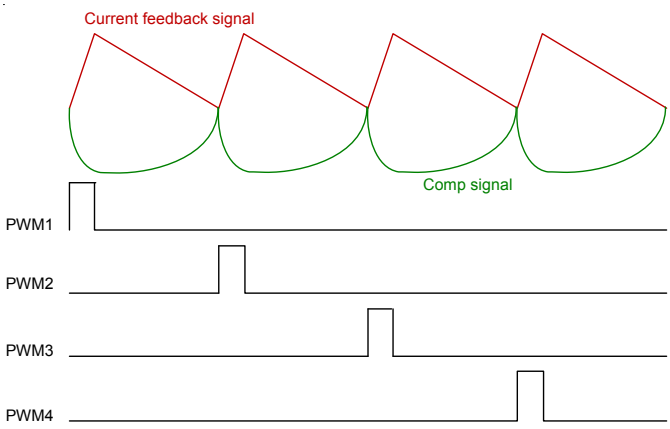


Figure 1 (a). G-NAVP™ CCM behavior waveforms in CCM in Steady State

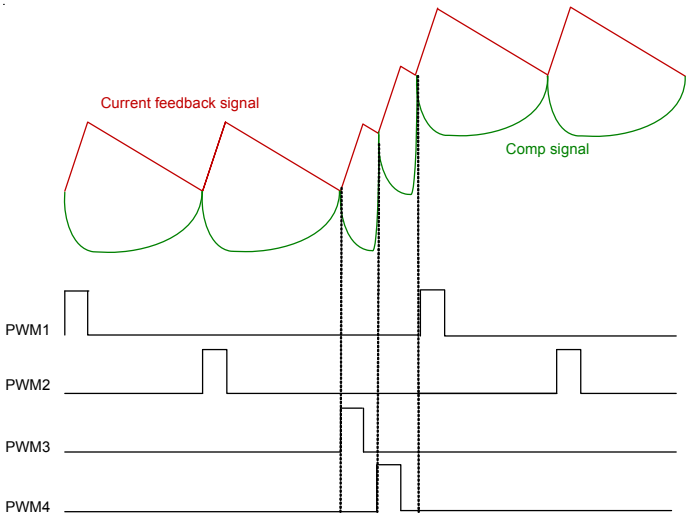


Figure 1 (b). G-NAVP™ CCM behavior waveforms in CCM in Load Transient

Diode Emulation Mode (DEM)

As well-known, the dominant power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduction mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. The RT3607BC can operate in diode emulation mode (DEM) to improve light load efficiency. In DEM operation, the behavior of the low side MOSFET(s) needs to work like a diode, that is, the low side MOSFET(s) is turned on when the phase voltage is a negative value, i.e. the inductor current follows from Source to Drain of low-side MOSFET(s). And the low-side MOSFET(s) is turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching loss are reduced to improve efficiency at light load condition.

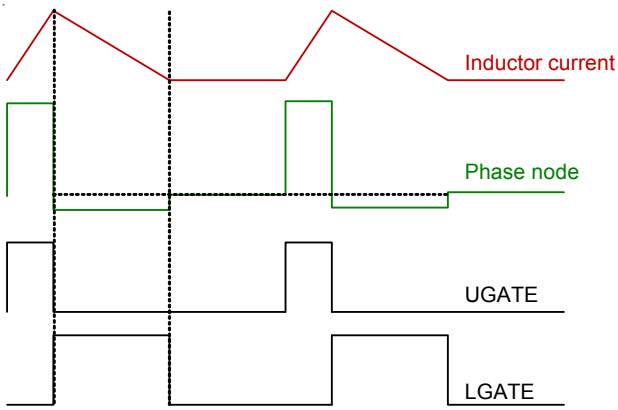


Figure 2. Diode Emulation Mode (DEM) in Steady State

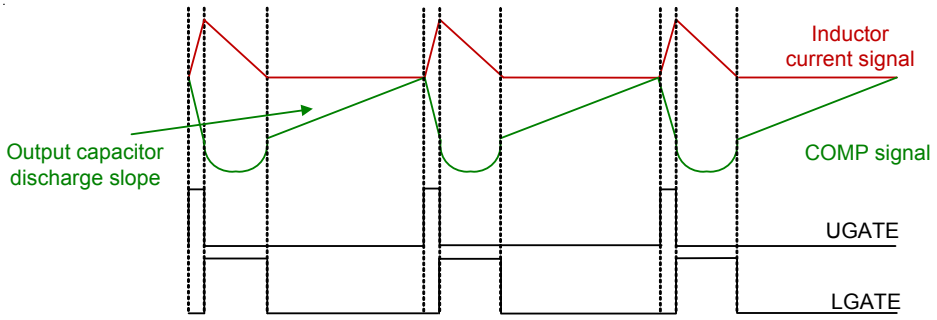


Figure 3. (a)

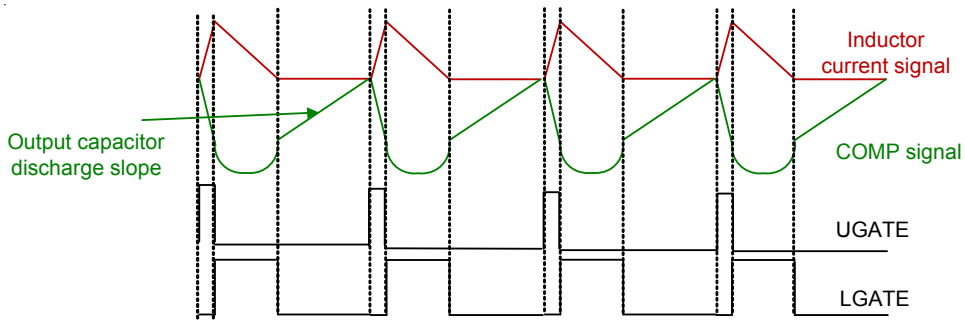


Figure 3. (b)

Figure 3. G-NAVP™ operation in DEM. (a) : The load is lighter, output capacitor discharge slope is smaller and the switching frequency is lower. (b) : The load is increasing, output capacitor discharge slope is increased and switching frequency is increased, too.

Phase Interleaving Function

The RT3607BC is a multiphase controller, which has a phase interleaving function, 90 degree phase shift for 4-phase operation, 120 degree phase shift for 3-phase operation and 180 degree phase shift for 2-phase operation which can help reduce output voltage ripple and EMI problem.

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, SET [1:3] and SETA[1:2] pins adopt the multi-function pin setting mechanism in the RT3607BC. SET [1:3] and SETA[1:2] are used to set CORE VR and AXG VR, respectively. Figure 4 illustrates this operating mechanism. The voltage at VREF pin is pulled up to 3.2V during pin setting mode after power ready (POR). External voltage divider is used to set the Function1. Then an internal current source 80μA sources the R network to set the Function2. The setting voltage of Function1 and Function2 can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

$V_{Function1}$/$V_{Function2}$ is coded by ADC and stored in the registers to set specified functions. For example, Function1 of SET1 can set ICCMAX; Function2 of SET1 can set DVID Compensation magnitude. All function setting will be done within 1900μs after power ready (POR), and the voltage at VREF pin is fixed to be 0.6V after all function settings are over.

If $V_{Function1}$ and $V_{Function2}$ are determined by application or performance requirement, R1 and R2 can be calculated as follows :

$$R1 = \frac{3.2V \times V_{Function2}}{80\mu A \times V_{Function1}}$$

$$R2 = \frac{R1 \times V_{Function1}}{3.2V - V_{Function1}}$$

In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the SETx and SETAx resistor network for the RT3607BC.

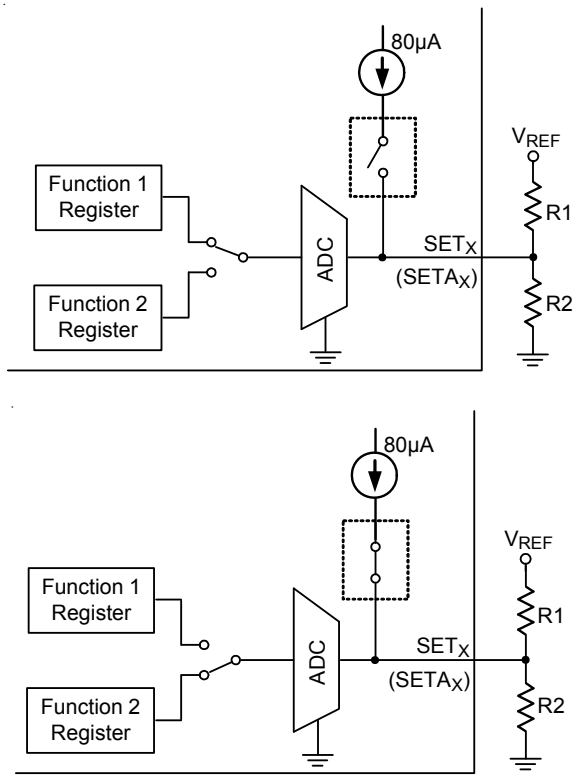


Figure 4. Multi-Function Pin Setting Mechanism

Connecting a R3 resistor from SETx pin or SETAx pin to the middle node of voltage divider can help to fine tune the set voltage of Function2, which does not affect the set voltage of Function1. The Figure 5 shows the setting method and the set voltage of Function 1 and Function2 can be represented as :

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1+R2} \right)$$

By the way, SET1 and SET2 are used to set CORE rail setting and SETA1 and SETA2 are used to set AXG rail setting. The setting of SET3 is suitable for both CORE rail and AXG rail. Table 2 summarizes the overall pin setting function. Table 3 and Table 4 show the SET3 pin setting function table.

Table 2. Pin Setting Function Table

	Function1	Function2
Set1(Main Rail)	ICCMAX	Zero Load-line DVID Threshold
Set2(Main Rail)	Over Current Protection (OCP) threshold RAMP setting	Quick Response(QR) Threshold RAMP Offset setting
Set3(Main/AXG Rail)	Enable PSYS DVID Width for Main Rail Quick Response(QR) Width for Main Rail	DVID Width for AXG Rail Quick Response(QR) Width for AXG Rail
SetA1(AXG Rail)	ICCMAXA	DVID Threshold
SetA2(AXG Rail)	Over Current Protection (OCP) threshold RAMP setting	Quick Response(QR) threshold RAMP Offset setting

Table 3. SET3 Pin Setting for Enable PSYS, DVID Width_CORE Rail and QR Width_CORE Rail

$V_{divider\_SET3}$ (mV)	ENABLE PSYS	DVID_WIDTH_M	QR_WIDTH_M (%TON)
25	DISABLE	12us	133.2
75			88
125			44
175			DISABLE
225		24us	133.2
275			88
325			44
375			DISABLE
425		36us	133.2
475			88
525			44
575			DISABLE
625		48us	133.2
675			88
725			44
775			DISABLE
825	ENABLE	12us	133.2
875			88
925			44
975			DISABLE
1025		24us	133.2
1075			88
1125			44
1175			DISABLE
1225		36us	133.2
1275			88
1325			44
1375			DISABLE
1425		48us	133.2
1475			88
1525			44
1575			DISABLE

Table 4. SET3 Pin Setting for DVID Width_AXG Rail and QR Width_AXG Rail

V_{IxR_SET3} (mV)	DVID_WIDTH_A	QR_WIDTH_A (%TON)
50	12us	133.2
150		88
250		44
350		DISABLE
450	24us	133.2
550		88
650		44
750		DISABLE
850	36us	133.2
950		88
1050		44
1150		DISABLE
1250	48us	133.2
1350		88
1450		44
1550		DISABLE

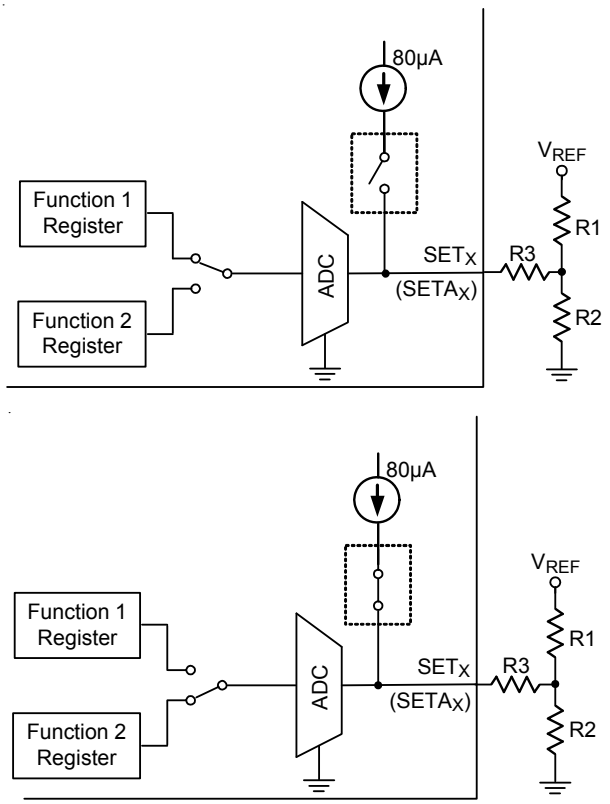


Figure 5. Multi-Function Pin Setting Mechanism with a R3 Resistor to Fine Tune the Set Voltage of Function2

VR Rail Addressing Setting

The VR address of the RT3607BC can be flipped by setting the voltage on SET3 with an external voltage divider as shown in Figure 6. The voltage at VREF pin is pulled up to 3.2V after power ready (POR) and the voltage at VREF pin is fixed to be 0.6V within 1900μs after power ready (POR).

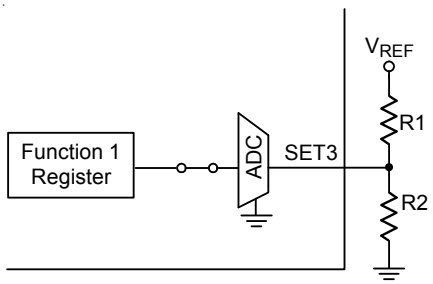


Figure 6. VR Rail Addressing and Zero Load-Line Setting for SET3

Zero Load-line

The RT3607BC can support zero load-line function. It is enabled when 0LL_EN pin >4.3V and SET1 pin-setting for Enable Zero Load-line determines whether both rail has zero load-line function or only one rail has this function.

For example, if ISET1 set to 1.25V and 0LL_EN pin >4.3V, both CORE rail and AXG rail have zero load-line function, if ISET1 set to 0.05V and 0LL_EN pin >4.3V, only CORE rail has zero load-line function. If 0LL_EN pin <1, both rails don't have load-line function even if SET1 pin set to enable zero load-line function. In addition, the zero load-line function can be dynamically enabled by varying 0LL_EN pin.

When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3607BC adopts a new feature, i.e. AC-droop, to effectively suppress load transient ring back and further well-control overshoot for zero load-line application. Figure 7 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back ΔV2 due to C area charge. Figure 8 shows the condition with AC-droop control. While loading occurs, controller will temporarily change VID target to short-term voltage target. Short term voltage target is related to transient loading current ΔICC and can be represented as the following :

$$Short\_Time\_Voltage\_Target = VID - \Delta I_{CC} \times R_{LL}$$

The setting method of RLL is the same as load line system. The short term voltage target will revert to VID target slowly after a period of time. The short term voltage target can help inductor current not to exceed loading current too much and then the ring back can be suppressed. The overshoot amplitude is reduced to only ΔV3.

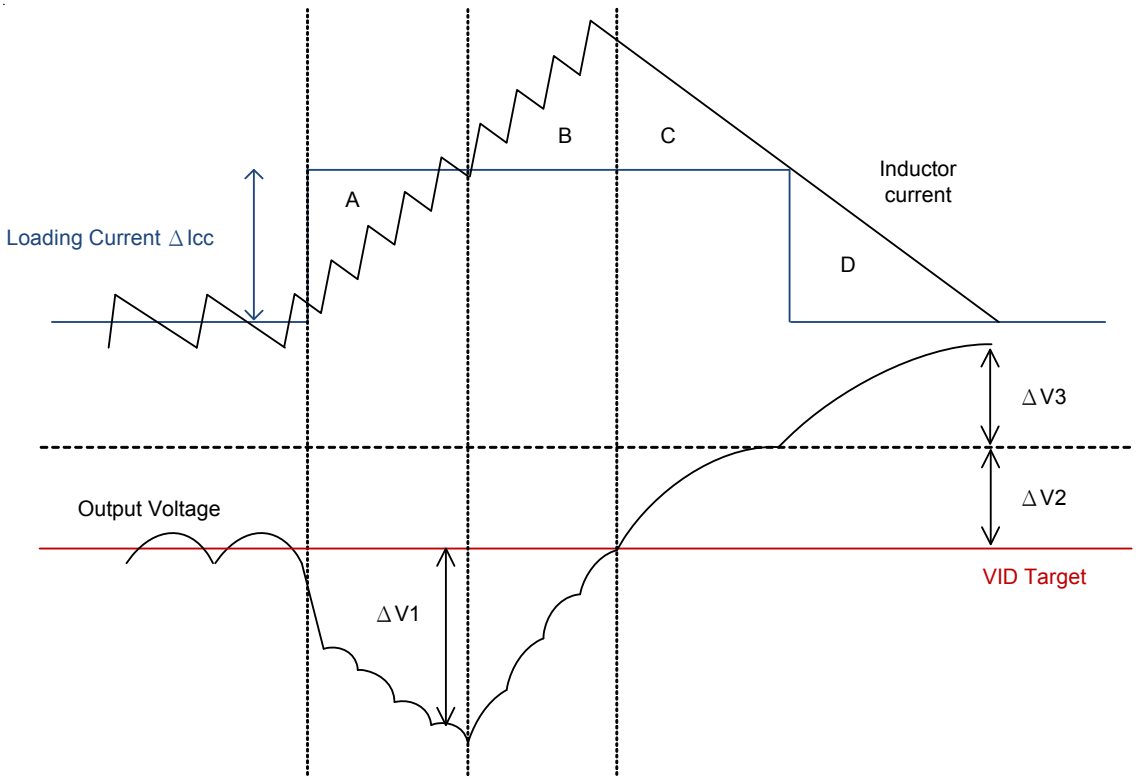


Figure 7. Zero Loadline without AC-droop Control

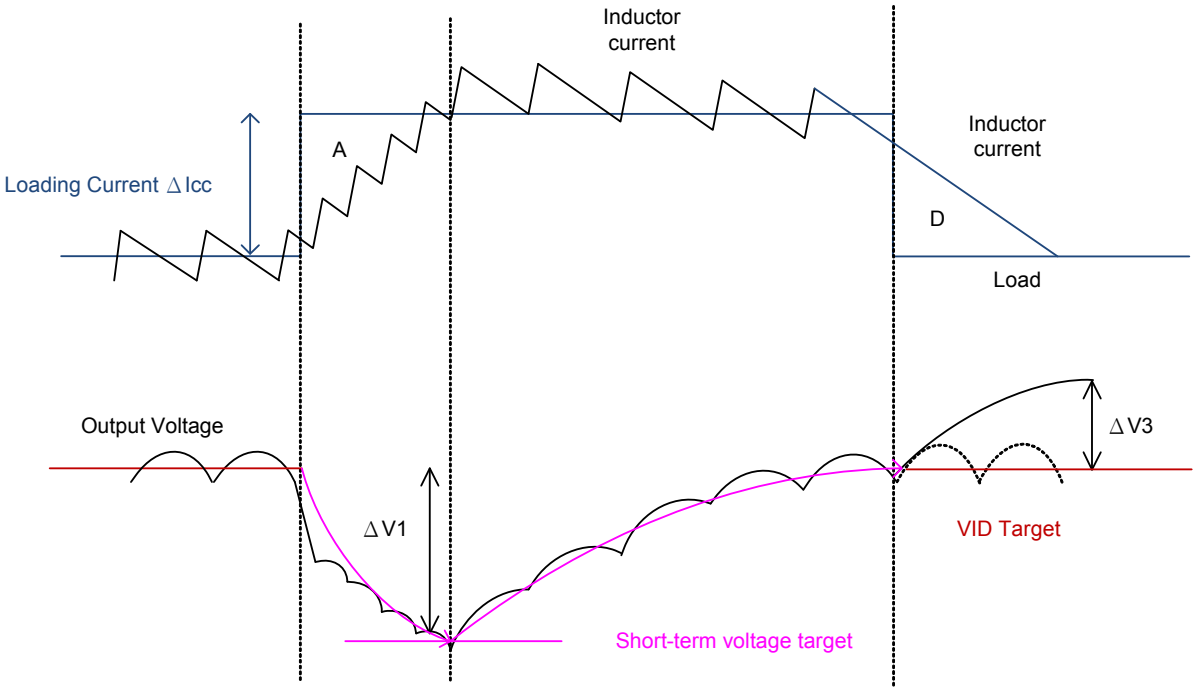


Figure 8. Zero Loadline with AC-droop Control

High Switching Frequency Ramp

The switching frequency of the RT3607BC can be adjustable from 300kHz to 1.1MHz, however, with higher switching frequency, the ramp needs to be increased simultaneously to improve the system stability and smooth the mode transient performance. As switching is higher than 550kHz, the high switching frequency ramp is suggested to be enabled. The high switching frequency ramp can be enabled or disabled by the internal current source 80μA and the resistors connected to SET3 pin.

Precise Reference Current Generation, IBIAS

Analog circuits need very precise reference current to drive/set these analog devices. The RT3607BC provides a 2V voltage source at the IBIAS pin, and a precise 100kΩ resistor is required to be connected between the IBIAS pin and analog ground to generate a very precise reference current. Through this connection, the RT3607BC generates a 20μA current from the IBIAS pin to analog ground, and this 20μA current is mirrored inside the RT3607BC for internal use. The IBIAS pin can only be connected with a 100kΩ resistor to GND for internal analog circuit use. The resistance error of this resistor is recommended to be 1% or smaller. Figure 9 shows the IBIAS setting circuit.

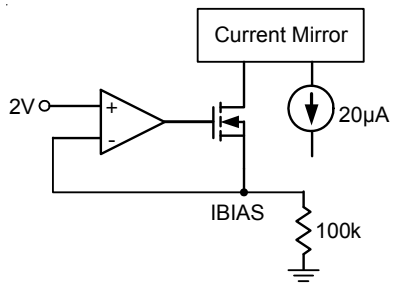


Figure 9. IBIAS Setting Circuit

TSEN, TSENA and VR_HOT

The VR_HOT signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage at TSEN(A) pin is less than 1.092V, the VR_HOT signal is pulled-low to notify CPU that the thermal protection needs to work. According to Intel VR definition, VR_HOT signal needs acting if VR power chain temperature exceeds 100°C. Place an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 10, to design the voltage divider elements (R1, R2 and NTC) so that VTSEN(A) = 1.092V at 100°C. The resistance error of TSEN network is recommended to be 1% or smaller.

$$V_{TSEN(A)} = 80\mu A \times (R1//(R2 + R_{NTC\ (100^{\circ}C)}))$$

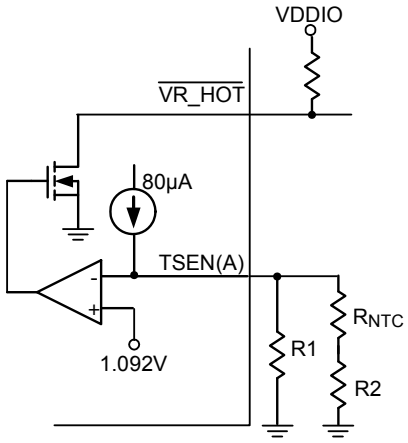


Figure 10. VR_HOT Circuit

Power Ready (POR) Detection

During start-up, the RT3607BC detects the voltage at the voltage input pins: V_{CC}, EN and DVD. When V_{CC} > 4.34V and V_{DVD} > 2V, the RT3607BC recognizes the power state of system to be ready (POR = high) and waits for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT3607BC enters start-up sequence. If the voltage at any voltage pin drops below low threshold (POR = low), the RT3607BC enters power down sequence and all the functions are disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin and power stage VIN (12V, through a voltage divider) to the DVD pin is recommended. 2ms (max) after the chip has been enabled, the SVID circuitry is ready. All the protection latches (OVP, OCP) are cleared only by VCC. The condition of VEN = low does not clear these latches. Figure 11 and Figure 12 show the POR detection and the timing chart for POR process, respectively. For California Energy Commission (CEC) Regulatory Design Recommendations, VRs that can tolerate removal of +V12 input while VID = 0. To achieve this requirement, the DVD pin should connect to 5V and make sure that VIN is higher

than 10.8V when EN signal is coming.

Under Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC drops below POR threshold 3.95V (min) or DVD voltage drops below POR threshold 1.3V, the VR triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers.

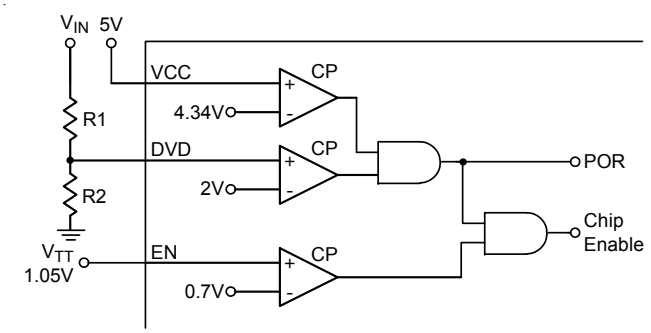


Figure 11. POR Detection

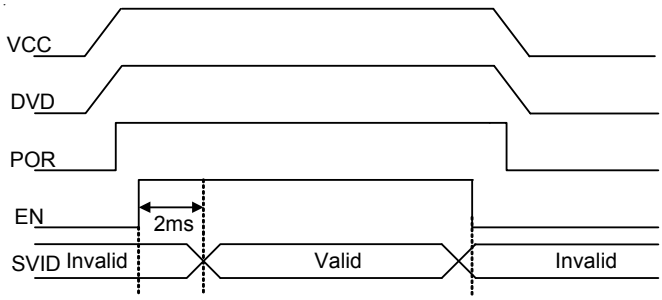


Figure 12. Timing Chart for POR Process

CORE VR

Phase Disable (Before POR)

The number of active phases is determined by the internal circuitry that monitors the ISENxN voltages during startup. Normally, the VR operates as a 4-phase PWM controller. Pulling ISEN4N to VCC programs a 3-phase operation, and pulling ISEN4N and ISEN3N to VCC programs a 2-phase operation. Before POR, VR detects whether the voltages of ISEN3N and ISEN4N are higher than "VCC – 1V" respectively to decide how many phases should be active. Phase selection is only active during POR. When POR = high, the number of active phases is determined and latched. The unused ISENxP pins are recommended to be connected to VCC and unused PWM pins can be left floating.

NO Load Offset (Platform)

The CORE VR features no load offset function which provides the possibility of wide range positive offset of output voltage. Users can disable offset function by simply connecting OFSM pin to GND. Figure 13 shows a voltage divider used to set no load offset voltage. No load offset voltage setting is :

$$V_{OFS\_CORE} = 0.4 \times (V_{OFSM} - 1.7)$$

The range of V_{OFS_CORE} is between –500mV and 590mV and the resolution is 10mV.

For example, for a 100mV no load offset requirement, V_{OFSM} needs to be set as 1.95V.

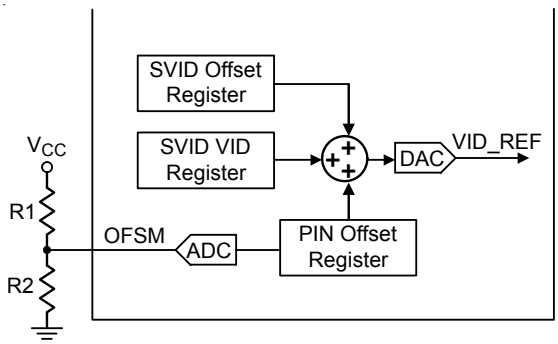


Figure 13. No Load Offset Circuit

Switching Frequency Setting

The RT3607BC is one kind of constant on-time controller. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time. The on-time varies with the input voltage and VID code to obtain a constant current ripple, so that the output voltage ripple can be controlled nearly like a constant as different input and output voltages change.

For CORE VR, connect a resistor R_{TON} between input terminal and TONSET pin to set the on-time width.

$$T_{ON} = \frac{R_{TON} \times 4.73p \times 1.2}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2)$$

$$T_{ON} = \frac{R_{TON} \times 4.73p \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 1.2)$$

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{SW(MAX)} = \frac{VID1 + \frac{IccTDC}{N} \cdot \left(DCR + \frac{R_{ON\_LS,max}}{n_{LS}} - N \cdot R_{LL} \right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} - \frac{R_{ON\_HS,max}}{n_{HS}} \right) \right] \cdot (T_{ON} - T_D + T_{ON,VAR}) + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} \right) \cdot T_D}$$

Where $F_{sw(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number. The $R_{ON\_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$, and n_{HS} is the number of high-side MOSFETs; $R_{ON\_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for the RT3607BC.

When load increases, on-time keeps constant. The off-time width is reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Per Phase Current Sense

In the RT3607BC, the current signal is used for load-line setting and over-current protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in Figure 12. When inductance and DCR time constant is equal to R_XC_X filter network time constant, a voltage I_{Lx} x DCR drops on C_x to generate inductor current signal. According to the Figure 14, the ISENxN is as follows :

$$ISENxN = \frac{I_{LX} \times DCR}{R_{CSx}}$$

Where Lx/DCR = R_XC_X is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, so an NTC resistor should be added in the resistor network at the IMON pin to achieve DCR thermal compensation.

In the RT3607BC design, the resistance of R_{CSx} is restricted to be 680Ω; moreover, the error of R_{CSx} is recommended to be 1% or smaller. R_X is highly recommended as two 0603 size resistors in series to alleviate the I_{OUT} reporting inaccuracy issue at no load due to the VCR (voltage coefficient of resistance) effect.

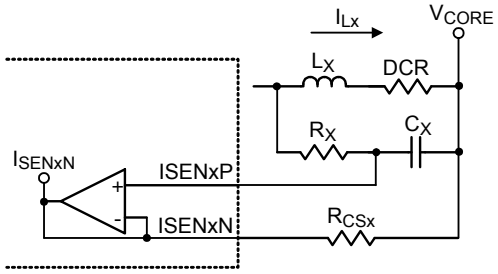


Figure 14. Lossless Current Sense Method

Total Current Sense

Total current sense method is a patented topology, unlike conventional current sense method needs an NTC resistor in per phase current loop for thermal compensation. The RT3607BC adopts the total current sense method requiring only one NTC resistor for thermal compensation, and NTC resistor cost can be saved by using this method. Figure 15 shows the total current sense method which connects the resistor network between IMON pin and VREF pin to set a part of current loop gain for load line (droop) setting and set accurate over current protection.

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3} + I_{L4})$$

R_{EQ} includes an NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

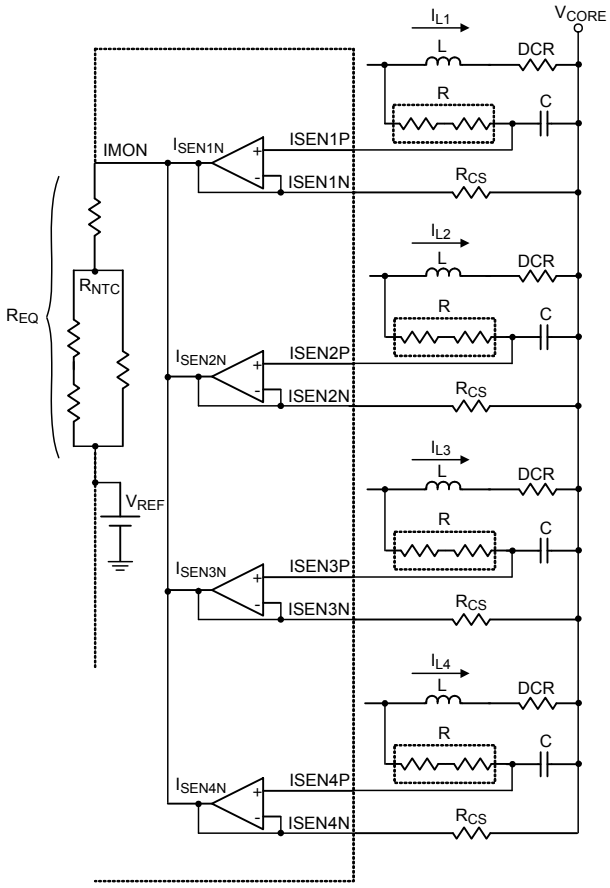


Figure 15. Total Current Sense Method

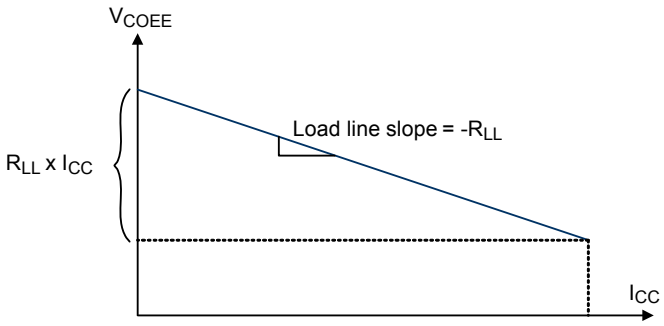


Figure 16. Load-Line (Droop)

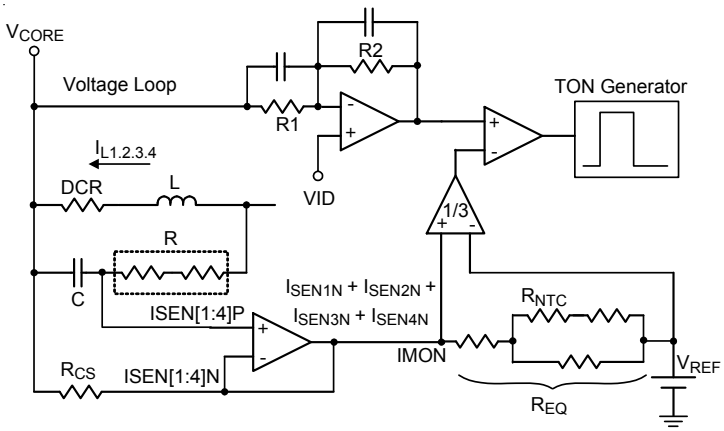


Figure 17. Voltage Loop and Current Loop

Load-Line Setting (Droop)

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop. The load-line is a slope between load current I_{CC} and output voltage V_{CORE} as shown in Figure 16. Figure 17 shows the voltage control and current loop. By using both the loops, the load-line (droop) can be set easily. The load-line set equation is :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} (m\Omega)$$

Compensator Design

The compensator of the RT3607BC doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP™ topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 18, the transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range

$$G_{CON}(S) \approx \frac{A_I}{R_{LL}} \frac{1 + \frac{s}{\omega \times fsw}}{1 + \frac{s}{\omega ESR}}$$

Where A_I is current loop gain, R_{LL} is load line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1 / (C_{OUT} x ESR). Then the C1 and C2 should be designed as

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \qquad C2 = \frac{C_{OUT} \times ESR}{R2}$$

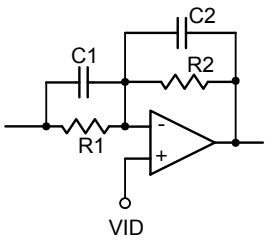


Figure 18. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 19. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

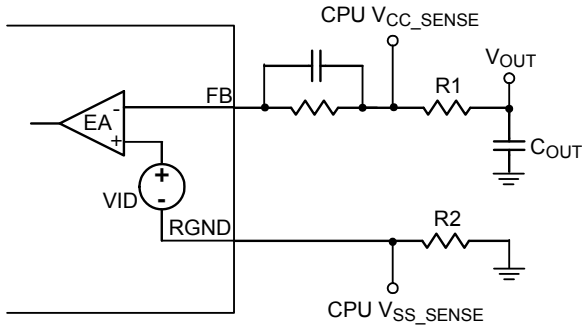


Figure 19. Remote Sensing Circuit

Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by the SET1 pin. ICCMAX register is set by an external voltage divider with the multi-function mechanism. The table 5 shows the ICCMAX setting on the SET1 pin. For example, ICCMAX = 80A, the V_{SET1} needs to set as 0.503V typical. Additionally, V_{IMON} – V_{REF} needs to be set as 1.6V at ICCMAX when the maximum phase > 1. As in 1-phase application, the V_{IMON} – V_{REF} needs to be set as 0.4V at ICCMAX. The ICCMAX alert signal is pulled to low level if V_{IMON} – V_{REF} = 1.6V (for maximum phase > 1) or V_{IMON} – V_{REF} = 0.4V (for 1-phase application).

Table 5. SET1 Pin Setting in ICCMAX

$V_{divider\_SET1}$ (mV)	ICCMAX	Unit
3.125	0	A
15.625	2	A
28.125	4	A
40.625	6	A
53.125	8	A
65.625	10	A
78.125	12	A
90.625	14	A
103.125	16	A
115.625	18	A
128.125	20	A
140.625	22	A
153.125	24	A
165.625	26	A
178.125	28	A
190.625	30	A
203.125	32	A
215.625	34	A
228.125	36	A
240.625	38	A
253.125	40	A
265.625	42	A
278.125	44	A
290.625	46	A
303.125	48	A
315.625	50	A
328.125	52	A
340.625	54	A
353.125	56	A
365.625	58	A
378.125	60	A
390.625	62	A
403.125	64	A
415.625	66	A
428.125	68	A
440.625	70	A
453.125	72	A
465.625	74	A
478.125	76	A
490.625	78	A

$V_{divider\_SET1}$ (mV)	ICCMAX	Unit
503.125	80	A
515.625	82	A
528.125	84	A
540.625	86	A
553.125	88	A
565.625	90	A
578.125	92	A
590.625	94	A
603.125	96	A
615.625	98	A
628.125	100	A
640.625	102	A
653.125	104	A
665.625	106	A
678.125	108	A
690.625	110	A
703.125	112	A
715.625	114	A
728.125	116	A
740.625	118	A
753.125	120	A
765.625	122	A
778.125	124	A
790.625	126	A
803.125	128	A
815.625	130	A
828.125	132	A
840.625	134	A
853.125	136	A
865.625	138	A
878.125	140	A
890.625	142	A
903.125	144	A
915.625	146	A
928.125	148	A
940.625	150	A
953.125	152	A
965.625	154	A
978.125	156	A
990.625	158	A

$V_{divider\_SET1}$ (mV)	ICCMAX	Unit
1003.125	160	A
1015.625	162	A
1028.125	164	A
1040.625	166	A
1053.125	168	A
1065.625	170	A
1078.125	172	A
1090.625	174	A
1103.125	176	A
1115.625	178	A
1128.125	180	A
1140.625	182	A
1153.125	184	A
1165.625	186	A
1178.125	188	A
1190.625	190	A
1203.125	192	A
1215.625	194	A
1228.125	196	A
1240.625	198	A
1253.125	200	A
1265.625	202	A
1278.125	204	A
1290.625	206	A
1303.125	208	A
1315.625	210	A
1328.125	212	A
1340.625	214	A
1353.125	216	A
1365.625	218	A
1378.125	220	A
1390.625	222	A
1403.125	224	A
1415.625	226	A
1428.125	228	A
1440.625	230	A
1453.125	232	A
1465.625	234	A
1478.125	236	A
1490.625	238	A

$V_{divider\_SET1}$ (mV)	ICCMAX	Unit
1503.125	240	A
1515.625	242	A
1528.125	244	A
1540.625	246	A
1553.125	248	A
1565.625	250	A
1578.125	252	A
1590.625	254	A

Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop. However, the DVID performance will be deteriorated by this induced charge current, this phenomenon is called droop effect. The droop effect is shown in Figure 20, when VID up transition occurs, and this output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

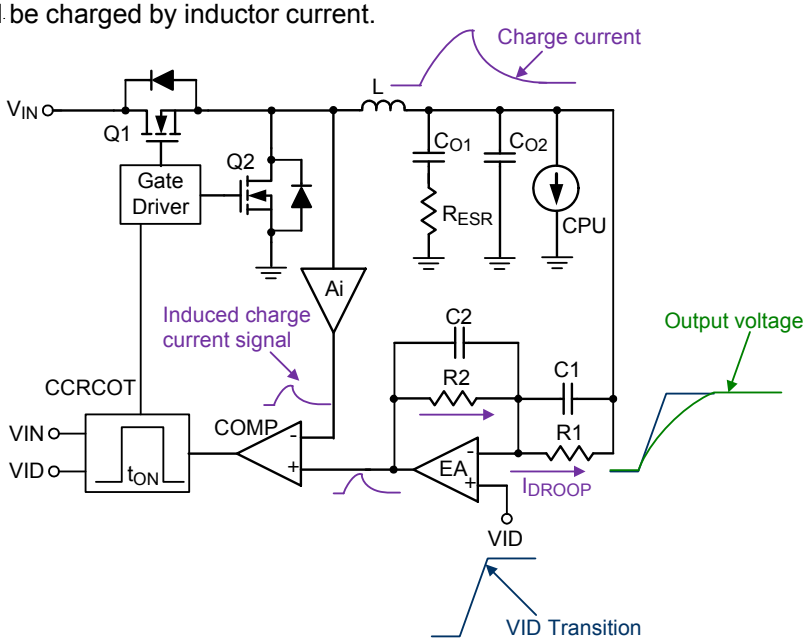


Figure 20. Droop Effect in VID transition

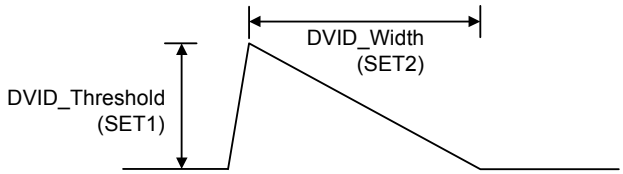


Figure 21. Definition of Virtual Charge Current Signal

The RT3607BC provide a DVID compensation function. A virtual charge current signal can be established by the SET1/SET3 pins to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 21. Figure 22 shows the operation of canceling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal to be generated on the FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

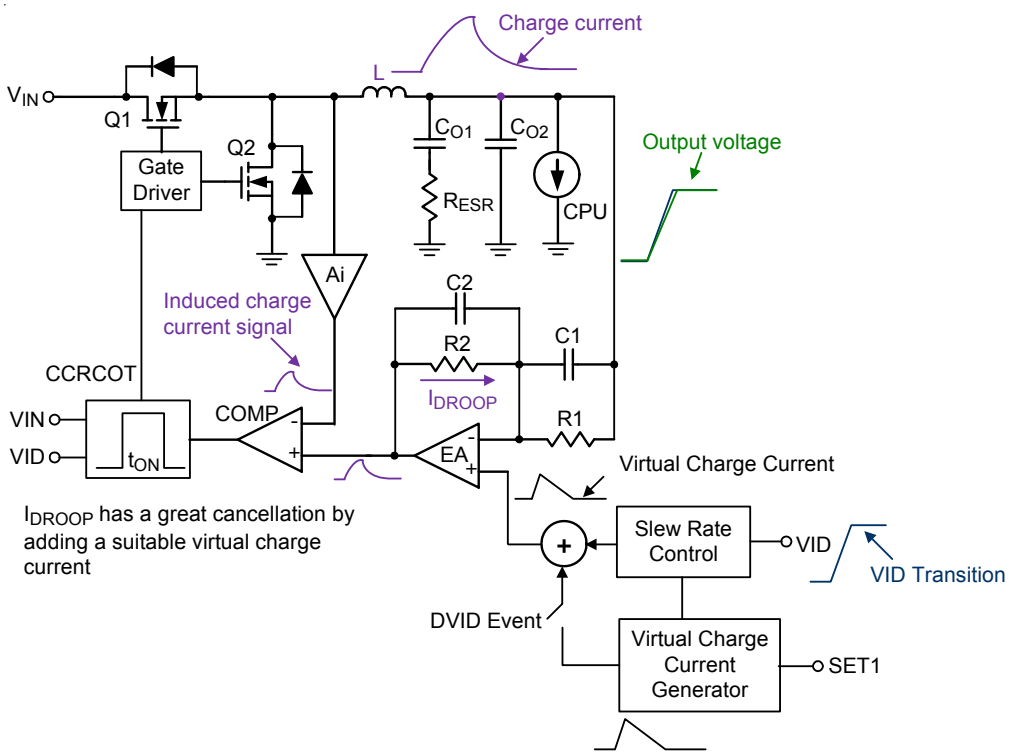


Figure 22. DVID Compensation

Table 6 shows the DVID_Threshold on the SET1 pin with internal 80μA current source and Table 3 describes DVID_Width settings in SET3 pin with external voltage divider. For example, 39.67mV DVID_Threshold (Enable Zero LL) and 36μs DVID_Width are designed (Enable PSYS, QR_width = 88%). According to Table 6 and Table 3, the DVID_Threshold set voltage should be 1.05V and the DVID_Width set voltage should be 1.475V. Please note that a high accuracy resistor is needed for this setting, < 1% error tolerance is recommended.

Table 6. SET1 Pin Setting for Zero Load Line and DVID_Threshold

V_{IxR_SET1} (mV)	Zero Load Line	DVID_Threshold_M
50	Main : Enable AXG : Disable	18.33mV
150		29mV
250		39.67mV
350		50.33mV
450		61mV
550		71.67mV
650		82.33mV
750		93mV
850	Main : Enable AXG : Enable	18.33mV
950		29mV
1050		39.67mV
1150		50.33mV
1250		61mV
1350		71.67mV
1450		82.33mV
1550		93mV

Table 7. SET2 Pin Setting for OCP and RAMP Setting

$V_{divider\_SET2}$ (mV)	OCP_M = %ICCMAX	Ramp Setting_M, if Ramp Offset_M = 0kHz	Ramp Setting_M, if Ramp Offset_M = 50kHz
25	110%	300kHz	350kHz
75		400kHz	450kHz
125		500kHz	550kHz
175		600kHz	650kHz
225	110%	300kHz	350kHz
275		400kHz	450kHz
325		500kHz	550kHz
375		600kHz	650kHz
425	120%	300kHz	350kHz
475		400kHz	450kHz
525		500kHz	550kHz
575		600kHz	650kHz
625	130%	300kHz	350kHz
675		400kHz	450kHz
725		500kHz	550kHz
775		600kHz	650kHz
825	140%	300kHz	350kHz
875		400kHz	450kHz
925		500kHz	550kHz
975		600kHz	650kHz
1025	150%	300kHz	350kHz
1075		400kHz	450kHz
1125		500kHz	550kHz
1175		600kHz	650kHz
1225	160%	300kHz	350kHz
1275		400kHz	450kHz
1325		500kHz	550kHz
1375		600kHz	650kHz
1425	160%	300kHz	350kHz
1475		400kHz	450kHz
1525		500kHz	550kHz
1575		600kHz	650kHz

RAMP Setting

RAMP plays an important role in the balance of loop stability and transient response. It also helps to smooth power state transition process. The ramp height should link with switching frequency. After switching frequency is decided, the ramp still can be slightly adjusted to fine tune performance. The RT3607BC provide RAMP setting function through SET2 pin. SET2 are used to select more specific switching frequency for CORE rail. Table 7 describes Ramp setting in SET2 pin. Figure 23 shows the ramp compensation.

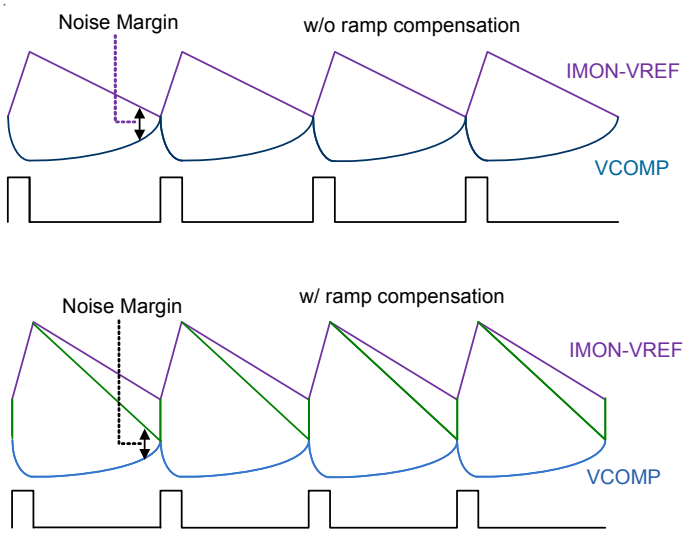


Figure 23.

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT3607BC has Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping. Figure 24 shows the QR behavior.

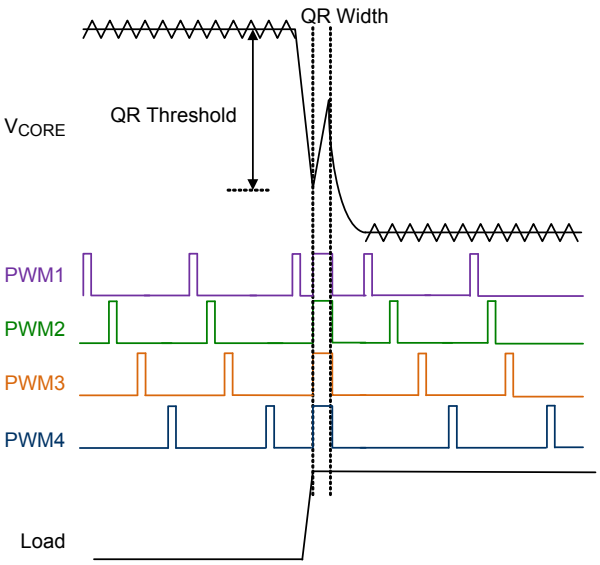


Figure 24. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at VSEN pin that is shown in Figure 25. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 22. A proper QR mechanism set can meet different applications. SET2 can set QR threshold by internal current source 80μA with multi-function pin setting mechanism. SET3 can set QR width with external voltage divider.

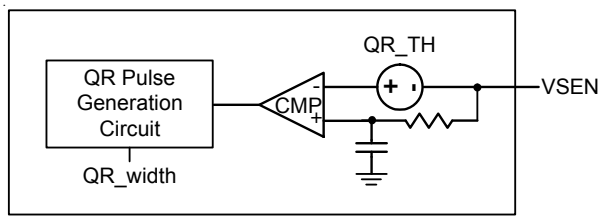


Figure 25. Simplified QR Trigger Schematic

For example, QR threshold 20mV/10mV at PS0/PS1 (Ramp Offset Setting = +0kHz) According to Table 8, the set voltage should be 0.45V. 0.88 x TON QR width (Enable PSYS, DVID width = 24μs) According to Table 3, the set voltage should be 1.075V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

Table 8. SET2 Pin Setting for QR Threshold and Ramp Offset Setting

V_{IxR_SET2} (mV)	QR Threshold_M		Ramp Offset Setting_M
	PS0	PS1	
50	15mV	10mV	+0 kHz
150			+50 kHz
250	15mV	15mV	+0 kHz
350			+50 KHz
450	20mV	10mV	+0 KHz
550			+50 KHz
650	20mV	15mV	+0 kHz
750			+50 KHz
850	25mV	10mV	+0 KHz
950			+50 KHz
1050	25mV	15mV	+0 KHz
1150			+50 KHz
1250	30mV	10mV	+0 KHz
1350			+50 KHz
1450	30mV	15mV	+0 KHz
1550			+50 KHz

Current Monitor, IMON

The RT3607BC includes a current monitor (IMON) function which can be used to detect over-current protection and the maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

The calculation for IMON-VREF voltage is shown as below :

$$V_{IMON} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQ} \times (I_{L1} + I_{L2} + I_{L3} + I_{L4})$$

Where I_{L1} + I_{L2} + I_{L3} + I_{L4} are output current and the definitions of DCR, R_{CS} and R_{EQ} can refer to Figure 15.

Over-Current Protection

The RT3607BC provides Over-Current Protection (OCP) which is set by the SET2 pin. The OCP threshold setting can refer to ICCMAX current in Table 5. For example, if ICCMAX is set as 120A, users can set voltage by using the external voltage divider on the SET1 pin as 0.754V typically. If 156A OCP (130% x ICCMAX) threshold and ramp setting = 400kHz will be set according to Table 7,

the set voltage should be 675mV. When output current is higher than the OCP threshold, OCP is latched with a 40μs delay to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs, and soft-start period. And the OCP function is re-active 46μs after DVID or soft-start alert is asserted.

Output Over-Voltage Protection

An OVP condition is detected when the VSEN pin is 350mV more than VID as VID > 1V. If VID < 1V, the OVP is detected when the VSEN pin is 350mV more than 1V. When OVP is detected, the high-side gate voltage UGATEx is pulled low and the low-side gate voltage LGATEx is pulled high. OVP is latched with a 0.5μs delay to prevent false trigger. Besides, the OVP function is masked during DVID and soft-start period. 46μs after DVID or soft-start alert is asserted, the OVP function is re-active.

Negative Voltage Protection

Since the OVP latch continuously turns on all low side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.07V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs reCOREs off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.07V due to OVP latch and NVP triggering. The NVP function is active only after OVP is triggered.

Current Loop Design in Details

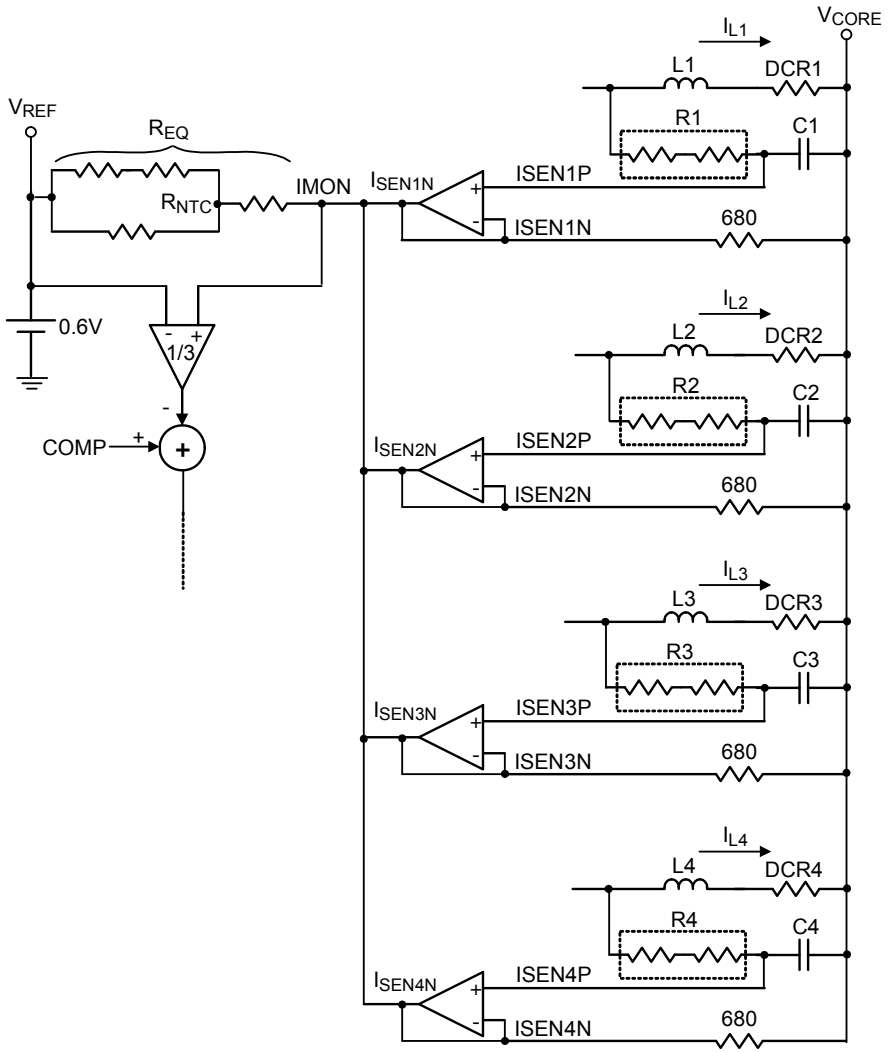


Figure 26. Current Loop Structure

Figure 26 shows the whole current loop structure. The current loop plays an important role in the RT3607BC that can decide ACLL performance, DCLL accuracy and ICCMAX accuracy. For ACLL performance, the correct compensator design is assumed, and if RC network time constant matches inductor time constant L_X / DCR_X, an ideal load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_X / DCR_X, V_{CORE} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_X / DCR_X, V_{CORE} waveform sags to create an undershooting to fail the specification. Figure 27 shows the output waveforms according to the R_XC_X constant.

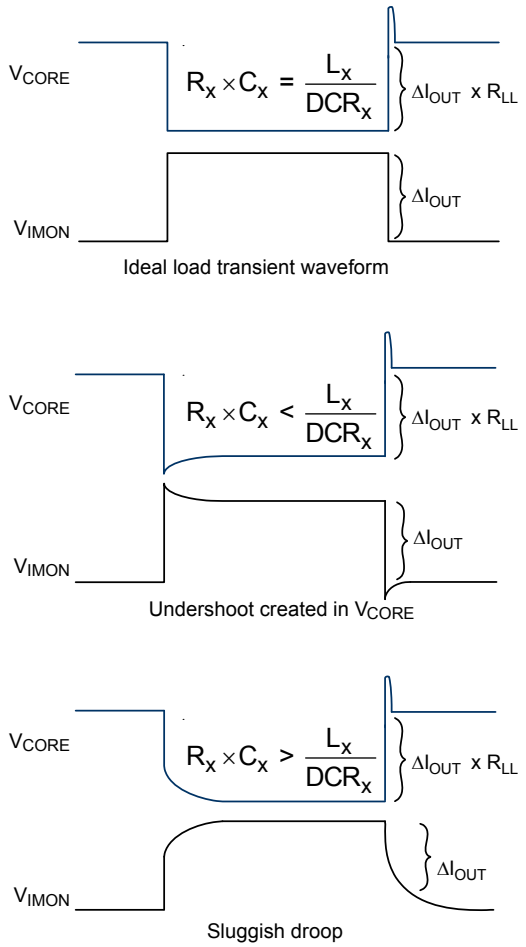


Figure 27. All Kinds of RxCx Constants

For DCLL performance and ICCMAX accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition, DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between IMON and REF pins is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as follows :

Step1 : Enter the three need are compensated system temperature, as low temperature (T_L), room temperature (T_R) and high temperature (T_H).

Step2 : Three equations can be listed as

$$\frac{DCR(T_L)}{680}\times\sum_{i=1}^{4} i_{Li}\times R_{EQ}(T_L)=1.6$$

$$\frac{DCR(T_R)}{680}\times\sum_{i=1}^{4} i_{Li}\times R_{EQ}(T_R)=1.6$$

$$\frac{DCR(T_H)}{680}\times\sum_{i=1}^{4} i_{Li}\times R_{EQ}(T_H)=1.6$$

Where :

(1) The relationship between DCR and temperature is as follows :

$$DCR(T)=DCR(25°C)\times[1+0.00393(T-25)]$$

(2) $R_{EQ}(T)$ is the equivalent resistor of the resistor network with an NTC thermistor

$$R_{EQ}(T)=R_{IMON1}+\{R_{IMON2}//[R_{IMON3}+R_{NTC}(T)]\}$$

And the relationship between NTC and temperature is as follows :

$$R_{NTC}(T)=R_{NTC}(25°C)\times e^{\beta(\frac{1}{T+273}-\frac{1}{298})}$$

β is in the NTC thermistor datasheet.

Step3 : Using the three equation, the three unknowns R_{IMON1}, R_{IMON2} and R_{IMON3} can be determined by the following equations.

$$R_{IMON1}=K_{TR}-\frac{R_{IMON2}\times(R_{NTCTR}+R_{IMON3})}{R_{IMON2}+R_{NTCTR}+R_{IMON3}}$$

$$R_{IMON2}=\sqrt{[K_{R3}^2+K_{R3}(R_{NTCTL}+R_{NTCTR})+R_{NTCTL}R_{NTCTR}]\alpha_{TL}}$$

$$R_{IMON3}=-R_{IMON2}+K_{R3}$$

Where :

$$\alpha_{TH}=\frac{K_{TH}-K_{TR}}{R_{NTCTH}-R_{NTCTR}}$$

$$\alpha_{TL}=\frac{K_{TL}-K_{TR}}{R_{NTCTL}-R_{NTCTR}}$$

$$K_{R3}=\frac{(\alpha_{TH}/\alpha_{TL})R_{NTCTH}-R_{NTCTL}}{1-(\alpha_{TH}/\alpha_{TL})}$$

$$K_{TL}=\frac{1.6}{G_{CS(TL)}\times I_{CC-MAX}}$$

$$K_{TR}=\frac{1.6}{G_{CS(TR)}\times I_{CC-MAX}}$$

$$K_{TH}=\frac{1.6}{G_{CS(TH)}\times I_{CC-MAX}}$$

Design Step :

The RT3607BC excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. There are three main design procedures for the RT3607BC design. The first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain the RT3607BC design procedure :

	V_{CORE} Specification
Input Voltage	12V
No. of Phases	3
ICCMAX	90A
ICC-DY	69A
ICC-TDC	68A
Load Line	2.1mΩ
Fast Slew Rate	10mV/μs
Max Switching Frequency	400kHz

In IMVP8 VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are :

Output Inductor : 220nH/0.49mΩ

Output Bulk Capacitor : 560μF/2.5V/5mΩ (max) 4 to 5pcs

Output Ceramic Capacitor : 22μF/0805 (19pcs max in cavity)

(1) Initial Settings :

- IBIAS needs to connect a 100kΩ resistor to ground.
- A voltage divider for setting DVD can choose R_{DVD_U} = 510kΩ and R_{DVD_L} = 125kΩ to set V_{DVD} > 2V, the RT3607BC enabled.

(2) Loop Design :

- On time setting : Using the specification, T_{ON} is

$$T_{ON} = \frac{R_{TON} \times 4.73p \times 1.2}{V_{IN} - V_{DAC}} (V_{DAC} < 1.2) = 246n$$

The on time setting resistor R_{TON} = 483kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an desirable load transient waveform, RxCx time constant needs to match Lx / DCRx per phase. Cx = 0.47μF is set, then

$$R_X = \frac{L_X}{0.47\mu F \times DCR_X} = 960\Omega$$

- IMON resistor network design : T_L = 25°C, T_R = 50°C, T_H = 100°C, NTC thermistor = 100kΩ@25°C, β = 4485 and ICCMAX = 90A. According to the sub-section "Current Loop Design in Details", R_{IMON1} = 10.66kΩ, R_{IMON2} = 16.16kΩ and R_{IMON3} = 1 2.63kΩ can be determined. The R_{EQ} (25°C) = 24.91kΩ.
- Load-line design : 2.1mΩ droop is requirement, because R_{EQ} (25°C) has been determined, the voltage loop Av gain also can be determined by following equation

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQ}}{\frac{R2}{R1}} (m\Omega)$$

Where DCR (25°C) = 0.49mΩ, R_{CS} = 680Ω and R_{EQ} (25°C) = 24.91kΩ. Hence the A_V = R2 / R1 = 2.85 can be obtained. R1 = 10kΩ is usually used, so R2 = 28.5kΩ.

- Typical compensator design can use the following equations to design the C1 and C2 values

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \approx 470pF$$

$$C2 = \frac{C_{OUT} \times ESR}{R2} \approx 98pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero of the compensator can be designed close to 1/10 of switching frequency.

- SET1 resistor network design : First the ICCMAX is design as 90A. Next, OCP threshold is designed as 1.3 x ICCMAX. Last, DVID compensation parameters need to be decided. The DVID_TH can be calculated as following equation

$$V_{DVID\_TH} = LL \times C_{OUT} \times \frac{dVID}{dt}$$

Where LL is load-line, C_{OUT} is total output capacitance and dVID/dt is DVID fast slew rate. Thus V_{DVID_TH} = 50.33mV is needed in this case. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.566 = \frac{R2}{R1+R2} \times 3.2$$

$$0.625 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 44.15kΩ, R2 = 9.49kΩ.

- SET2 resistor network design :

  RAMP Setting is 400kHz, Disable HIGH FREQ RAMP and DVID_Width is chosen as 24μs typical. Last, the QR mechanism parameters need to be designed first. Initial QR_TH is designed as 25mV and QR_Width is designed as 0.44 x T_{ON}. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$0.661 = \frac{R2}{R1+R2} \times 3.2$$

$$0.925 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R 1 = 55.93kΩ, R2 = 14.58kΩ.

(1) Protection Settings :

- OVP protections : When VSEN pin voltage is 350mV more than VID, the OVP is latched.
- TSEN and $\overline{\text{VR\_HOT}}$ design : Using the following equation to calculate related resistances for $\overline{\text{VR\_HOT}}$ setting.

$$V_{TSEN} = 80\mu A \times \left(R1 // \left(R2 + R_{NTC\ (100°C)}\right)\right)$$

- Choosing R1 is open and an NTC thermistor R_{NTC}(25°C) = 100kΩ with β = 4485. When temperature is 100°C, the R_{NTC} (100°C) = 4.85kΩ. Then R2 = 8.8kΩ can be calculated.

AXG VR

No Load Offset (Platform)

The AXG VR features no load offset function which provides the possibility of wide range positive offset of output voltage. Users can disable offset function by simply connecting OFSA/PSYS pin to GND. Figure 28 shows a voltage divider used to set no load offset voltage. No load offset voltage setting is :

$$V_{OFS\_AXG} = 0.4 \times (V_{OFSA} - 1.7)$$

The range of V_{OFS_AXG} is between –500mV and 590mV and the resolution is 10mV.

For example, for a 100mV no load offset requirement, V_{OFSA} needs to be set as 1.95V.

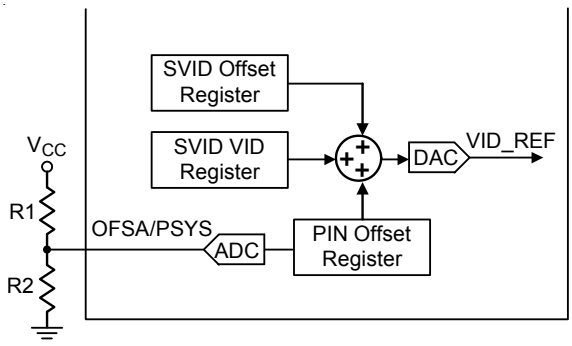


Figure 28. No Load Offset Circuit

Switching Frequency Setting

As mentioned in switching frequency setting section of CORE VR, connect a resistor R_{TONA} between input terminal and TONSETA pin to set the on-time width.

$$T_{ONA} = \frac{R_{TONA} \times 4.793p \times 1.2}{V_{IN} - V_{DAC}} \quad (V_{DAC} < 1.2)$$

$$T_{ONA} = \frac{R_{TONA} \times 4.793p \times V_{DAC}}{V_{IN} - V_{DAC}} \quad (V_{DAC} \geq 1.2)$$

For better efficiency in the given load range, the maximum switching frequency is suggested to be :

$$F_{SWA(MAX)} = \frac{VID1 + \frac{IccTDC}{N} \cdot \left(DCR + \frac{R_{ON\_LS,max}}{n_{LS}} - N \cdot R_{LL} \right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} - \frac{R_{ON\_HS,max}}{n_{HS}} \right) \right] \cdot (T_{ONA} - T_D + T_{ONA,VAR}) + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} \right) \cdot T_D}$$

where $F_{SW(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN\,(MAX)}$ is the maximum application input voltage, IccTDC is the thermal design current of application, N is the phase number. The $R_{ON\_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$, and n_{HS} is the number of high-side MOSFETs; $R_{ON\_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for the RT3607BC.

When load increases, on-time keeps constant. The off-time width is reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Per Phase Current Sense

In the RT3607BC, the current signal is used for load-line setting and Over-Current Protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in the Figure 29. When inductance and DCR time constant is equal to $R_{AX}C_{AX}$ filter network time constant, a voltage I_{LAx} x DCR drops on C_{AX} to generate inductor current signal. According to the Figure 29, the ISENAxN is as follows :

$$ISENAxN = \frac{I_{LAX} \times DCR}{R_{CSAx}}$$

Where L_{AX} / DCR = $R_{AX}C_{AX}$ is held. The method can get high efficiency performance, but DCR value will be drifted by temperature, so an NTC resistor should be added in the resistor network at the IMONA pin to achieve DCR thermal compensation.

In the RT3607BC design, the resistance of R_{CSAx} is restricted to be 680Ω; moreover, the error of R_{CSAx} is recommended to be 1% or smaller. R_X is highly recommended as two 0603 size resistors in series to alleviate the I_{OUT} reporting inaccuracy issue at no load due to the VCR (voltage coefficient of resistance) effect.

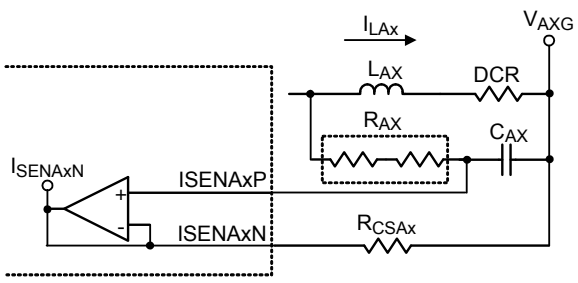


Figure 29. Lossless Current Sense Method

Total Current Sense

As presented in total current sense section of AXG VR, Figure 30 shows the total current sense method which connects the resistor network between IMONA and VREF pins to set a part of current loop gain for load-line (droop) setting and set accurate over current protection.

$$V_{IMONA} - V_{REF} = \frac{DCR}{R_{CS}} \times R_{EQA} \times (I_{LA1} + I_{LA2})$$

R_{EQA} includes an NTC resistor to compensate DCR thermal drifting for high accuracy load-line (droop).

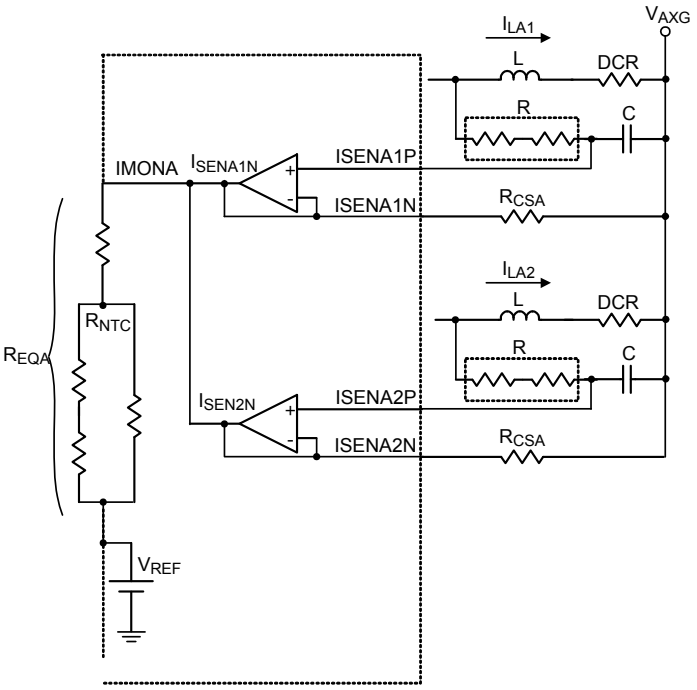


Figure 30. Total Current Sense Method

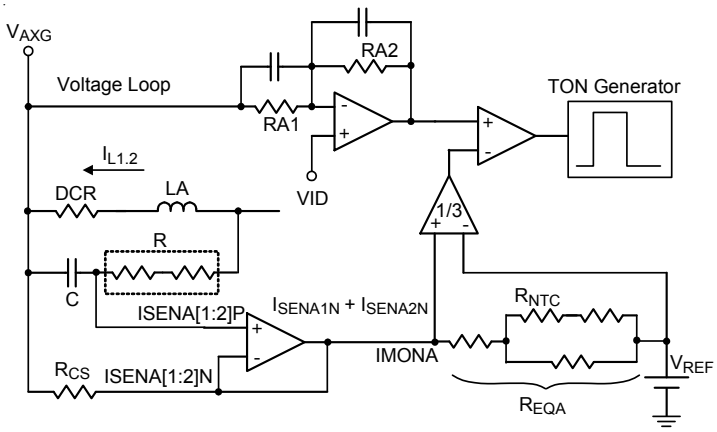


Figure 32. Voltage Loop and Current Loop

Load-Line (Droop) Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop. The load-line is a slope between load current I_{CCA} and output voltage V_{AXG} as shown in Figure 31. Figure 32 shows the voltage control and current loop. By using both the loops, the load-line (droop) can be set easily. The load-line set equation is :

$$R_{LLA} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CS}} \times R_{EQA}}{\frac{RA2}{RA1}} (m\Omega)$$

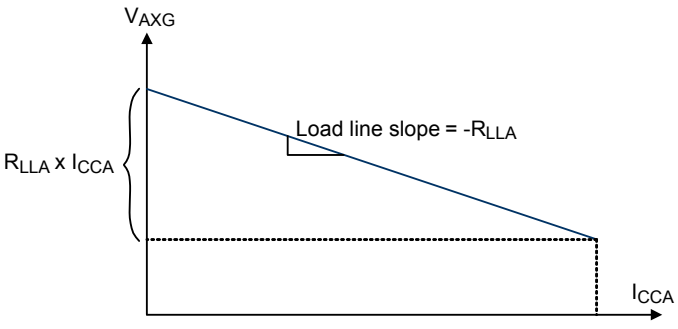


Figure 31. Load-Line (Droop)

Compensator Design

The compensator of the RT3607BC doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in G-NAVP™ topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 33, the transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range

$$G_{CON}(S) \approx \frac{A_I}{R_{LLA}} \frac{1 + \frac{s}{\omega \times f_{SWA}}}{1 + \frac{s}{\omega ESRA}}$$

Where A_I is current loop gain, R_{LLA} is load line for AXG VR, f_{SWA} is switching frequency for AXG VR and ω_{ESRA} is a pole that should be located at 1 / (C_{OUTA} x ESR). Then the CA1 and CA2 should be designed as follows :

$$CA1 = \frac{1}{RA1 \times \pi \times f_{SWA}}$$

$$CA2 = \frac{C_{OUTA} \times ESR}{RA2}$$

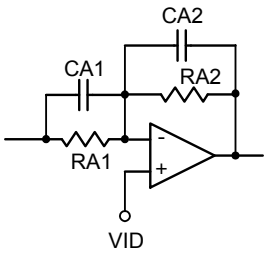


Figure 33. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, V_{CCAXG_SENSE} and V_{SSAXG_SENSE}. Connect RGNDA to V_{SSAXG_SENSE} and connect FBA to V_{CCAXG_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 34. The V_{DAC} and the precision voltage reference are referred to RGNDA for accurate remote sensing.

Maximum Processor Current Setting, ICCMAXA

The maximum processor current ICCMAXA can be set by the SETA1 pin. ICCMAXA register is set by an external voltage divider with the multi-function mechanism. Table 9 shows the ICCMAXA setting on the SETA1 pin. For example, ICCMAXA = 40A, the V_{SETA1} needs to be set as 0.253V. Additionally, $V_{IMONA} - V_{REF}$ needs to be set as 1.6V at ICCMAXA. The ICCMAXA alert signal is pulled to low level when

$V_{IMONA} - V_{REF}$ = 1.6V (for maximum phase >1)

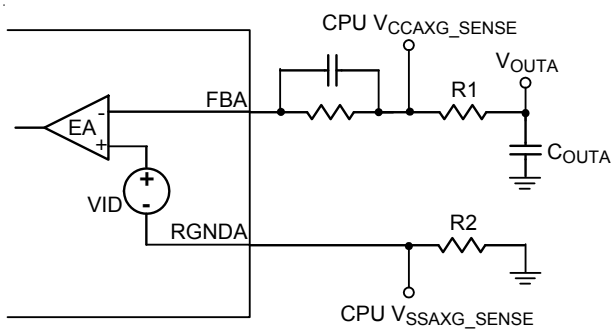


Figure 34. Remote Sensing Circuit

Table 9. SETA1 Pin Setting for ICCMAXA

$V_{divider\_SETA1}$ (mV)	ICCMAXA	Unit
3.125	0	A
15.625	2	A
28.125	4	A
40.625	6	A
53.125	8	A
65.625	10	A
78.125	12	A
90.625	14	A
103.125	16	A
115.625	18	A
128.125	20	A
140.625	22	A
153.125	24	A
165.625	26	A
178.125	28	A
190.625	30	A
203.125	32	A
215.625	34	A
228.125	36	A
240.625	38	A
253.125	40	A
265.625	42	A
278.125	44	A
290.625	46	A
303.125	48	A
315.625	50	A
328.125	52	A
340.625	54	A
353.125	56	A
365.625	58	A
378.125	60	A
390.625	62	A
403.125	64	A
415.625	66	A
428.125	68	A

$V_{divider\_SETA1}$ (mV)	ICCMAXA	Unit
440.625	70	A
453.125	72	A
465.625	74	A
478.125	76	A
490.625	78	A
503.125	80	A
515.625	82	A
528.125	84	A
540.625	86	A
553.125	88	A
565.625	90	A
578.125	92	A
590.625	94	A
603.125	96	A
615.625	98	A
628.125	100	A
640.625	102	A
653.125	104	A
665.625	106	A
678.125	108	A
690.625	110	A
703.125	112	A
715.625	114	A
728.125	116	A
740.625	118	A
753.125	120	A
765.625	122	A
778.125	124	A
790.625	126	A
803.125	128	A
815.625	130	A
828.125	132	A
840.625	134	A
853.125	136	A
865.625	138	A

$V_{divider\_SETA1}$ (mV)	ICCMAXA	Unit
878.125	140	A
890.625	142	A
903.125	144	A
915.625	146	A
928.125	148	A
940.625	150	A
953.125	152	A
965.625	154	A
978.125	156	A
990.625	158	A
1003.125	160	A
1015.625	162	A
1028.125	164	A
1040.625	166	A
1053.125	168	A
1065.625	170	A
1078.125	172	A
1090.625	174	A
1103.125	176	A
1115.625	178	A
1128.125	180	A
1140.625	182	A
1153.125	184	A
1165.625	186	A
1178.125	188	A
1190.625	190	A
1203.125	192	A
1215.625	194	A
1228.125	196	A
1240.625	198	A
1253.125	200	A
1265.625	202	A
1278.125	204	A
1290.625	206	A
1303.125	208	A

$V_{divider\_SETA1}$ (mV)	ICCMAXA	Unit
1315.625	210	A
1328.125	212	A
1340.625	214	A
1353.125	216	A
1365.625	218	A
1378.125	220	A
1390.625	222	A
1403.125	224	A
1415.625	226	A
1428.125	228	A
1440.625	230	A
1453.125	232	A
1465.625	234	A
1478.125	236	A
1490.625	238	A
1503.125	240	A
1515.625	242	A
1528.125	244	A
1540.625	246	A
1553.125	248	A
1565.625	250	A
1578.125	252	A
1590.625	254	A

Dynamic VID (DVID) Compensation for AXG VR

As mentioned in DVID compensation section of CORE VR, the RT3607BC also provide a DVID compensation function for AXG VR. A virtual charge current signal can be established by SETA1 and SET3 pins to cancel the real induced charge current signal.

Table 10 shows the DVID_Threshold on SETA1 pin with internal 80μA current source and Table 4 describes DVID_Width settings on SET3 pin with internal 80μA current source. For example, 39.67mV DVID_Threshold (SR = 11.25mV/μs) and 36μs DVID_Width are designed (QR width = 88%). According to Table 10 and Table 4, the DVID_Threshold set voltage should be 0.25V and the DVID_Width set voltage should be 0.95V. Please note that a high accuracy resistor is needed for this setting, < 1% error tolerance is recommended.

Table 10. SETA1 Pin Setting for DVID_Threshold

V_{IxR_SETA1} (mV)	DVID_Threshold_A
50	18.33mV
150	29mV
250	39.67mV
350	50.33mV
450	61mV
550	71.67mV
650	82.33mV
750	93mV
850	18.33mV
950	29mV
1050	39.67mV
1150	50.33mV
1250	61mV
1350	71.67mV
1450	82.33mV
1550	93mV

Table 11. SETA2 Pin Setting for OCP and Ramp setting

$V_{divider\_SETA2}$ (mV)	OCP_A = %ICCMAX	Ramp Setting_A, if Ramp Offset_A = 0kHz	Ramp Setting_A, if Ramp Offset_A = 50kHz
25	110%	300kHz	350kHz
75		400kHz	450kHz
125		500kHz	550kHz
175		600kHz	650kHz
225	110%	300kHz	350kHz
275		400kHz	450kHz
325		500kHz	550kHz
375		600kHz	650kHz
425	120%	300kHz	350kHz
475		400kHz	450kHz
525		500kHz	550kHz
575		600kHz	650kHz
625	130%	300kHz	350kHz
675		400kHz	450kHz
725		500kHz	550kHz
775		600kHz	650kHz
825	140%	300kHz	350kHz
875		400kHz	450kHz
925		500kHz	550kHz
975		600kHz	650kHz
1025	150%	300kHz	350kHz
1075		400kHz	450kHz
1125		500kHz	550kHz
1175		600kHz	650kHz
1225	160%	300kHz	350kHz
1275		400kHz	450kHz
1325		500kHz	550kHz
1375		600kHz	650kHz
1425	160%	300kHz	350kHz
1475		400kHz	450kHz
1525		500kHz	550kHz
1575		600kHz	650kHz

RAMP Setting

RAMP plays an important role in the balance of loop stability and transient response. It also helps to smooth power state transition process. The ramp height should link with switching frequency. After switching frequency is decided, the ramp still can be slightly adjusted to fine tune performance. The RT3607BC provide RAMP setting function through SETA2 pin. SETA2 are used to select more specific switching frequency for AXG rail. Table 11 describes Ramp setting in SETA2 pin. Figure 35 shows the ramp compensation

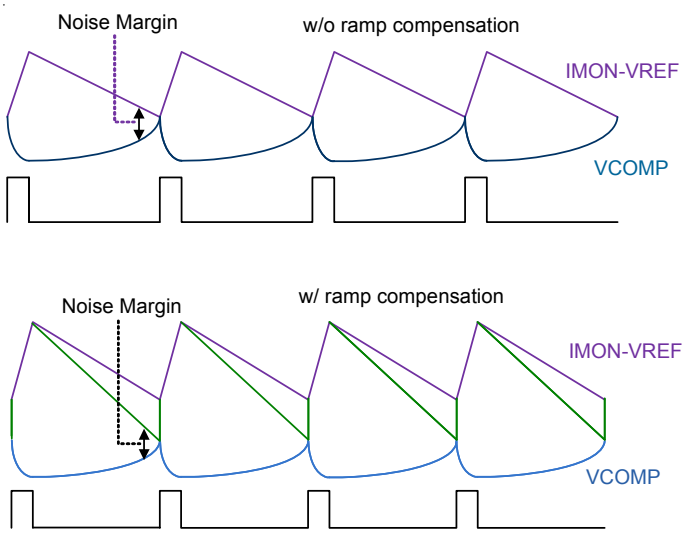


Figure 35

Quick Response (QR) Mechanism

As presented in QR mechanism section of CORE VR, the RT3607BC also supports QR function in AXG VR. The output voltage signal behavior needs to be detected so that QR mechanism can be trigged. The output voltage signal is via a remote sense line to connect at VSENA pin that is shown in Figure 36. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 24. A proper QR mechanism set can meet different applications. SETA2 can set QR threshold and SET3 can set QR width. QR threshold and QR width can set by internal current source 80μA with multi-function pin setting mechanism.

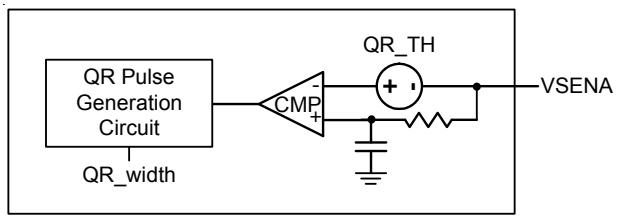


Figure 36. Simplified QR Trigger Schematic

For example, QR threshold 20mV/10mV at PS0/PS1(Ramp offset = +0kHz) According to Table 12, the set voltage should be 0.45V. 0.88 x TON QR width(DVID width = 48μs). According to Table 4, the set voltage should be 1.35V. Please note that a high accuracy resistor is needed for this setting accuracy, < 1% error tolerance is recommended.

Table 12. SETA2 Pin Setting for QR Threshold and Ramp Offset Setting

V_{IxR_SET2} (mV)	QR Threshold		Ramp Offset Setting_A
	PS0	PS1	
50	15mV	10mV	+0 kHz
150			+50 KHz
250	15mV	15mV	+0 KHz
350			+50 KHz
450	20mV	10mV	+0 kHz
550			+50 kHz
650	20mV	15mV	+0 kHz
750			+50 kHz
850	25mV	10mV	+0 kHz
950			+50 kHz
1050	25mV	15mV	+0 kHz
1150			+50 kHz
1250	30mV	10mV	+0 kHz
1350			+50 kHz
1450	30mV	15mV	+0 kHz
1550			+50 kHz

Current Monitor, IMONA

The RT3607BC includes a current monitor (IMONA) function which can be used to detect over current protection and the maximum processor current ICCMAXA, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMONA and VREF pins.

The calculation for IMONA-VREF voltage is shown as below :

$$V_{IMONA} - V_{REF} = \frac{DCR}{R_{CSA}} \times R_{EQA} \times (I_{LA1} + I_{LA2})$$

Where $I_{LA1} + I_{LA2}$ are output current and the definitions of DCR, R_{CSA} and R_{EQA} can refer to Figure 29.

Over Current Protection

The RT3607BC provides the Over Current Protection (OCP) which is set by the SETA2 pin in AXG VR. The OCP threshold setting can refer to ICCMAXA current in Table 11. For example, if ICCMAXA is set as 120A (130% ICCMAX, Ramp = 400kHz), user can set voltage by using the external voltage divider on SETA2 pin as 0.675V typically.

According to Table 11, the set voltage should be 0.675V When output current is higher than the OCP threshold, OCP is latched with a 40µs delay to prevent false trigger. Besides, the OCP function is masked when dynamic VID transient occurs, and soft-start period. And the OCP function is re-active 46µs after DVID or soft-start alert is asserted.

Output Over-Voltage Protection

An OVP condition is detected when the VSENA pin is 150mV more than VID. as VID > 1V. If VID < 1V, the OVP is detected when the VSEN pin is 350mV more than 1V. When OVP is detected, the high-side gate voltage UGATEAx is pulled low and the low-side gate voltage LGATEAx is pulled high, OVP is latched with a 0.5µs delay to prevent false trigger. Besides, the OVP function is masked during DVID and soft-start period. 46µs after DVID or soft-start alert is asserted, the OVP function is re-active.

Negative Voltage Protection

Since the OVP latch continuously turns on all low-side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSENA detects a voltage below –0.07V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs reCORE off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.07V due to OVP latch and NVP triggering. The NVP function is active only after OVP is triggered.

Current Loop Design in Details

Figure 37 shows the whole current loop structure. The current loop plays an important role in the RT3607BC that can decide ACLL performance, DCLL accuracy and ICCMAXA accuracy. For ACLL performance, the correct compensator design is assumed, and if RC network time constant matches inductor time constant L_{AX} / DCR_X, an ideal load transient waveform can be designed. If R_XC_X network time constant is larger than inductor time constant L_{AX} / DCR_X, V_{AXG} waveform has a sluggish droop during load transient. If R_XC_X network is smaller than inductor time constant L_{AX} /DCR_X, V_{AXG} waveform sags to create an undershooting to fail the specification.

For DCLL performance and ICCMAXA accuracy, since the copper wire of inductor has a positive temperature coefficient, when temperature goes high in the heavy load condition, DCR value goes large simultaneously. A resistor network with NTC thermistor compensation connecting between the IMONA to REF pins is necessary, to compensate the positive temperature coefficient of inductor DCR. The design flow is as presented in current loop design in details of CORE VR.

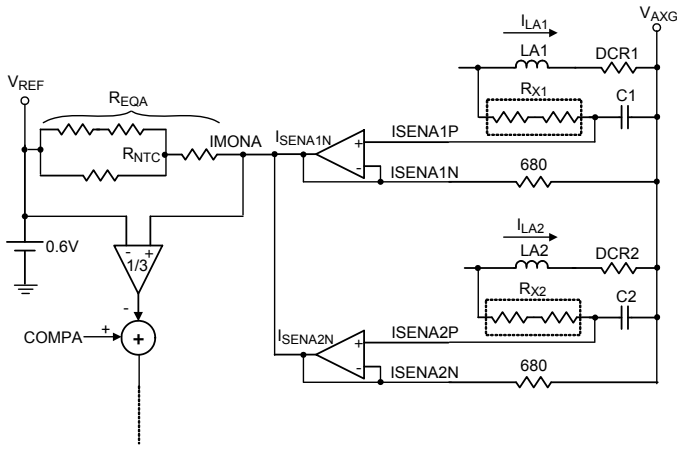


Figure 37. Current Loop Structure

System Input Power Monitor, PSYS

The RT3607BC provides PSYS function to monitor total platform system power, and the obtained information will be provided directly to the CPU via the SVID interface. The PSYS function can be enabled/disabled by the SET3 pin. The PSYS function can be described as in Figure 38. When PSYS voltage V_{PSYS} = 3.2V, the RT3607BC will generate an 8-bit code, FF, for 100% Pmax, which will be stored in the 1Bh register. To choose the resistor value R, for example, if the maximum current from the PSYS "Meter" I = 320μA in conjunction with V_{PSYS} = 3.2V for 100% Pmax, R = V_{PSYS} / I =10kΩ can be obtained. The resistor must be as close to the RT3607BC as.

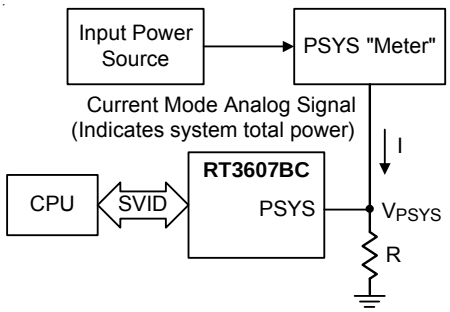


Figure 38. PSYS Function Block Diagram

Design Step

The RT3607BC excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. There are three main design procedures for the RT3607BC design. The first step is initial settings, second step is loop design and the last step is protection settings. The following design example is to explain the RT3607BC design procedure :

	V_{AXG} Specification
Input Voltage	12V
No. of Phases	2
Vboot	0.9V
ICCMAX	76A
ICC-DY	42A
ICC-TDC	45A
Load Line	3.1mΩ
Fast Slew Rate	10mV/μs
Max Switching Frequency	400kHz

In IMVP8 VRTB Guideline, the output filter requirements of VRTB specification for desktop platform are :

Output Inductor : 220nH/0.49mΩ

Output Bulk Capacitor : 470μF/2.5V/7mΩ (max) 4 to 5pcs

Output Ceramic Capacitor : 22μF/0805 (14pcs max in cavity)

(1) Initial Settings :

The RT3607BC initial voltage is 0.9V.

(2) Loop Design :

On time setting : Using the specification, T_{ONA} is

$$T_{ONA} = \frac{R_{ONA} \times 4.73p \times 1.2}{V_{IN}-V_{DAC}} (V_{DAC} < 1.2) = 204n$$

The on time setting resistor R_{TONA} = 400kΩ

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an ideal load transient waveform, RxCx time constant needs to match Lx / DCRx per phase. Cx = 0.47μF is set, then

$$R_X = \frac{L_X}{0.47\mu F \times DCR_X} = 780\Omega$$

- IMONA resistor network design : T_L = 25°C, T_R = 50°C, T_H = 100°C, NTC thermistor = 100kΩ@25°C, β = 4485 and ICCMAXA = 76A. According to the sub-section "Current Loop Design in Details", R_{IMONA1} = 10.6kΩ, R_{IMONA2} = 15.05kΩ and R_{IMONA3} = 11.46kΩ can be determined. The R_{EQA}(25°C) = 23.86kΩ.
- Load-line design : 2.1mΩ droop is requirement and because R_{EQA}(25°C) has been determined, the voltage loop Av gain also can be determined by following equation

$$R_{LLA} = \frac{A_I}{A_V} = \frac{\frac{1}{3} \times \frac{DCR}{R_{CSA}} \times R_{EQA}}{\frac{R2}{R1}} (m\Omega)$$

Where DCR (25°C) = 0.6mΩ, R_{CS} = 680Ω and R_{EQA}(25°C) = 23.86kΩ. Hence the A_V = R2 / R1 = 2.26 can be obtained. R = 10kΩ usually is determined, so R2 = 22.6kΩ.

- Typical compensator design can use the following equations to design the C1 and C2 values

$$C1 = \frac{1}{R1 \times \pi \times f_{SWA}} \approx 87pF$$

$$C2 = \frac{C_{OUT} \times ESR}{R2} \approx 115pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero of the compensator can be designed close to 1/10 of switching frequency.

- SETA1 resistor network design : First the ICCMAX is design as 76A. Next, DVID compensation parameters need to be decided. The DVID_TH can be calculated as following equation

$$V_{DVID\_TH} = LL \times C_{OUT} \times \frac{dVID}{dt}$$

Where LL is load line, C_{OUT} is total output capacitance and dVID/dt is DVID fast slew rate. Thus V_{DVID_TH} = 39.67mV is needed in this case. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$0.478 = \frac{R2}{R1+R2} \times 3.2$$

$$0.25 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 20.915kΩ, R2 = 3.674kΩ.

- SETA2 resistor network design :

First the OCP threshold is designed as 1.6 x ICCMAX. Ramp Setting is 400kHz and Initial QR_TH is designed as 20/15mV. By using the information, the two equations can be listed by using multi-function pin setting mechanism

$$1.275 = \frac{R2}{R1+R2} \times 3.2$$

$$0.65 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 20.39kΩ, R2 = 13.50kΩ.

- SET3 resistor network design : First the PSYS is design Enable. CORE rail DVID_TH and QR_TH are chosen 24us and 44%. AXG rail are chosen 24us and 44%. By using above information, the two equations can be listed by using multi-function pin setting mechanism

$$1.125 = \frac{R2}{R1+R2} \times 3.2V$$

$$0.65 = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

R1 = 23.11kΩ, R2 = 12.53kΩ.

(3) Protection Settings :

- OVP protections : When the VSENA pin voltage is 350mV more than VID, the OVP is latched. When VSENA pin voltage is 350mV less than VID, the UVP is latched.
- TSEN and $\overline{VR\_HOT}$ design : Use the following equation to calculate related resistances for $\overline{VR\_HOT}$ setting.

$$V_{TSENA} = 80\mu A \times \left(RA1 // \left(RA2 + R_{ANTC\ (100°C)}\right)\right)$$

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-60L 7x7, the thermal resistance, θ_{JA}, is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (25.5°C/W) = 3.92W for a WQFN-60L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 39 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

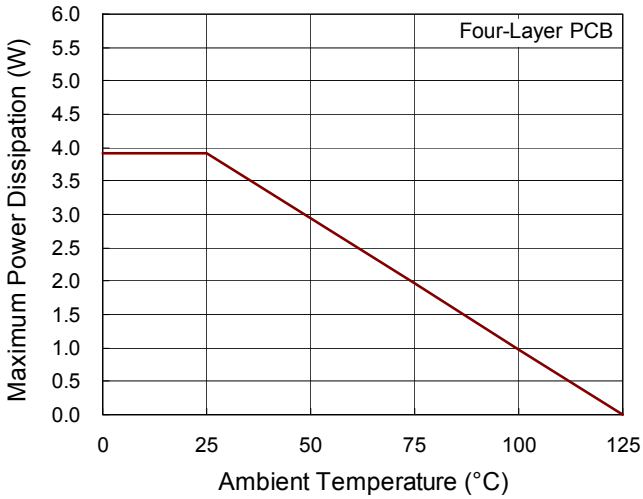
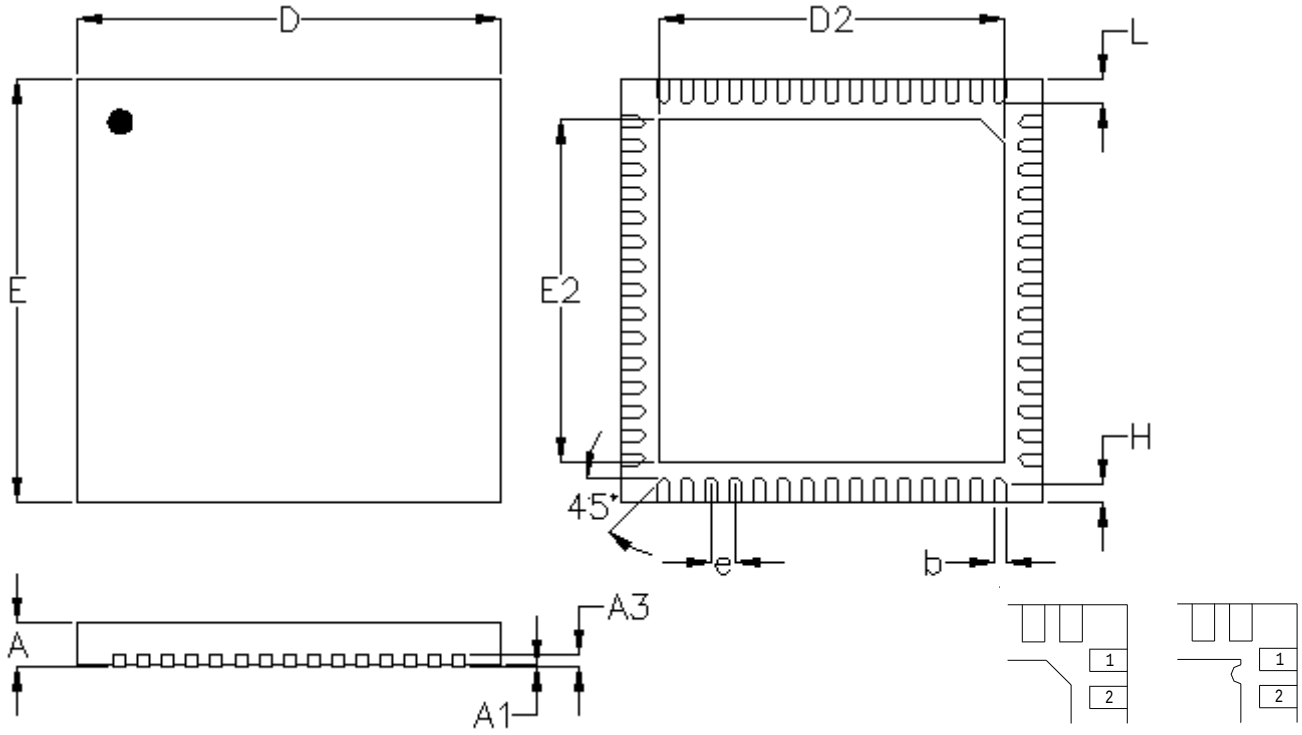


Figure 39. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

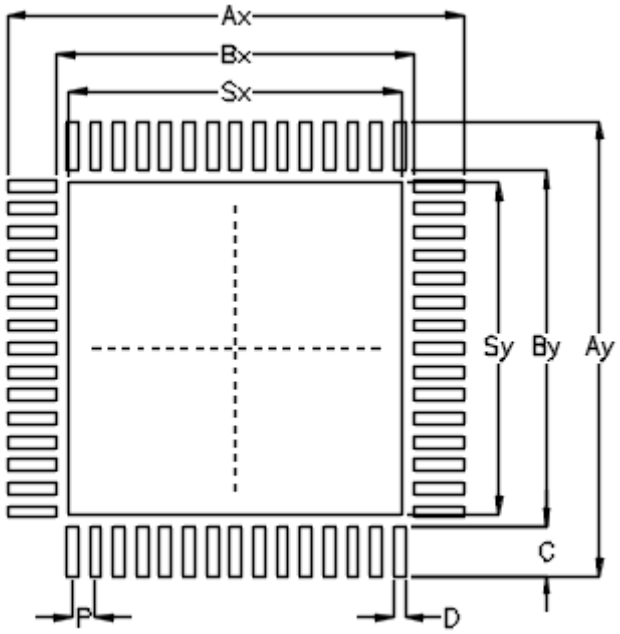
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-60	60	0.40	7.80	7.80	6.10	6.10	0.85	0.20	5.70	5.70	±0.05

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