General Description

The HL7550L series is a high voltage ultralow-power,low dropout voltage regulator. The device can deliver 100mA output current with a dropout voltage of 450mV@ 100mA and allows an input voltage as high as 24V. The typical quiescent current is only 2.5μA.

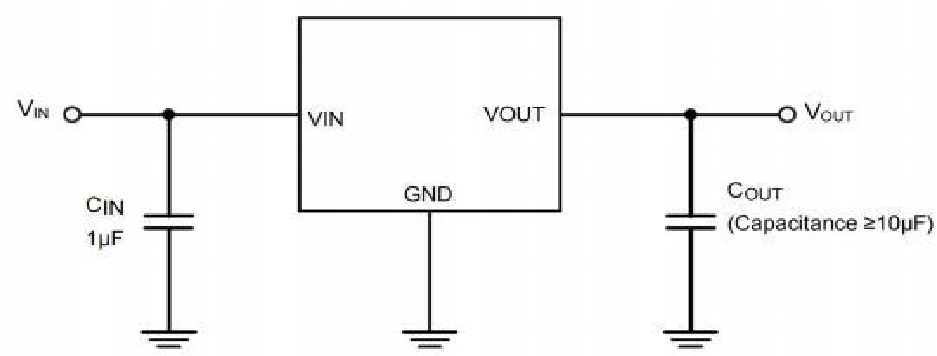
Features

- SLow Power Consumption: 2.5μA (Typ)
- Maximum Output Current: 150mA
- Operating Voltage Range: 5.5~24V
- Output Voltage Accurate: ±2%
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection Output Current Limit
- Low Temperature Coefficient
- Stable with Ceramic Capacitor
- RoHS Compliant and Lead (Pb) Free
- -40℃ to +85℃ Operating Temperature Range
- Fixed Output Voltage Versions:5V
- Available in Green SOT89-3 Packages

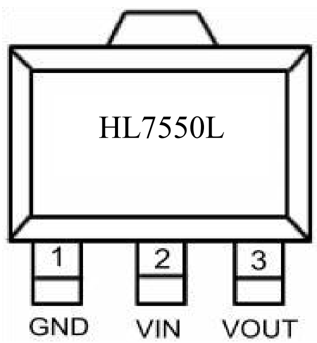
Applications

- Portable, Battery Powered Equipment
- Audio/Video Equipmen
- Home Automation
- Electronic fingerprint lock
- Smoke detector and sensor
- Weighting Scales

Typical Applications



Package and Pin Description



Pin Description

Pin No	Pin Name	Pin Description
1	GND	Ground
2	VIN	Power Input
3	VOUT	Output Voltage

Pin Description

Device	Device Marking	Device Package	Quantity
HL7550L	7550	SOT89-3	4,000

Absolute maximum rating

Parameter	Symbol	Conditions	Ratings	Unit
Supply Input Voltage	V_{IN}	-	-0.3 ~ 30	V
Regulated Output Voltage	V_{OUT}	-	5	V
Output Current	I_{OUT}	-	Internally limited	mA
Power Dissipation PD@TA=25℃	P_D	-	700	mW
Thermal Resistance	θ_{JA}	-	180	℃/W
Human Body Model	±2000			V
Charged Device Mode	±1000			V
Machine Mode	200			V
Storage Temperature Range	T_{STG}	-	-65 ~ 150	℃
Operating Junction Temperature	T_J	-	150	℃
Lead Temperature (Soldering 10s)	T_{LEAD}	-	260	℃

Note:

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device . These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated. conditions for extended period may affect device reliability.

2 Ratings apply to ambient temperature at 25°C.

3 The package thermal impedance is calculated in accordance to JESD 51-7.

Recommended Operating Conditions

Item	Min	Max	Unit
Operating Ambient Temperature	-40	85	℃
Input voltage	5.5	24	V
Output Voltage	4.9	5.1	V

Electrical Characteristics （Test Conditions:V_{IN}=V_{OUT}+1V,C_{IN}=C_{OUT}=1uF,T_A=25℃,unless otherwise specifi）

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	-	5.5	-	24	V
I_Q	Quiescent Current	VIN=12V,ILOAD=0mA	-	2.5	3	μA
V_{OUT}	Output Voltage	VIN=12V,ILOAD=10mA	4.9	5	5.1	V
I_{OUT}	Output Current	VIN=VOUT+2V	-	150	-	mA
V_{DROP}	Dropout Voltage V_{OUT}=5V	ILOAD=100mA	-	450	-	mV
		ILOAD=150mA	-	700	-	mV
ΔV_{LINE}	Line Regulation	I_{LOAD}=1mA V_{OUT}+20V≦V_{IN}≦24V	-	0.15	-	%/V
ΔV_{LOAD}	Load Regulation	V_{IN}=V_{OUT}+2V 1mA≦I_{LOAD}≦100mA	-	-	20	mV
I_{SHORT}	Short Current	V_{OUT}=GND	-	80	-	mA
T_{SHDN}	Thermal Shutdown Temperature	-	-	160	-	℃
ΔT_{SHDN}	Thermal Shutdown Hysteresis	-	-	20	-	℃

Note:

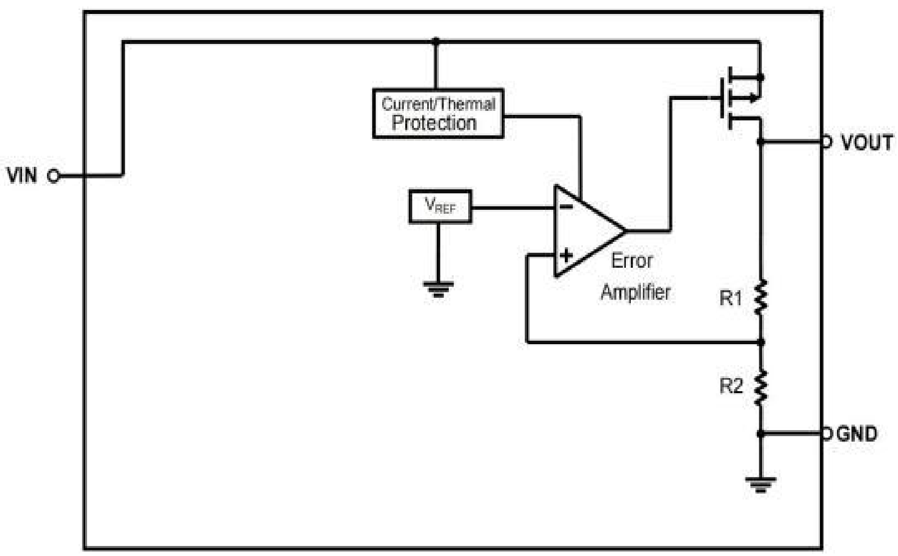
All limits specified at room temperature (TA = 25°C) unless otherwise specified.

All room temperature limits are 100% production tested.

All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods.

All limits are used to calculate Average Outgoing Quality Level (AOQL) .

Block diagram



Application Guideline

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 10 μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass- FET at specific output current (IRATED) while the pass-FET is fully operating at ohmic region and the pass- FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as (VDROP = VIN − VOUT = RDS(ON) x IRATED). Fornormal operation, the suggested LDO operating range is (VIN > VOUT + VDROP) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Therm al Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: T_A=25°C, AISIS DEMO PCB, The max $P_D = (T_J - T_A) / \theta_{JA}$.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

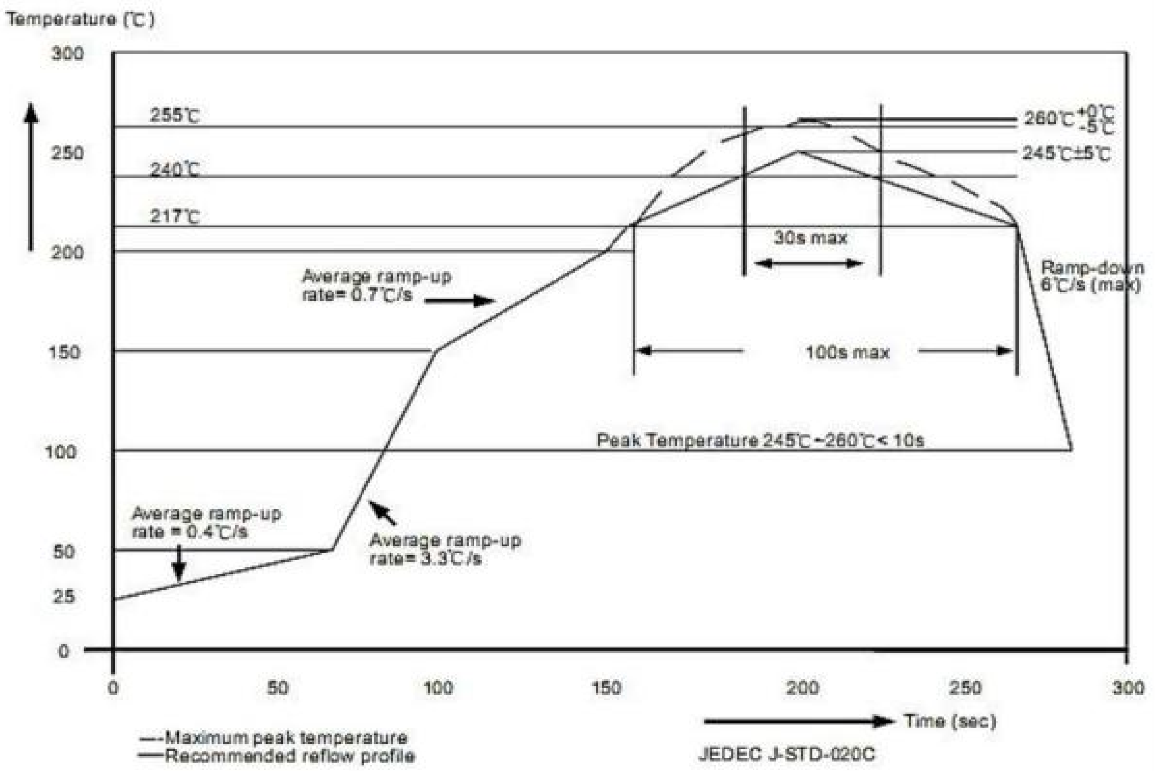
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HL7550L ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

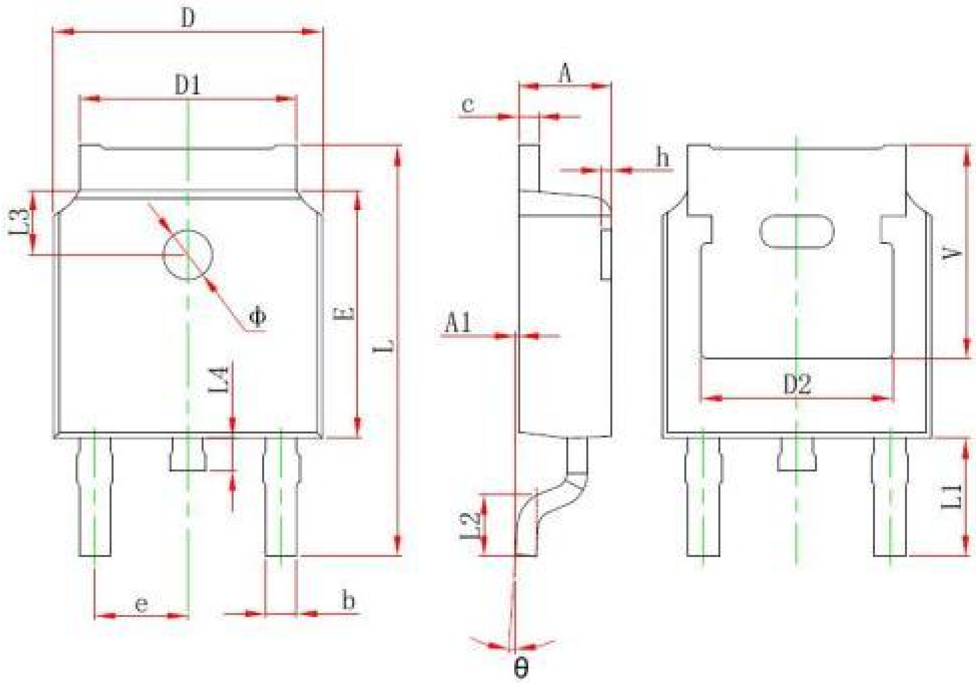
Packaging and welding process

The semiconductor products produced by Dersem Microelectronics follow the European RoHs standard, and the temperature of tin furnace in the packaging and welding process meets the J-STD-020 standard.



Package thickness	Volume mm3 < 350	Volume mm3：350~2000	Volume mm3 ≥ 2000
<1.6mm	260+0°C	260+0°C	260+0°C
1.6mm~2.5mm	260+0°C	250+0°C	245+0°C
≥2.5mm	250+0°C	245+0°C	245+0°C

Package information



Symbol	Min(mm)	Max(mm)
A	2.0	2.7
A1	-	0.2
b	0.5	1.1
c	0.3	0.8
D	6.3	6.9
D1	4.9	5.7
D2	4.83(REF)	
E	5.9	6.4
e	2.086	2.486
L	9.5	10.7
L1	2.9(REF)	
L2	1.2	1.9
L3	1.6(REF)	
L4	0.4	1.2
Φ	0.9	1.5
θ	0°	10°
h	-	0.5
V	5.35(REF)	

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