

20-V/300-mA Wide-Input High-PSRR Ultra-Low Noise LDO Regulator

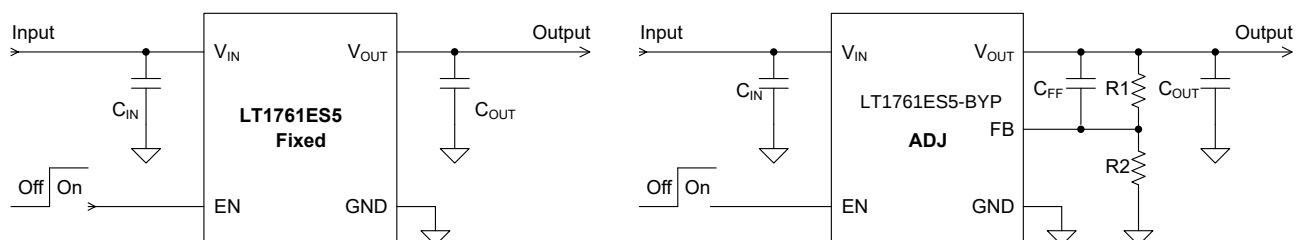
Features

- Input Voltage Range: 2.5 V to 20 V
- Output Voltage Range:
 - Adjustable: 1.22 V to 18 V
 - Fixed: 1.5 V to 5 V
- $\pm 2\%$ Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 300-mA Maximum Output Current
- Low Dropout Voltage: 550 mV Maximum at 300 mA
- High PSRR:
 - 79 dB at 1 kHz
 - 56 dB at 100 kHz
- 5.68- μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Stable with a 2.2- μF to 100- μF Ceramic Output Capacitor
- Integrated Protection:
 - Over-Current Protection
 - Output Short-Circuit Protection
 - Over-Temperature Protection
- Junction Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Package Options:
 - SOT23-5

Applications

- Low-Noise Power Supply
- High-Definition Imaging System
- Infrared Image Equipment
- Medical Equipment

Typical Application Circuit



Product Family Table

Generic Part Number	Orderable Part Number	Output Voltage	Package
LT1761ES5	TL1761ES5-BYP	Adjustable	SOT23-5
LT1761ES5	LT1761ES5-1.5	Fixed 1.5 V	SOT23-5
LT1761ES5	LT1761ES5-1.8	Fixed 1.8 V	SOT23-5
LT1761ES5	LT1761ES5-2.1	Fixed 2.1 V	SOT23-5
LT1761ES5	LT1761ES5-2.5	Fixed 2.5 V	SOT23-5
LT1761ES5	LT1761ES5-2.7	Fixed 2.7 V	SOT23-5
LT1761ES5	LT1761ES5-2.8	Fixed 2.8 V	SOT23-5
LT1761ES5	LT1761ES5-2.9	Fixed 2.9 V	SOT23-5
LT1761ES5	LT1761ES5-3	Fixed 3.0 V	SOT23-5
LT1761ES5	LT1761ES5-3.3	Fixed 3.3 V	SOT23-5
LT1761ES5	LT1761ES5-3.6	Fixed 3.6 V	SOT23-5
LT1761ES5	LT1761ES5-3.7	Fixed 3.7 V	SOT23-5
LT1761ES5	LT1761ES5-3.8	Fixed 3.8 V	SOT23-5
LT1761ES5	LT1761ES5-4	Fixed 4.0 V	SOT23-5
LT1761ES5	LT1761ES5-4.2	Fixed 4.2 V	SOT23-5
LT1761ES5	LT1761ES5-4.5	Fixed 4.5 V	SOT23-5
LT1761ES5	LT1761ES5-5	Fixed 5.0 V	SOT23-5

Pin Configuration and Functions

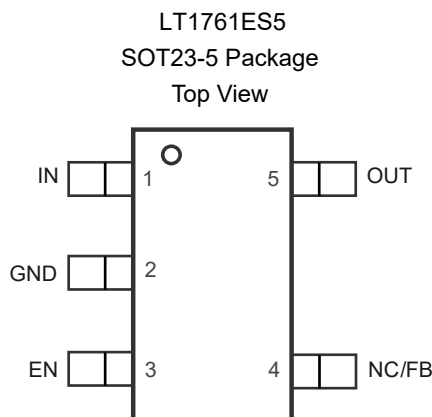


Table 1. Pin Functions: LT1761ES5

Pin No.	Name	I/O	Description
3	EN	I	Regulator enable pin. Drive EN high to turn on the regulator, and drive EN low to turn off the regulator.
4	FB	I	Output voltage feedback pin (adjustable output only). Connect to a resistor divider to adjust the output voltage.
2	GND	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
1	IN	I	Input voltage pin. Connect a 4.7- μ F or greater capacitor from IN to GND to reduce the jitter from the previous-stage power supply.
4	NC	–	No connection (fixed output only).
5	OUT	O	Regulated output voltage pin. Connect a 2.2- μ F to 100- μ F ceramic capacitor from OUT to GND to ensure regulator stability.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{IN}, V_{EN}		-0.3	24	V
V_{OUT} (fixed output only)		-0.3	6	V
V_{OUT} (adjustable output only)		-0.3	24	V
V_{FB} (adjustable output only)		-0.3	6	V
T_J	Maximum Junction Temperature	-40	150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{IN}		2.5	20	V
V_{EN}		0	V_{IN}	V
C_{OUT}		2.2	100	µF
T_J	Junction Temperature Range	-40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC, TOP}$	Unit
SOT23-5	162.4	79	62.33	°C/W

Electrical Characteristics

All test conditions: $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1\text{ V}$ or 2.5 V , whichever is greater; typically, $T_J = 25^{\circ}\text{C}$, $V_{\text{OUT}} = 3.3\text{ V}$, $C_{\text{IN}} = C_{\text{OUT}} = 4.7\text{ }\mu\text{F}$, and $C_{\text{FF}} = 100\text{ nF}$ for adjustable output, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current					
$V_{\text{IN}}^{(1)}$	Input Supply Voltage Range	$V_{\text{IN(MIN)}}$		20	V
UVLO	Input Supply Voltage Rising		2.25	2.4	V
	Hysteresis		200		mV
I_{Q}	Quiescent Current	$I_{\text{OUT}} = 0\text{ mA}$	98	160	μA
		$I_{\text{OUT}} = 1\text{ mA}$	127		μA
I_{SD}	Shutdown Current	$\text{EN} = \text{GND}$, $V_{\text{IN}} = V_{\text{IN(MIN)}}$ to 20 V	0.6	5	μA
Enable Input Voltage and Current					
$V_{\text{IH(EN)}}$	EN Input High Level (enable)	1.6		V_{IN}	V
$V_{\text{IL(EN)}}$	EN Input Low Level (disable)	0		0.5	V
I_{EN}	EN Pin Leakage Current	$V_{\text{EN}} = 0\text{ V}$ to 20 V	0.5	1	μA
Regulated Output Voltage and Current					
$V_{\text{OUT}}^{(2)}$	Output Voltage Accuracy	-2%		2%	
$V_{\text{FB}}^{(2)}$	Feedback Pin Voltage	Adjustable output only	1.22		V
$I_{\text{FB}}^{(2)}$	Feedback Pin Leakage Current	$V_{\text{FB}} = 1.5\text{ V}$	100		nA
ΔV_{OUT}	Line Regulation	$V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1\text{ V}$ to 20 V , $I_{\text{OUT}} = 1\text{ mA}$	0.007		%/V
	Load Regulation	$I_{\text{OUT}} = 1\text{ mA}$ to 300 mA	0.01		%/mA
$V_{\text{DO}}^{(3)}$	Dropout Voltage	$I_{\text{OUT}} = 100\text{ mA}$, $V_{\text{OUT}} = 5\text{ V}$	210	250	mV
		$I_{\text{OUT}} = 300\text{ mA}$, $V_{\text{OUT}} = 5\text{ V}$	350	550	mV
		$I_{\text{OUT}} = 100\text{ mA}$, $V_{\text{OUT}} = 3.3\text{ V}$	210	250	mV
		$I_{\text{OUT}} = 300\text{ mA}$, $V_{\text{OUT}} = 3.3\text{ V}$	350	550	mV
I_{LIM}	Output Current Limit	$V_{\text{OUT}} = 0.9 \times V_{\text{OUT(NOM)}}$	310	450	mA
I_{SC}	Short-Circuit Current Limit	V_{OUT} is forced to $\leq 20\text{ mV}$	180		mA
PSRR ⁽⁴⁾	Power Supply Rejection Ratio	$I_{\text{OUT}} = 100\text{ mA}$, $f = 120\text{ Hz}$	79		dB
		$I_{\text{OUT}} = 100\text{ mA}$, $f = 1\text{ kHz}$	79		dB
		$I_{\text{OUT}} = 100\text{ mA}$, $f = 100\text{ kHz}$	56		dB
		$I_{\text{OUT}} = 100\text{ mA}$, $f = 1\text{ MHz}$	41		dB
V_{N}	Output Noise Voltage ⁽⁴⁾	$I_{\text{OUT}} = 100\text{ mA}$, $\text{BW} = 10\text{ Hz}$ to 100 kHz	5.68		μV_{RMS}
t_{STR}	Start-up Time ⁽⁴⁾	From $\text{EN} \geq V_{\text{IH(EN)}}$ to $\text{OUT} \geq 95\%$ of $V_{\text{OUT(NOM)}}$	600		μs
Operating Temperature Range					

Parameter		Conditions	Min	Typ	Max	Unit
T _{SD}	Thermal Shutdown Temperature			165		°C
	Hysteresis			25		°C

(1) $V_{IN(MIN)} = V_{OUT(NOM)} + 1\text{ V}$ or 2.5 V , whichever is greater.

(2) FB pin is available for adjustable output only. Tolerance of external resistors is not included.

(3) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current and measure for $V_{OUT(NOM)} \geq 2.5\text{V}$. In the dropout mode, the output voltage will be equal to $V_{IN} - V_{DO}$.

(4) Not test during production. Measured with $C_{OUT} = 2.2\text{ }\mu\text{F}$.

Typical Performance Characteristics

All test conditions: $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 1\text{ V}$ or 2.5 V , whichever is greater; typically, $T_J = 25^{\circ}\text{C}$, $V_{\text{OUT}} = 3.3\text{ V}$, $C_{\text{IN}} = 4.7\text{ }\mu\text{F}$, $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$, and $C_{\text{FF}} = 100\text{ nF}$ for adjustable output, unless otherwise noted.

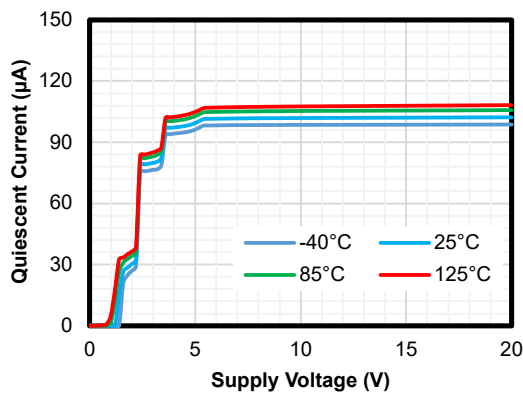


Figure 1. Quiescent Current vs Supply Voltage

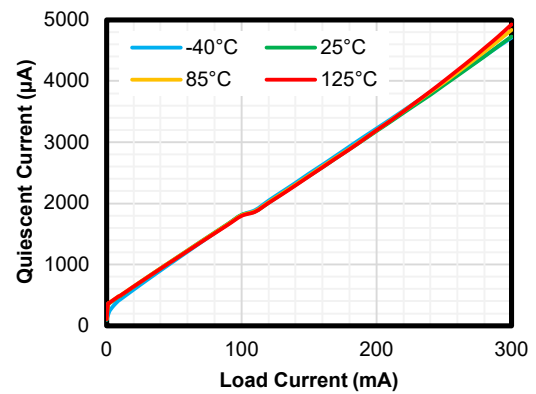


Figure 2. Quiescent Current vs Load Current

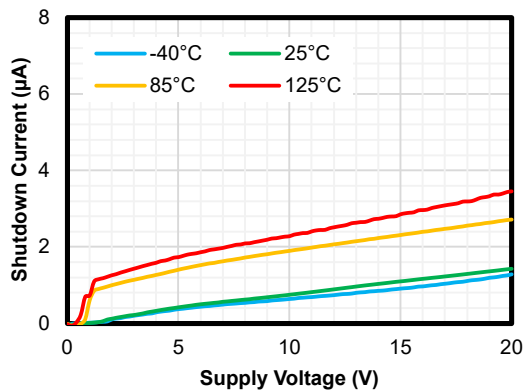


Figure 3. Shutdown Current vs Supply Voltage

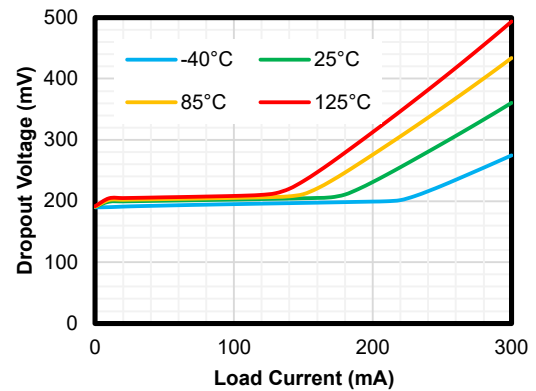


Figure 4. Dropout Voltage vs Load Current

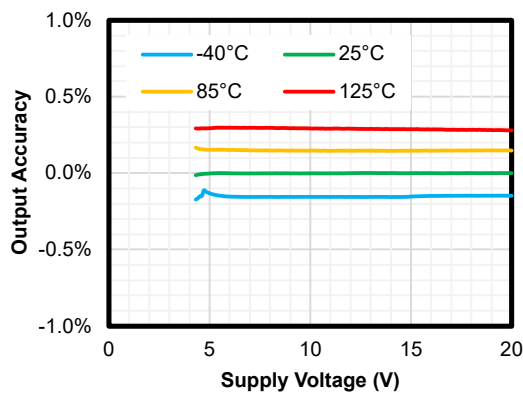


Figure 5. Line Regulation

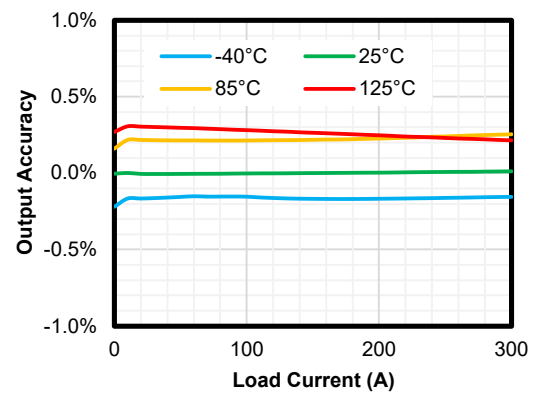


Figure 6. Load Regulation

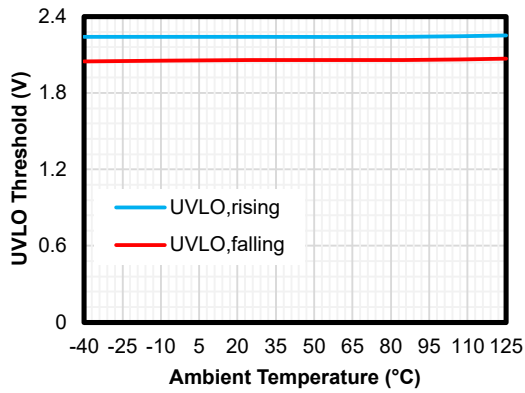


Figure 7. UVLO vs Temperature

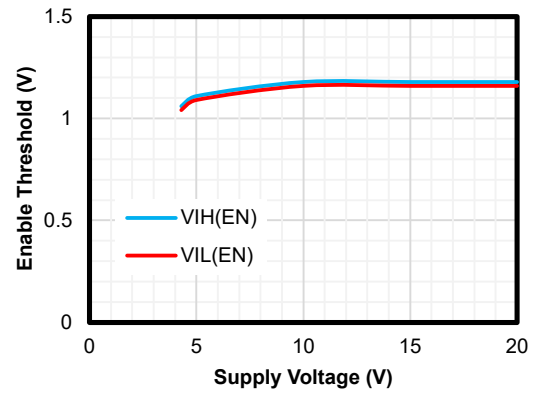


Figure 8. EN Threshold vs Supply Voltage

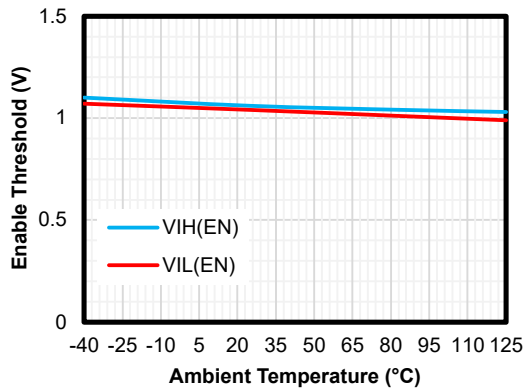


Figure 9. EN Threshold vs Temperature

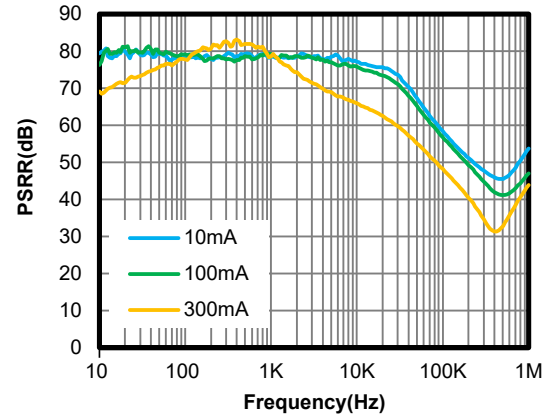


Figure 10. PSRR

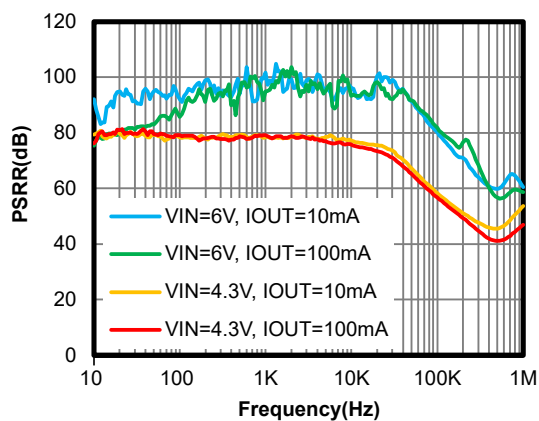


Figure 11. PSRR

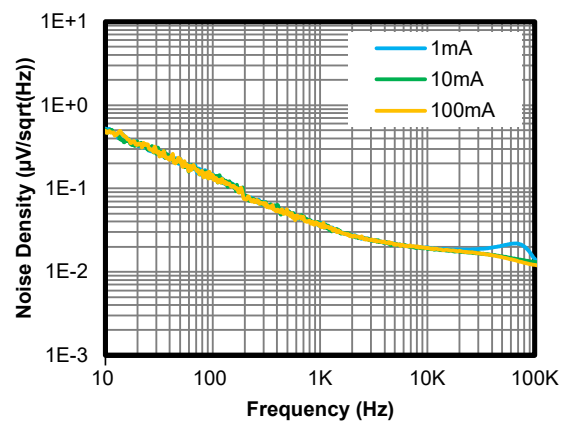


Figure 12. Noise

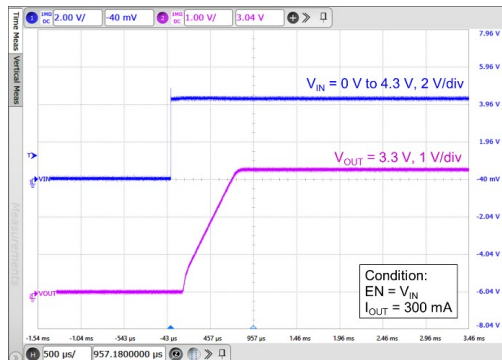


Figure 13. Startup with VIN

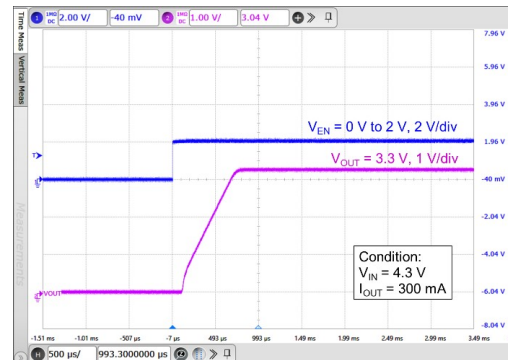


Figure 14. Startup with EN

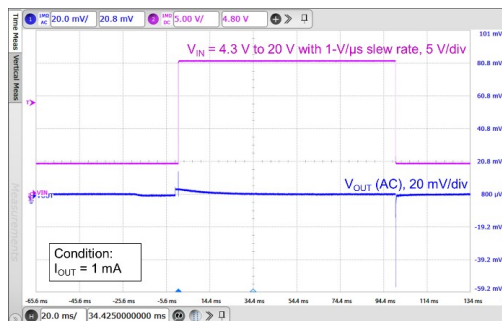


Figure 15. Line Transient

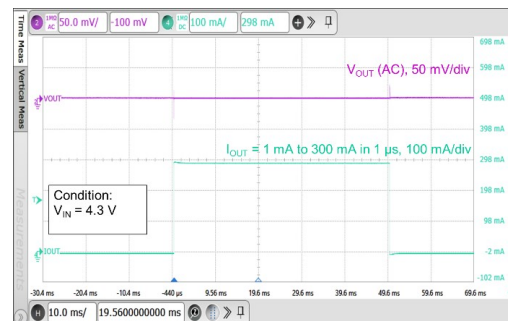


Figure 16. Load Transient

Detailed Description

Overview

The LT1761 series of products are 300-mA high PSRR, ultra-low noise, and low-dropout linear regulators with a 20-V wide input voltage range. The LT1761 series of products support both adjustable output voltage ranging from 1.22 V to 18 V with an external resistor divider and fixed output voltage ranging from 1.5 V to 5 V. The LT1761 series of products are stable with a 2.2- μ F to 100- μ F ceramic output capacitor.

The LT1761 series of products have high PSRR with 79 dB at 1 kHz and 5.68 μ V_{RMS} ultra-low noise. These features make the LT1761 series suitable for noise-sensitive applications, such as high-performance analog devices or high-definition imaging equipment, to suppress the large ripple and noise generated from the previous stage power supply. Besides, output short-circuit protection and thermal protection features improve system reliability under multiple operating conditions.

Functional Block Diagram

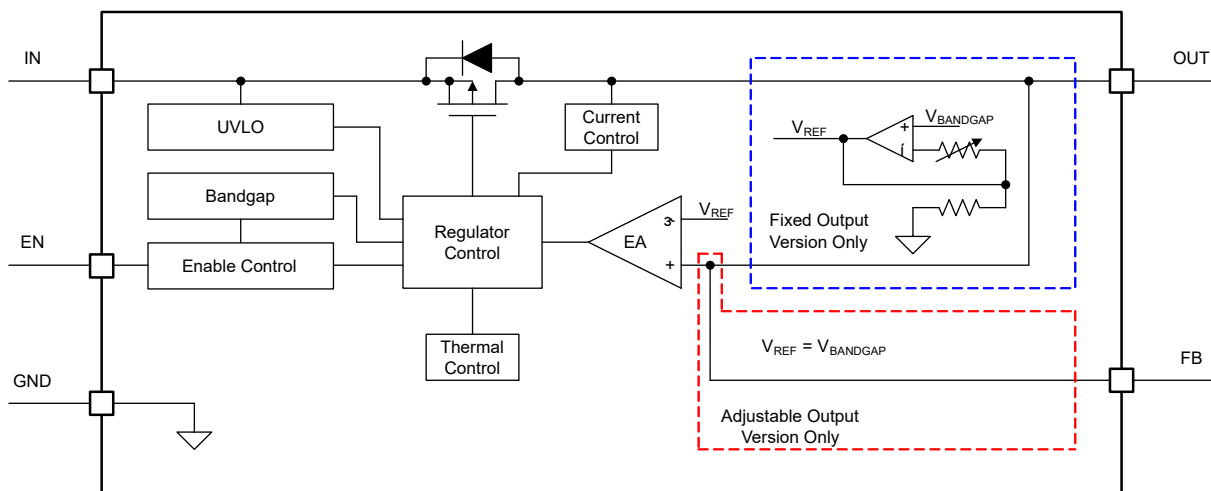


Figure 17. Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-Voltage Lockout (UVLO)

The LT1761 series uses an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the [Electrical Characteristics](#) table for the UVLO threshold and hysteresis.

Fixed Output Voltage

The LT1761 series is available in fixed voltage versions of 1.5 V to 5 V. When the input voltage is higher than $V_{OUT(NOM)} + 1$ V, the output voltage is well regulated according to the selected voltage option. When the input voltage falls below $V_{OUT(NOM)} + 1$ V, the output voltage tracks the input voltage minus the dropout voltage according to the load current. When the input voltage falls below UVLO, the output turns off.

Application Information

The LT1761 devices are a series of 20-V, 300-mA high PSRR, ultra-low noise, low-dropout linear regulators. The following application schematics show the typical usage of the LT1761 series.

Typical Application

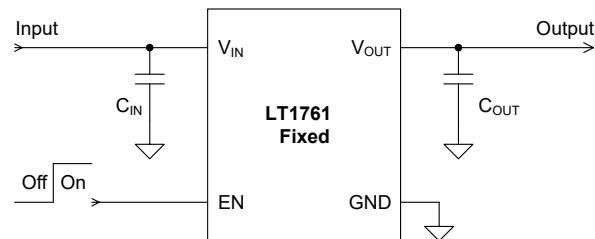


Figure 18. Typical Application Schematic of Fixed Output

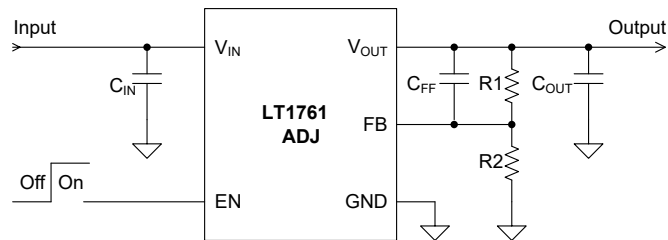


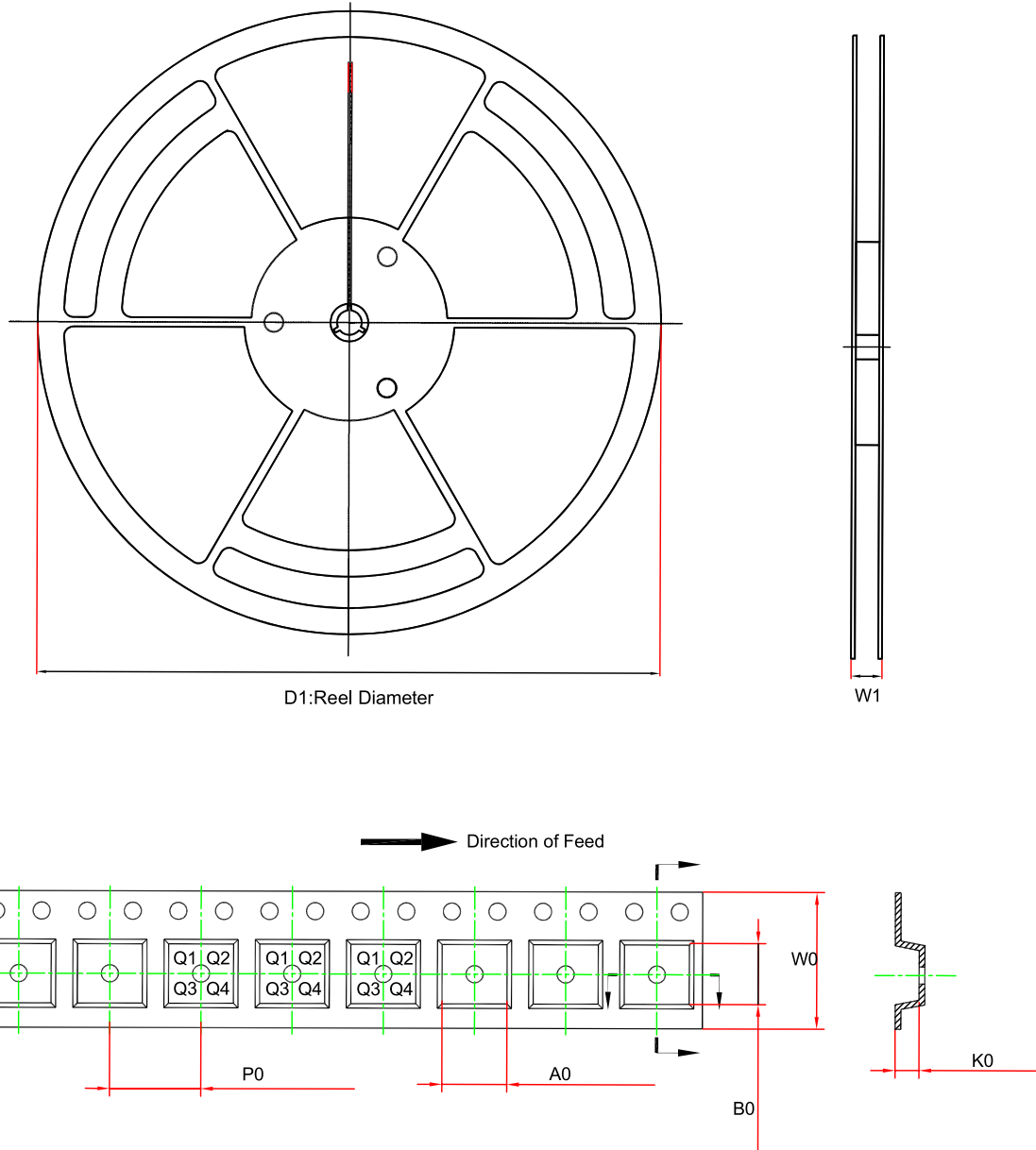
Figure 18. Typical Application Schematic of Adjustable Output

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1- μ F bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize $I \times R$ drop and heat dissipation.

Tape and Reel Information



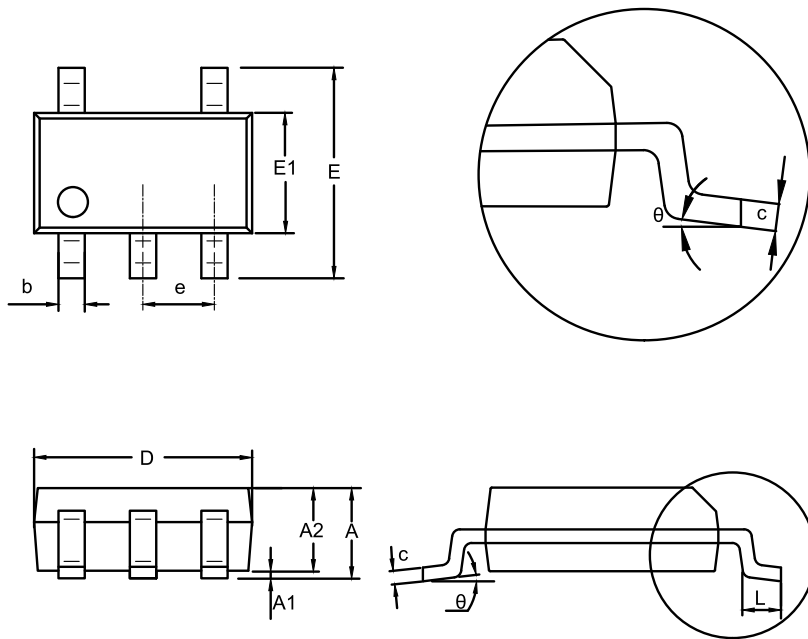
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
LT1761ES5	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3

(1) Output voltage value, xx = 15 to 50 and AD, e.g., 33 means 3.3 V output voltage, and AD means adjustable output.

Package Outline Dimensions

SOT23-5

Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.