SDM011PL03QB

-30V P-Channel MOSFETs

Rev 1.0

Feature

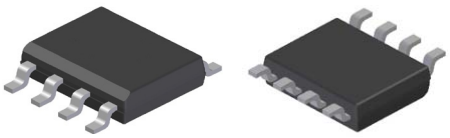
- ✧ Low $R_{DS(ON)}$
- ✧ Low Gate Charge
- ✧ High current Capability
- ✧ Green product RoHS compliant, lead free
- ✧ 100% UIS Tested, 100% Rg Tested

Product Summary

V_{DS}	-30	V
$V_{GS(th)\_Typ}$	-1.5	V
$R_{DS(ON)\_Typ}$ (@ V_{GS} =-10V)	8	mΩ
I_D (at V_{GS} =-10V) (1)	-10	A

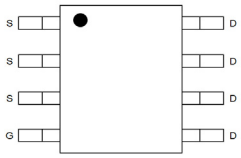
Type	Package	Marking	Outline	Media	Quantity (pcs)
SDM011PL03QB	SOP-8	4407	Tape	13" Reel	4000

SOP-8 Top View SOP-8 Bottom View

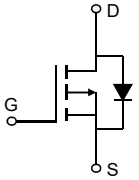


SOP-8

Top View



Pin Assignment



Schematic Diagram

Absolute Maximum Ratings (Rating at T_J=25℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	T_A=25 ℃	I_D	-10	A
	T_A=100 ℃		-6	
Pulsed Drain Current (2)		I_{DM}	-39.5	A
Body-Diode Continuous Current		I_S	-10	A
Avalanche Current (3)		I_{AS}	-25	A
Avalanche Energy (3)		E_{AS}	64	mJ
Power Dissipation (4)	T_A=25 ℃	P_D	2	W
	T_A=100 ℃		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	℃

Electrical Characteristics (Rating at T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
		T_J=55℃	-	-	-5	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS} =±20V	-	-	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=-250μA	-1.1	-1.5	-2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-15A	-	8	11	mΩ
		V_{GS}=-4.5V, I_D=-10A	-	12	17	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-15A	-	8.8	-	S
V_{SD}	Diode Forward Voltage	I_S=-15A, V_{GS}=0V	-	-0.9	-1.2	V
DYNAMIC PARAMETERS (5)						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz	-	1612	-	pF
C_{oss}	Output Capacitance		-	272	-	pF
C_{rss}	Reverse Transfer Capacitance		-	218	-	pF
R_g	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	14	-	Ω
SWITCHING PARAMETERS (5)						
Q_g	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-10A	-	29	-	nC
Q_{gs}	Gate Source Charge		-	15	-	nC
Q_{gd}	Gate Drain Charge		-	5.5	-	nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS}=-10V,V_{DS}=-15V,I_D=-10A,, R_{GEN}=1Ω	-	23	-	ns
t_r	Turn-On Rise Time		-	49	-	ns
$t_{D(off)}$	Turn-Off Delay Time		-	31	-	ns
t_f	Turn-Off Fall Time		-	25	-	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-10A, di/dt=100A/μs	-	27	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-10A, di/dt=100A/μs	-	13	-	nC

Thermal Resistances

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal resistance from junction to case	21	26	℃ /W
$R_{\theta JA}$	Thermal resistance from junction to ambient	42	53	℃ /W

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous depends on the thermal & electro-mechanical application board design.
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
3. This single-pulse measurement was taken under the following condition [L=0.1mH, VGS=-10V, VDS=-15V] while its value is limited by T_{J_Max}=150°C.
4. The power dissipation P_D is based on T_{J_Max}=150℃.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics

Figure 1: Saturation Characteristics

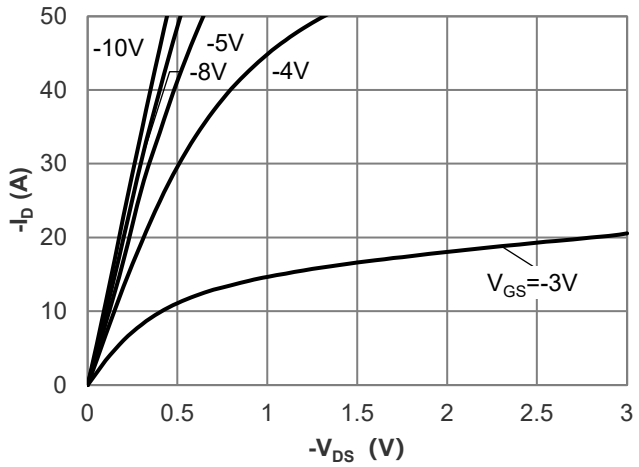


Figure 2: Transfer Characteristics

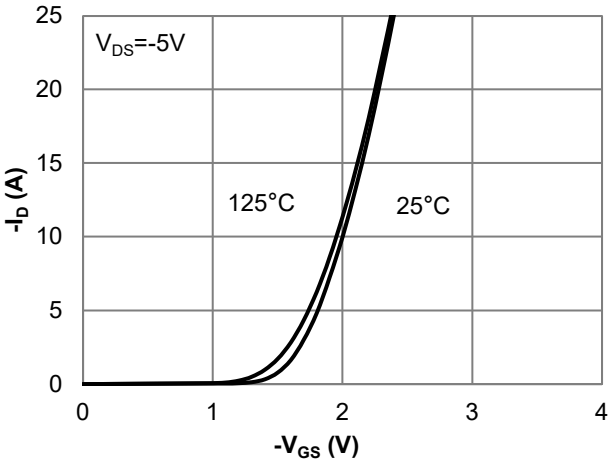


Figure 3: $R_{DS(ON)}$ vs. Drain Current

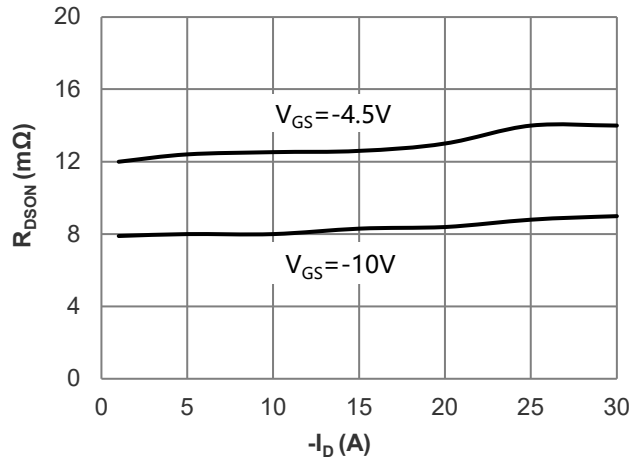


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

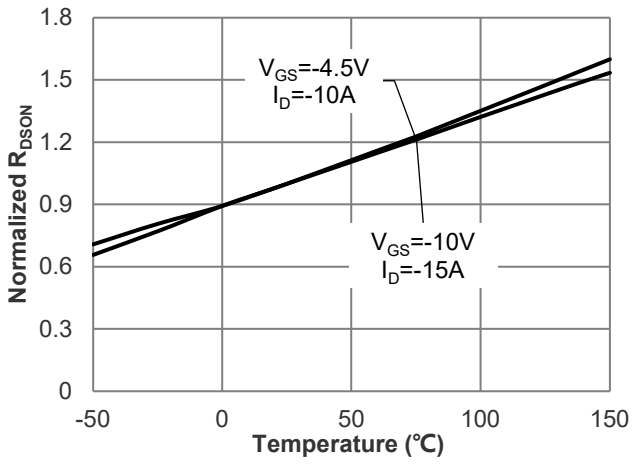


Figure 5: $R_{DS(ON)}$ vs. Gate-Source Voltage

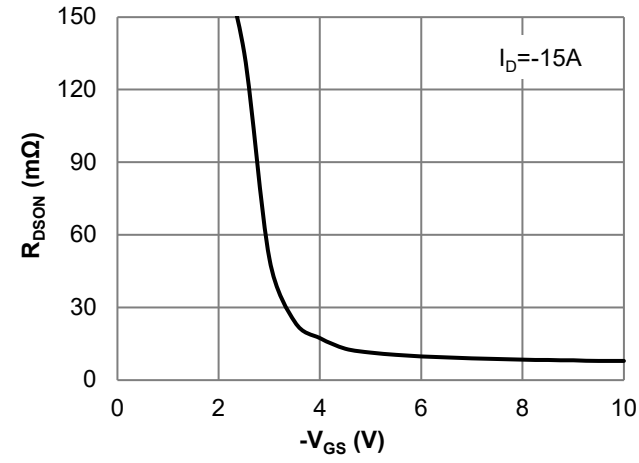
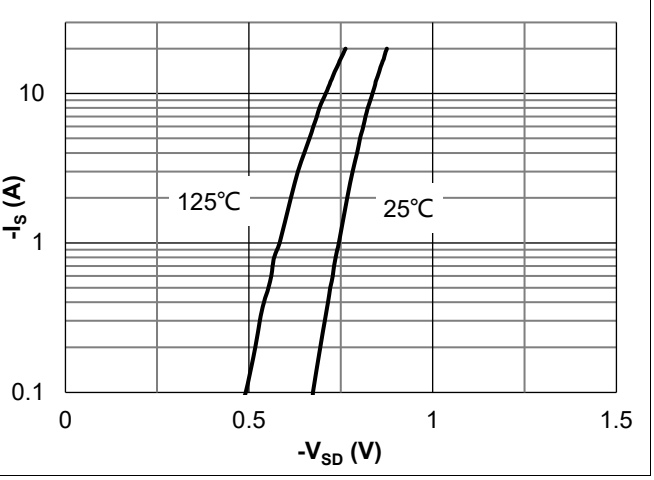


Figure 6: Body-Diode Characteristics



Typical Electrical and Thermal Characteristics

Figure 7: Gate-Charge characteristics

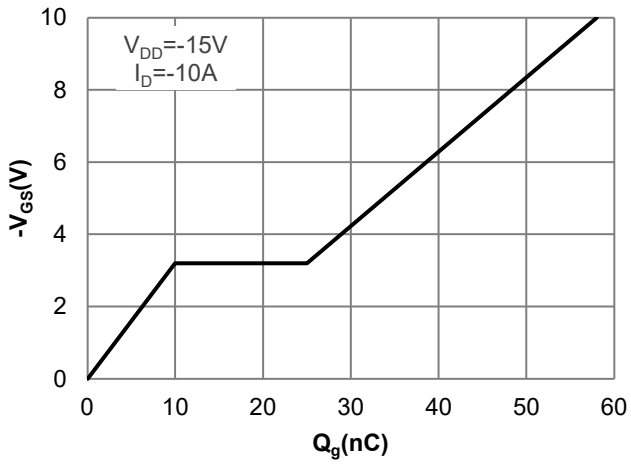


Figure 8: Capacitance characteristics

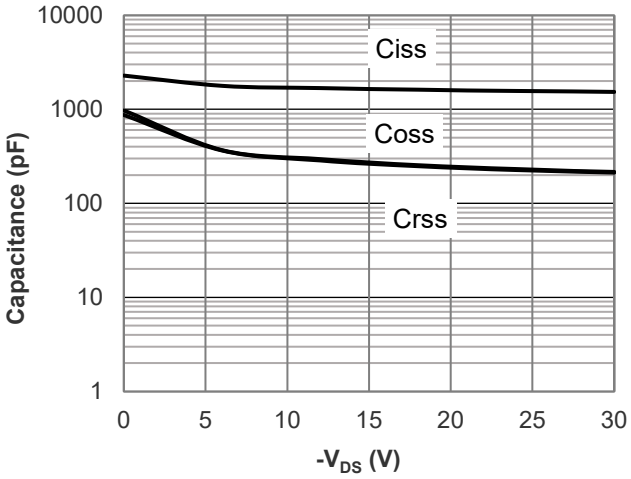


Figure 9: Current De-rating

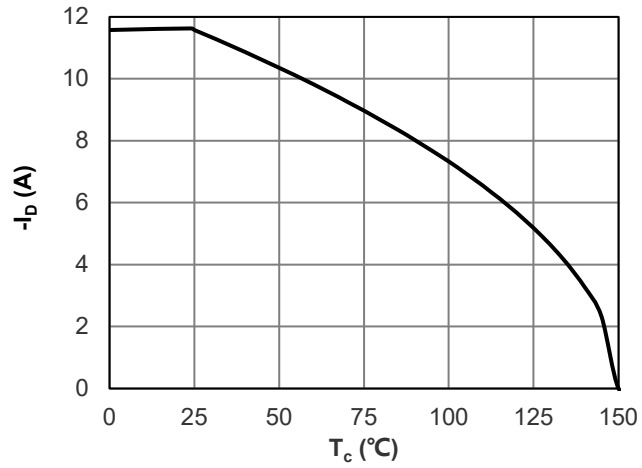


Figure 10: Power De-rating

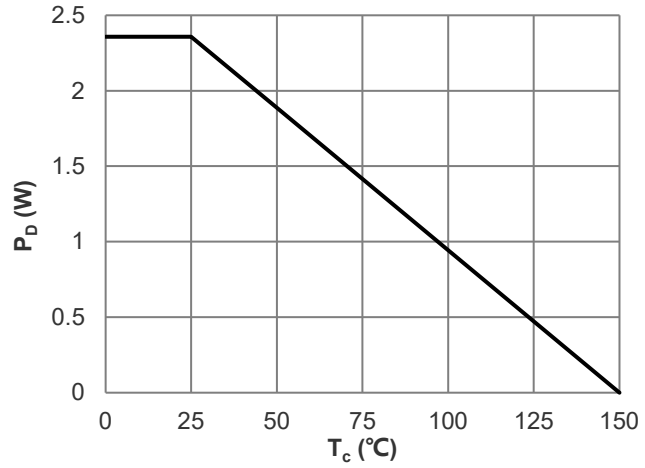


Figure 11: Maximum Safe Operating Area

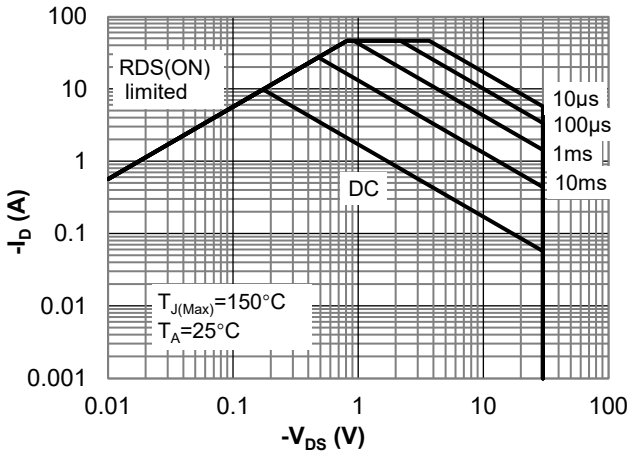
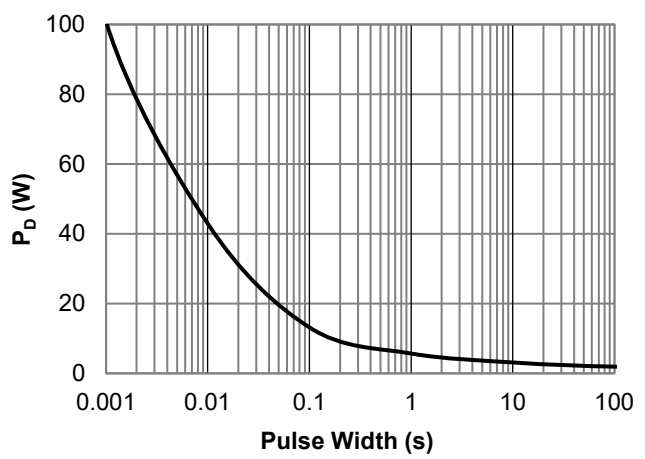
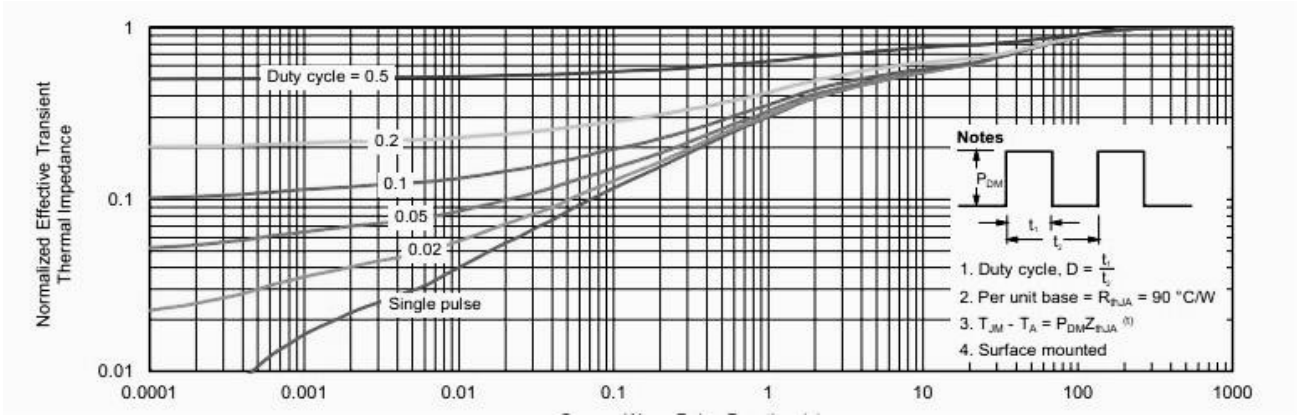


Figure 12: Single Pulse Power Rating, Junction-to-Ambient



Typical Electrical and Thermal Characteristics

Figure 13: Normalized Maximum Transient Thermal Impedance



Test Circuit

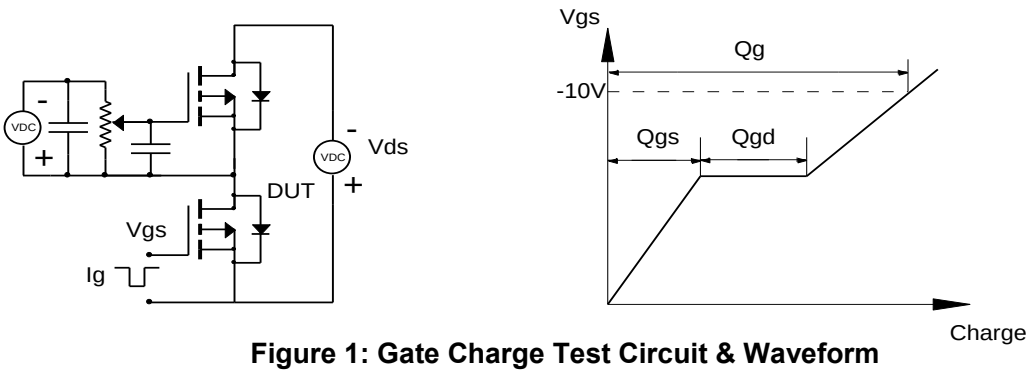


Figure 1: Gate Charge Test Circuit & Waveform

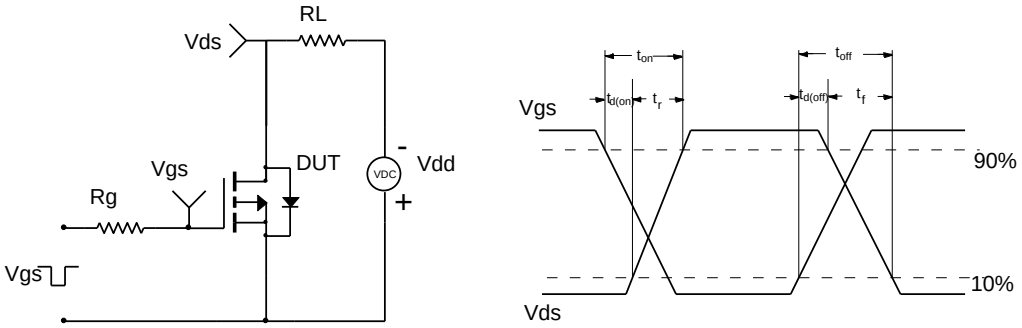


Figure 2: Resistive Switching Test Circuit & Waveform

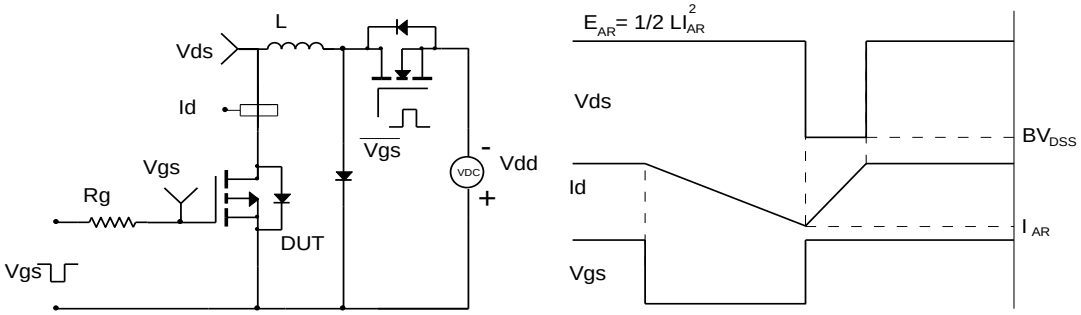


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

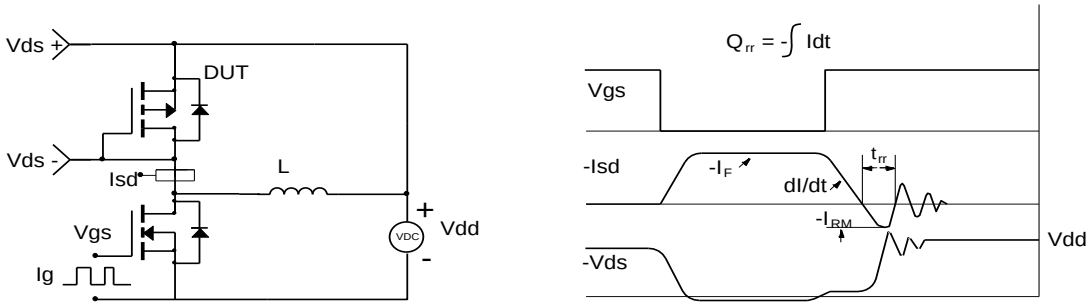
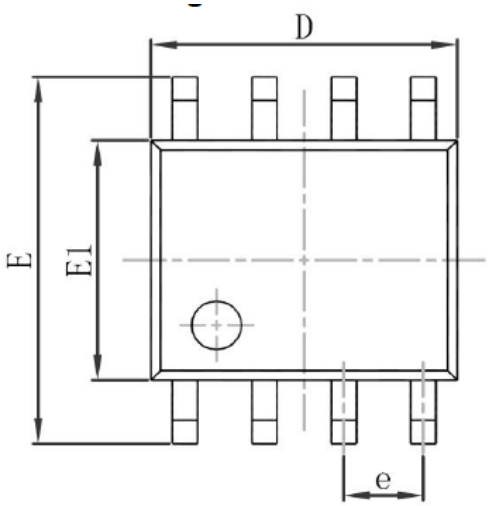
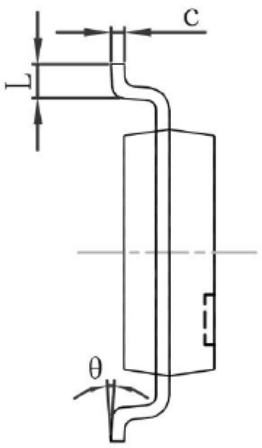


Figure 4: Diode Recovery Test Circuit & Waveform

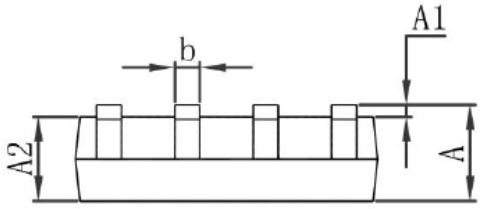
SOP-8 Package Information



TOP VIEW

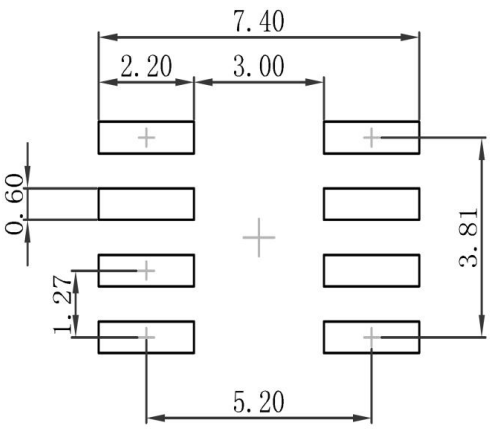


SIDE VIEW



SIDE VIEW

SOP-8 Suggested Pad Layout



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.800	5.000
e	1.270(BSC)	
E	5.800	6.200
E1	3.800	4.000
L	0.400	1.270
θ	0°	8°