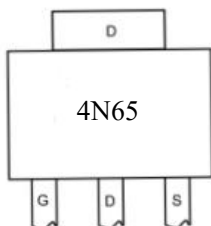




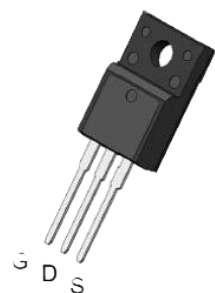
Features ➤ Planar Mosfets ➤ Excellent $R_{DS(on)}$ ➤ Low Gate Charge ➤ High current Capability ➤ Green product RoHS compliant	<i>Bvdss</i>	<i>Rdson</i>	<i>ID</i>
	650V	2.3Ω	4A
	Application ➤ Power factor correction (PFC) ➤ Switching power supply (SMPS) ➤ LED driver		



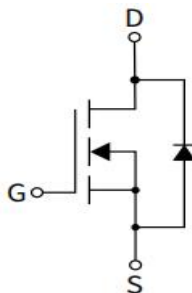
Package



Marking and pin assignment



TO-220F Top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
4N65	HL4N65RF	TO-220F	50

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current ¹	$T_C=25^{\circ}\text{C}$	I_D	4	A
	$T_C=100^{\circ}\text{C}$		2.6	A
Pulsed Drain Current ²		I_{DM}	16	A
Body-Diode Continuous Current		I_S	4	A
Avalanche Current ³		I_{AS}	4.6	A
Single Pulsed Avalanche Energy ³		EAS	84	mJ
Total Power Dissipation ⁴	$T_C = 25^{\circ}\text{C}$	P_D	114	W
	$T_C=100^{\circ}\text{C}$		45	
Operating Junction Temperature Range		T_J	-55 ~ 150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ 150	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	63	$^{\circ}\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	4.2	$^{\circ}\text{C/W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL4N65RF	TO-220F	1	2	3	Tube

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	650	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$	-	-	5	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}$, $V_{DS}=0\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.5	3.4	4.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=2\text{A}$	-	2300	2600	m Ω
Forward Transconductance	g_{fs}	$V_{DS}=5\text{V}$, $I_D=2\text{A}$	-	3	-	S
Gate Resistance	R_g	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	-	1.1	-	Ω
Total Gate Charge	Q_g	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=4\text{A}$	-	17.9	-	nC
Gate Source Charge	Q_{gs}		-	7.5	-	
Gate Drain Charge	Q_{gd}		-	4.3	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{DS}=325\text{V}$, $I_D=4\text{A}$, $R_G=25\Omega$	-	17	-	ns
Rise Time	T_r		-	27	-	
Turn-Off Delay Time	$T_{d(off)}$		-	31	-	
Fall Time	T_f		-	21	-	
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1\text{MHz}$	-	525	-	pF
Output Capacitance	C_{oss}		-	53	-	
Reverse Transfer Capacitance	C_{rss}		-	5.7	-	
Continuous Source Current	I_s	$V_G=V_D=0\text{V}$, Force Current	-	-	-	A
Diode Forward Voltage	V_{SD}	$I_s=2\text{A}$, $V_{GS}=0\text{V}$	-	0.8	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=400\text{V}$, $I_F=4\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	213	-	ns



Reverse Recovery Charge

 Q_{rr}

-

1.5

-

 μC

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous depends on the thermal & Electromechanical application board design.
2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
3. This single-pulse measurement was taken under the following condition [$L=10\text{mH}$, $V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$] while its value is limited by $T_{J_Max}=150^\circ\text{C}$.
4. The power dissipation P_D is based on $T_{J_Max}=150^\circ\text{C}$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

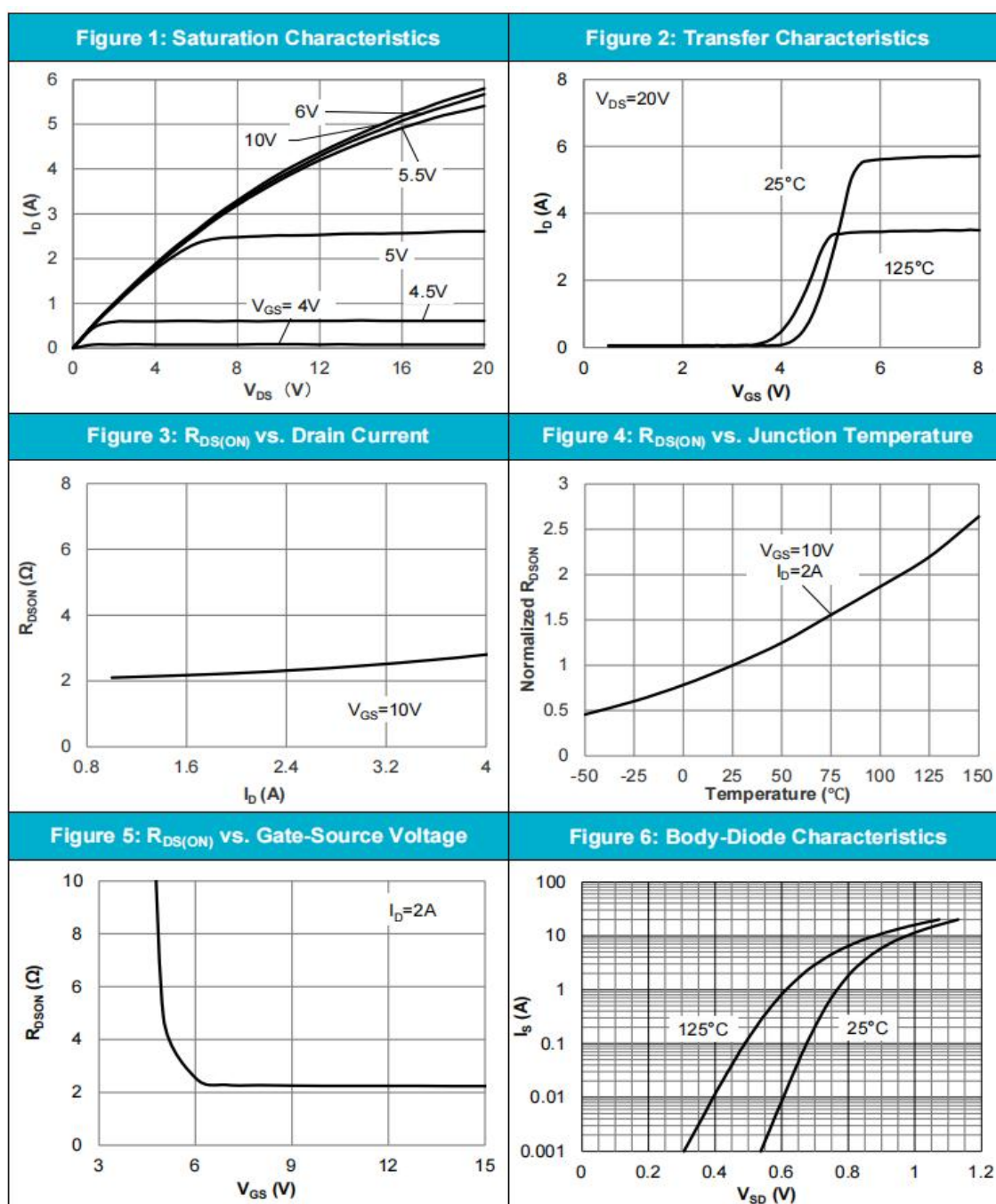




Figure 7: Gate-Charge characteristics

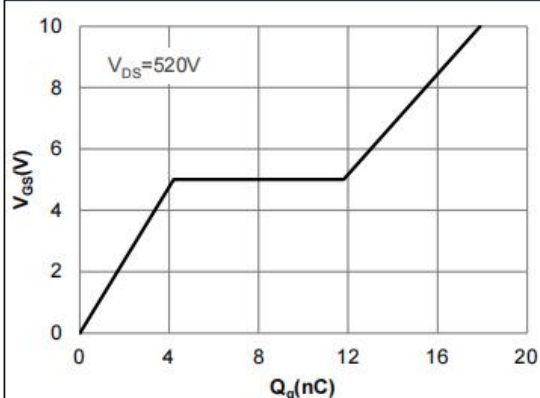


Figure 8: Capacitance characteristics

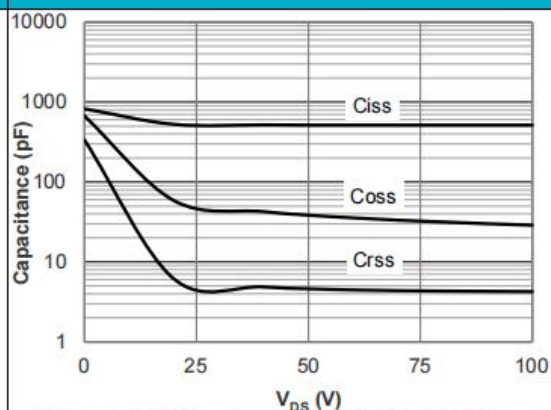


Figure 9: Current De-rating

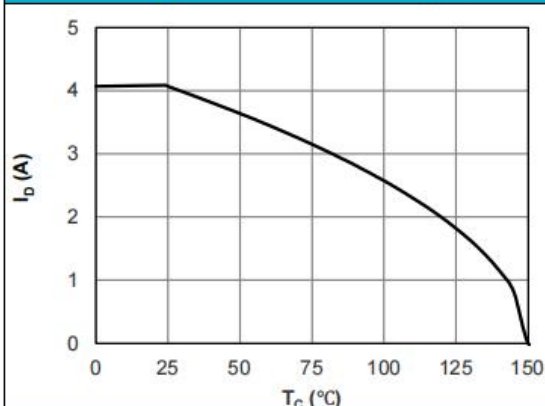


Figure 10: Maximum Safe Operating Area (TO-220C/TO-263)

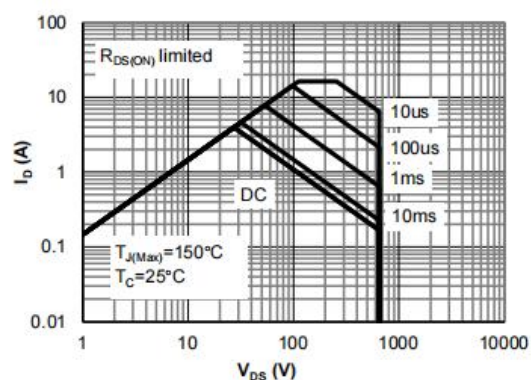


Figure 11: Maximum Safe Operating Area (TO-220F)

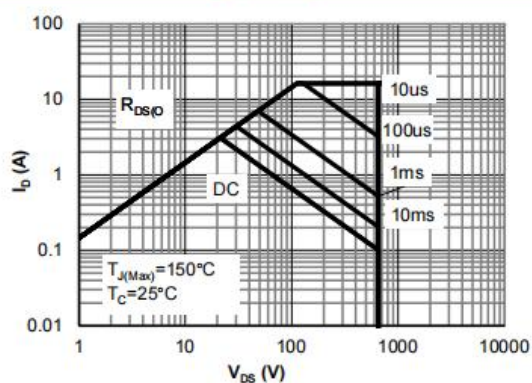


Figure 12: Normalized Maximum Transient Thermal Impedance (TO-220C/TO-263)

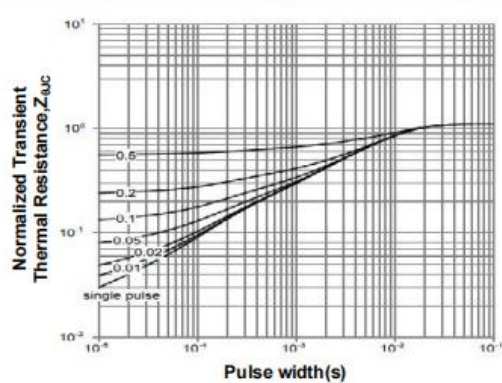
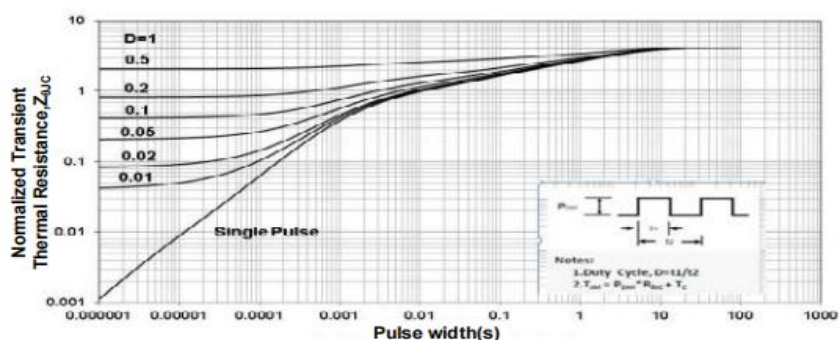


Figure 13: Normalized Maximum Transient Thermal Impedance (TO-220F)





Test Circuit and Waveform

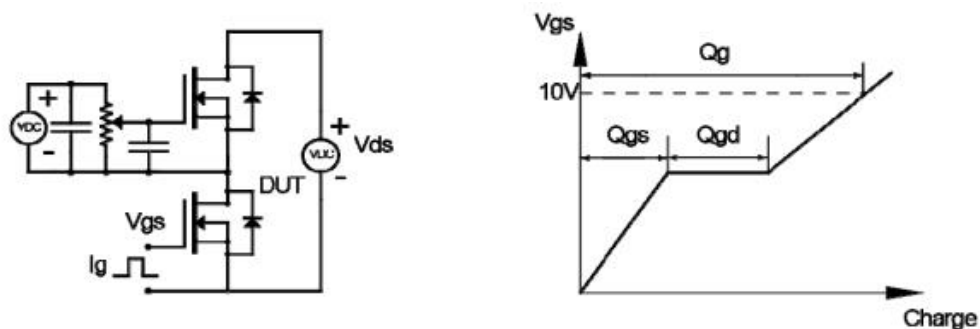


Figure1: Gate Charge Test Circuit & Waveforms

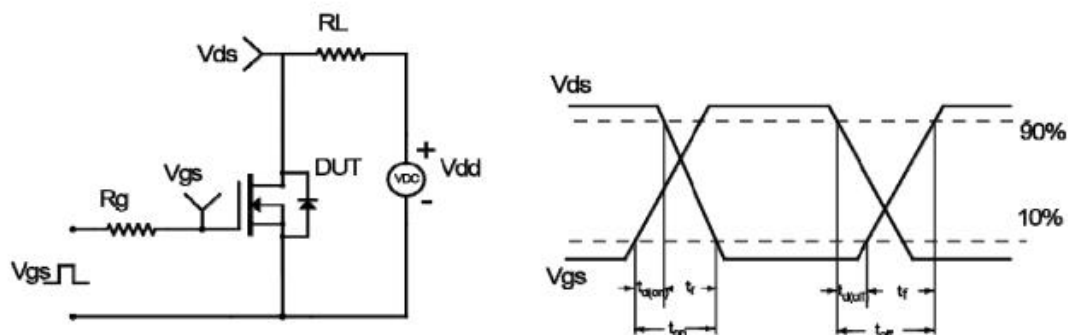


Figure2: Resistive Switching Test Circuit & Waveforms

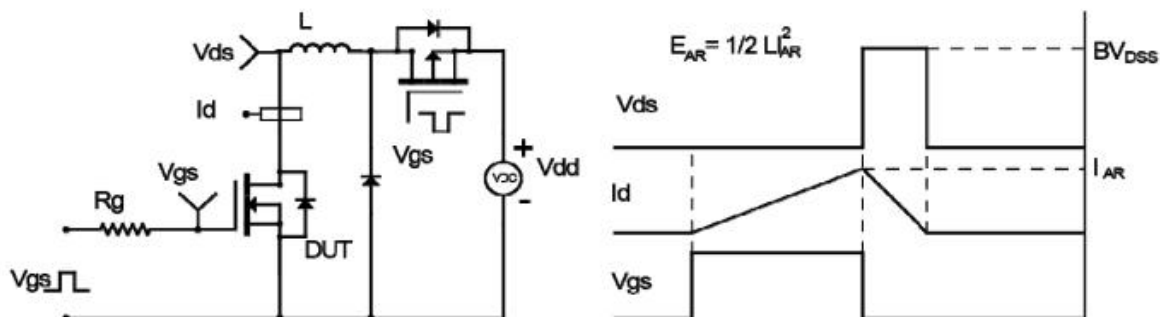


Figure3: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

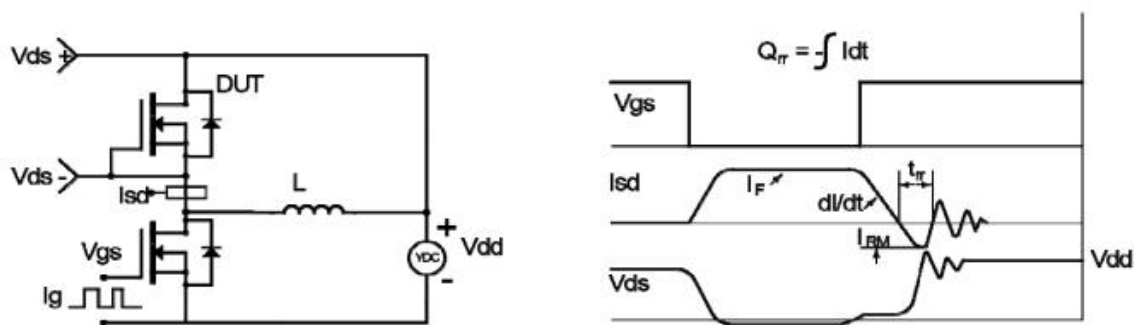
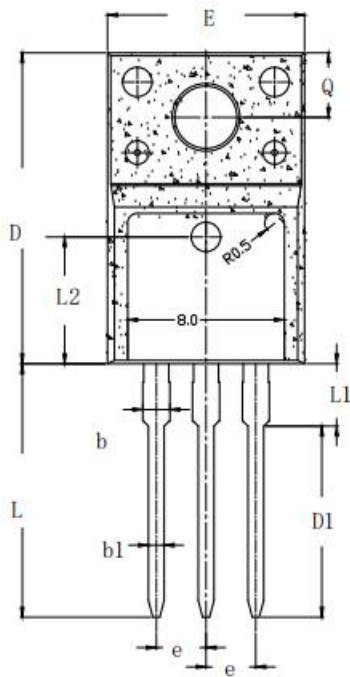


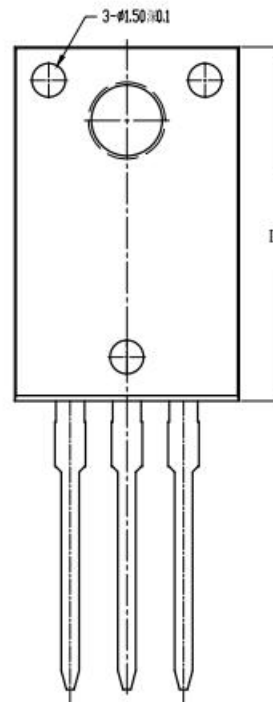
Figure4: Diode Recovery Test Circuit & Waveforms



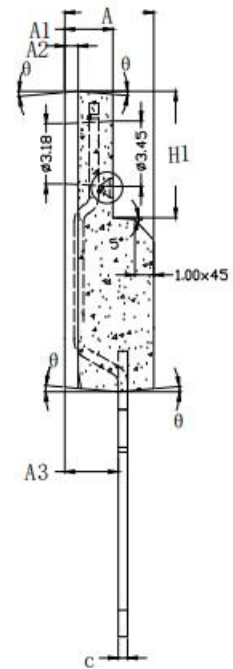
Package Dimensions TO-220F



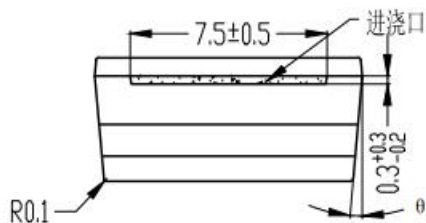
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	TYP.	MAX
A	4.60	4.70	4.80
A1	2.39	2.54	2.69
A2	0.60	0.70	0.80
A3	2.81	2.82	2.83
b	1.61	1.62	1.63
b1	-	0.80	-
c	-	0.50	-
D	15.72	15.87	16.02
D1	-	9.75	-
E	9.91	10.06	10.21
e	2.54 BSC		
H1	6.67	6.68	6.69
L	12.90	12.93	12.96
L1	-	3.18	-
L2	6.47 REF		
Q	-	3.30	-
θ1	1°	3°	5°



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