# *Single and Dual-Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier*

## GENERAL DESCRIPTION

The HT8623 is an integrated, single- or dual-supply instrumentation amplifier that delivers rail-to-rail output swing using supply voltages from 3 V to 12 V. The HT8623 offers superior user flexibility by allowing single gain set resistor programming and by conforming to the 8-lead industry standard pinout configuration. With no external resistor, the HT8623 is configured for unity gain (G = 1), and with an external resistor, the HT8623 can be programmed for gains of up to 1000.

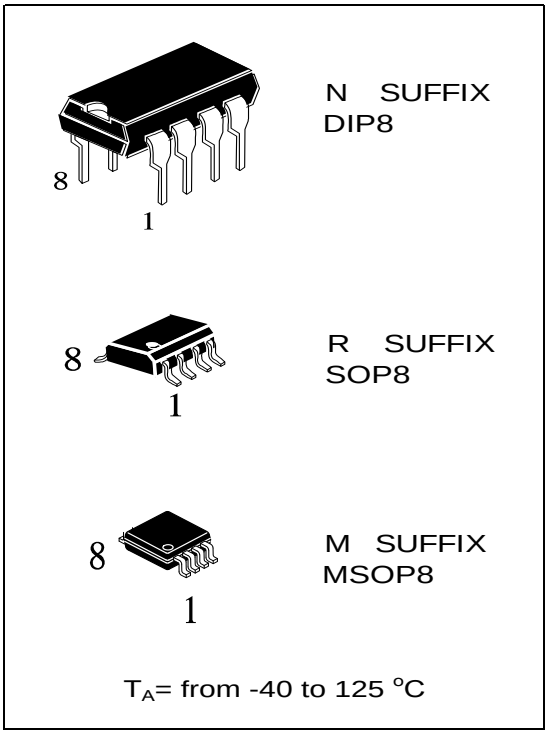
The superior accuracy of the HT8623 is the result of
increasing ac common-mode rejection ratio (CMRR)
coincident with increasing gain; line noise harmonics are rejected due to constant CMRR up to 200 Hz. The HT8623 has a wide input common-mode range and amplifies signals with common- mode voltages as low as 150 mV below ground. The HT8623 maintains superior performance with
dual and single polarity power supplies.

## FEATURES

Easy to use
Rail-to-rail output swing
Input voltage range extends 150 mV below ground
(single supply)
Low power, 550 μA maximum supply current
Gain set with one external resistor
Gain range: 1 to 1000
High accuracy dc performance
0.10% gain accuracy (G = 1)
0.35% gain accuracy (G > 1)
Noise: 35 nV/√Hz RTI noise at 1 kHz
Excellent dynamic specifications
800 kHz bandwidth (G = 1)
20 μs settling time to 0.01% (G = 10)

## APPLICATIONS

Low power medical instrumentation
Transducer interfaces
Thermocouple amplifiers
Industrial process controls
Difference amplifiers
Low power data acquisition




## FUNCTIONAL BLOCK DIAGRAM

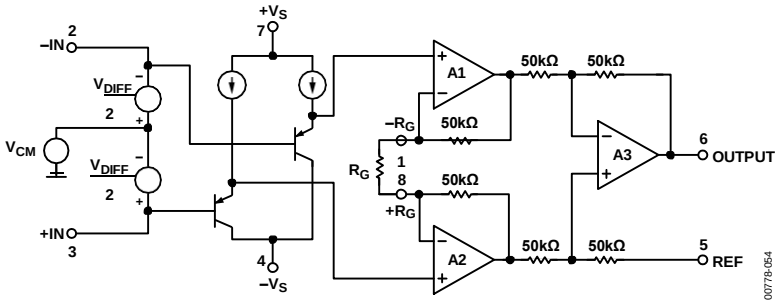



*Figure 1.*

## SINGLE SUPPLY

Typical at 25 ℃, single supply, $+V_S$ = 5 V, $-V_S$ = 0 V, and $R_L$ = 10 kΩ, unless otherwise noted.

**Table 2.**

| Parameter | Test Conditions/ Comments | HT8623ARZ | | | HT8623ARMZ | | | HT8623BRZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| GAIN | G=1+(100k/$R_G$) | | | | | | | | | | |
| Gain Range | | 1 | | 1000 | 1 | | 1000 | 1 | | 1000 | |
| Gain Error[1] | G1 $V_{OUT}$ = 0.05 V to 3.5 V<br>G > 1 $V_{OUT}$ = 0.05 V to 4.5 V | | | | | | | | | | |
| G = 1 | | | 0.03 | 0.10 | | 0.03 | 0.10 | | 0.03 | 0.05 | % |
| G = 10 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| G = 100 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| G = 1000 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| Nonlinearity | G1 $V_{OUT}$ = 0.05 V to 3.5 V<br>G > 1 $V_{OUT}$ = 0.05 V to 4.5 V | | | | | | | | | | |
| G = 1 to 1000 | | | 50 | | | 50 | | | 50 | | ppm |
| Gain vs. Temperature | | | | | | | | | | | |
| G = 1 | | | 5 | 10 | | 5 | 10 | | 5 | 10 | ppm/°C |
| G > 1[1] | | | 50 | | | 50 | | | 50 | | ppm/°C |
| VOLTAGE OFFSET | Total RTI error = $V_{OSI}$ + $V_{OSO}$/G | | | | | | | | | | |
| Input Offset, $V_{OSI}$ | | | 25 | 200 | | 200 | 500 | | 25 | 100 | µV |
| Over Temperature | | | | 350 | | | 650 | | | 160 | µV |
| Average Temperature Coefficient (Tempco) | | | 0.1 | 2 | | 0.1 | 2 | | 0.1 | 1 | µV/°C |
| Output Offset, $V_{OSO}$ | | | 200 | 1000 | | 500 | 2000 | | 200 | 500 | µV |
| Over Temperature | | | | 1500 | | | 2600 | | | 1100 | µV |
| Average Tempco | | | 2.5 | 10 | | 2.5 | 10 | | 2.5 | 10 | µV/°C |
| Offset Referred to the Input vs. Supply (PSR) | | | | | | | | | | | |
| G = 1 | | 80 | 100 | | 80 | 100 | | 80 | 100 | | dB |
| G = 10 | | 100 | 120 | | 100 | 120 | | 100 | 120 | | dB |
| G = 100 | | 120 | 140 | | 120 | 140 | | 120 | 140 | | dB |
| G = 1000 | | 120 | 140 | | 120 | 140 | | 120 | 140 | | dB |
| INPUT CURRENT | | | | | | | | | | | |
| Input Bias Current | | | 17 | 25 | | 17 | 25 | | 17 | 25 | nA |
| Over Temperature | | | | 27.5 | | | 27.5 | | | 27.5 | nA |
| Average Tempco | | | 25 | | | 25 | | | 25 | | pA/°C |
| Input Offset Current | | | 0.25 | 2 | | 0.25 | 2 | | 0.25 | 2 | nA |
| Over Temperature | | | | 2.5 | | | 2.5 | | | 2.5 | nA |
| Average Tempco | | | 5 | | | 5 | | | 5 | | pA/°C |
| INPUT | | | | | | | | | | | |
| Input Impedance | | | | | | | | | | | |
| Differential | | | 2\|\|2 | | | 2\|\|2 | | | 2\|\|2 | | GΩ\|\|pF |
| Common-Mode | | | 2\|\|2 | | | 2\|\|2 | | | 2\|\|2 | | GΩ\|\|pF |
| Input Voltage Range[2] | $V_S$ = 3 V to 12 V | ($-V_S$) − 0.15 | | ($+V_S$) − 1.5 | ($-V_S$) − 0.15 | | ($+V_S$) − 1.5 | ($-V_S$) − 0.15 | | ($+V_S$) − 1.5 | V |

| Parameter | Test Conditions/ Comments | HT8623ARZ | | | HT8623ARMZ | | | HT8623BRZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance | | | | | | | | | | | |
| G = 1 | $V_{CM}$ = 0 V to 3 V | 70 | 80 | | 70 | 80 | | 77 | 86 | | dB |
| G = 10 | $V_{CM}$ = 0 V to 3 V | 90 | 100 | | 90 | 100 | | 94 | 100 | | dB |
| G = 100 | $V_{CM}$ = 0 V to 3 V | 105 | 110 | | 105 | 110 | | 105 | 110 | | dB |
| G = 1000 | $V_{CM}$ = 0 V to 3 V | 105 | 110 | | 105 | 110 | | 105 | 110 | | dB |
| OUTPUT | | | | | | | | | | | |
| Output Swing | $R_L$ = 10 kΩ | 0.01 | | $(+V_S)$ − 0.5 | 0.01 | | $(+V_S)$ − 0.5 | 0.01 | | $(+V_S)$ − 0.5 | V |
| | $R_L$ = 100 kΩ | 0.01 | | $(+V_S)$ − 0.15 | 0.01 | | $(+V_S)$ − 0.15 | 0.01 | | $(+V_S)$ − 0.15 | V |
| DYNAMIC RESPONSE | | | | | | | | | | | |
| Small Signal −3 dB BW | | | | | | | | | | | |
| G = 1 | | | 800 | | | 800 | | | 800 | | kHz |
| G = 10 | | | 100 | | | 100 | | | 100 | | kHz |
| G = 100 | | | 10 | | | 10 | | | 10 | | kHz |
| G = 1000 | | | 2 | | | 2 | | | 2 | | kHz |
| Slew Rate | | | 0.3 | | | 0.3 | | | 0.3 | | V/µs |
| Settling Time to 0.01% | $V_S$ = 5 V | | | | | | | | | | |
| G = 1 | Step size: 3.5 V | | 30 | | | 30 | | | 30 | | µs |
| G = 10 | Step size: 4 V, $V_{CM}$ = 1.8 V | | 20 | | | 20 | | | 20 | | µs |

[1] Does not include effects of external resistor, $R_G$.
[2] One input grounded. G = 1.

## DUAL SUPPLIES

Typical at 25 ℃ dual supply, $V_S$ = ±5 V, and $R_L$ = 10 kΩ, unless otherwise noted.

**Table 3.**

| Parameter | Test Conditions/ Comments | HT8623ARZ | | | HT8623ARMZ | | | HT8623BRZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| GAIN | G = 1 + (100 k/$R_G$) | | | | | | | | | | |
| Gain Range | | 1 | | 1000 | 1 | | 1000 | 1 | | 1000 | |
| Gain Error[1] | G1 $V_{OUT}$ = −4.8 V to +3.5 V<br>G > 1 $V_{OUT}$ = 0.05 V to 4.5 V | | | | | | | | | | |
| G = 1 | | | 0.03 | 0.10 | | 0.03 | 0.10 | | 0.03 | 0.05 | % |
| G = 10 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| G = 100 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| G = 1000 | | | 0.10 | 0.35 | | 0.10 | 0.35 | | 0.10 | 0.35 | % |
| Nonlinearity | G1 $V_{OUT}$ = −4.8 V to +3.5 V<br>G > 1 $V_{OUT}$ = −4.8 V to +4.5 V | | | | | | | | | | |
| G = 1 to 1000 | | | 50 | | | 50 | | | 50 | | ppm |
| Gain vs. Temperature | | | | | | | | | | | |
| G = 1 | | | 5 | 10 | | 5 | 10 | | 5 | 10 | ppm/°C |
| G > 1[1] | | | 50 | | | 50 | | | 50 | | ppm/°C |
| VOLTAGE OFFSET | Total RTI error = $V_{OSI}$ + $V_{OSO}$/G | | | | | | | | | | |
| Input Offset, $V_{OSI}$ | | | 25 | 200 | | 200 | 500 | | 25 | 100 | µV |
| Over Temperature | | | | 350 | | | 650 | | | 160 | µV |
| Average Tempco | | | 0.1 | 2 | | 0.1 | 2 | | 0.1 | 1 | µV/°C |
| Output Offset, $V_{OSO}$ | | | 200 | 1000 | | 500 | 2000 | | 200 | 500 | µV |
| Over Temperature | | | | 1500 | | | 2600 | | | 1100 | µV |
| Average Tempco | | | 2.5 | 10 | | 2.5 | 10 | | 2.5 | 10 | µV/°C |
| Offset Referred to the Input vs. Supply (PSR) | | | | | | | | | | | |
| G = 1 | | 80 | 100 | | 80 | 100 | | 80 | 100 | | dB |
| G = 10 | | 100 | 120 | | 100 | 120 | | 100 | 120 | | dB |
| G = 100 | | 120 | 140 | | 120 | 140 | | 120 | 140 | | dB |
| G = 1000 | | 120 | 140 | | 120 | 140 | | 120 | 140 | | dB |
| INPUT CURRENT | | | | | | | | | | | |
| Input Bias Current | | | 17 | 25 | | 17 | 25 | | 17 | 25 | nA |
| Over Temperature | | | | 27.5 | | | 27.5 | | | 27.5 | nA |
| Average Tempco | | | 25 | | | 25 | | | 25 | | pA/°C |
| Input Offset Current | | | 0.25 | 2 | | 0.25 | 2 | | 0.25 | 2 | nA |
| Over Temperature | | | | 2.5 | | | 2.5 | | | 2.5 | nA |
| Average Tempco | | | 5 | | | 5 | | | 5 | | pA/°C |
| INPUT | | | | | | | | | | | |
| Input Impedance | | | | | | | | | | | |
| Differential | | | 2\|\|2 | | | 2\|\|2 | | | 2\|\|2 | | GΩ\|\|pF |
| Common-Mode | | | 2\|\|2 | | | 2\|\|2 | | | 2\|\|2 | | GΩ\|\|pF |
| Input Voltage Range[2] | $V_S$ = +2.5 V to ±6 V | (−$V_S$) − 0.15 | | (+$V_S$) − 1.5 | (−$V_S$) − 0.15 | | (+$V_S$) − 1.5 | (−$V_S$) − 0.15 | | (+$V_S$) − 1.5 | V |

| Parameter | Test Conditions/ Comments | HT8623ARZ | | | HT8623ARMZ | | | HT8623BRZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Common-Mode Rejection at 60 Hz with 1 kΩ Source Imbalance | | | | | | | | | | | |
| G = 1 | $V_{CM}$ = +3.5 V to −5.15 V | 70 | 80 | | 70 | 80 | | 77 | 86 | | dB |
| G = 10 | $V_{CM}$ = +3.5 V to −5.15 V | 90 | 100 | | 90 | 100 | | 94 | 100 | | dB |
| G = 100 | $V_{CM}$ = +3.5 V to −5.15 V | 105 | 110 | | 105 | 110 | | 105 | 110 | | dB |
| G = 1000 | $V_{CM}$ = +3.5 V to −5.15 V | 105 | 110 | | 105 | 110 | | 105 | 110 | | dB |
| OUTPUT | | | | | | | | | | | |
| Output Swing | $R_L$ = 10 kΩ, $V_S$ = ±5 V | (−$V_S$) + 0.2 | | (+$V_S$) − 0.5 | (−$V_S$) + 0.2 | | (+$V_S$) − 0.5 | (−$V_S$) + 0.2 | | (+$V_S$) − 0.5 | V |
| | $R_L$ = 100 kΩ | (−$V_S$) + 0.05 | | (+$V_S$) − 0.15 | (−$V_S$) + 0.05 | | (+$V_S$) − 0.15 | (−$V_S$) + 0.05 | | (+$V_S$) − 0.15 | V |
| DYNAMIC RESPONSE | | | | | | | | | | | |
| Small Signal −3 dB Bandwidth | | | | | | | | | | | |
| G = 1 | | | 800 | | | 800 | | | 800 | | kHz |
| G = 10 | | | 100 | | | 100 | | | 100 | | kHz |
| G = 100 | | | 10 | | | 10 | | | 10 | | kHz |
| G = 1000 | | | 2 | | | 2 | | | 2 | | kHz |
| Slew Rate | | | 0.3 | | | 0.3 | | | 0.3 | | V/µs |
| Settling Time to 0.01% | $V_S$ = ±5 V, 5 V step | | | | | | | | | | |
| G = 1 | | | 30 | | | 30 | | | 30 | | µs |
| G = 10 | | | 20 | | | 20 | | | 20 | | µs |

[1] Does not include effects of external resistor, $R_G$.

[2] One input grounded. G = 1.

## SPECIFICATIONS COMMON TO DUAL AND SINGLE SUPPLIES

**Table 4.**

| Parameter | Test Conditions/ Comments | HT8623ARZ | | | HT8623ARMZ | | | HT8623BRZ | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| NOISE | | | | | | | | | | | |
| Voltage Noise, 1 kHz | Total RTI noise = $\sqrt{(e_{ni})^2 + (2e_{no}/G)^2}$ | | | | | | | | | | |
| Input, Voltage Noise, $e_{ni}$ | | | 35 | | | 35 | | | 35 | | nV/√Hz |
| Output, Voltage Noise, $e_{no}$ | | | 50 | | | 50 | | | 50 | | nV/√Hz |
| RTI, 0.1 Hz to 10 Hz | | | | | | | | | | | |
| G = 1 | | | 3.0 | | | 3.0 | | | 3.0 | | μV p-p |
| G = 1000 | | | 1.5 | | | 1.5 | | | 1.5 | | μV p-p |
| Current Noise | f = 1 kHz | | 100 | | | 100 | | | 100 | | fA/√Hz |
| 0.1 Hz to 10 Hz | | | 1.5 | | | 1.5 | | | 1.5 | | pA p-p |
| REFERENCE INPUT | | | | | | | | | | | |
| $R_{IN}$ | | | 100 ± 20% | | | 100 ± 20% | | | 100 ± 20% | | kΩ |
| $I_{IN}$ | $V_{IN}$+, $V_{REF}$ = 0 V | | 50 | 60 | | 50 | 60 | | 50 | 60 | μA |
| Voltage Range | | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | V |
| Gain to Output | | | 1 ± 0.0002 | | | 1 ± 0.0002 | | | 1 ± 0.0002 | | V |
| POWER SUPPLY | | | | | | | | | | | |
| Operating Range | Dual supply | ±2.5 | | ±6 | ±2.5 | | ±6 | ±2.5 | | ±6 | V |
| | Single supply | 2.7 | | 12 | 2.7 | | 12 | 2.7 | | 12 | V |
| Quiescent Current | Dual supply | | 375 | 550 | | 375 | 550 | | 375 | 550 | μA |
| | Single supply | | 305 | 480 | | 305 | 480 | | 305 | 480 | μA |
| Over Temperature | | | | 625 | | | 625 | | | 625 | μA |
| TEMPERATURE RANGE | | | | | | | | | | | |
| For Specified Performance | | −40 | | +125 | −40 | | +125 | −40 | | +125 | °C |

## ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 12 V |
| Internal Power Dissipation[1] | 650 mW |
| Differential Input Voltage | ±6 V |
| Output Short-Circuit Duration | Indefinite |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +125°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Specification is for device in free air:
8-Lead PDIP Package: $\theta_{JA}$ = 95°C/W
8-Lead SOIC Package: $\theta_{JA}$ = 155°C/W
8-Lead MSOP Package: $\theta_{JA}$ = 200°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

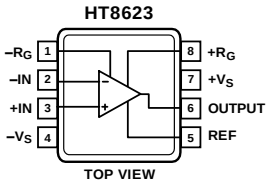



**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $-R_G$ | Inverting Terminal of External Gain-Setting Resistor, $R_G$. |
| 2 | −IN | Inverting In-Amp Input. |
| 3 | +IN | Noninverting In-Amp Input. |
| 4 | $-V_S$ | Negative Supply Terminal. |
| 5 | REF | In-Amp Output Reference Input. The voltage input establishes the common-mode voltage of the output. |
| 6 | OUTPUT | In-Amp Output. |
| 7 | $+V_S$ | Positive Supply Terminal. |
| 8 | $+R_G$ | Noninverting Terminal of External Gain Setting Resistor, $R_G$. |

# TYPICAL PERFORMANCE CHARACTERISTICS

At 25 ℃, $V_S$ = ±5 V, and $R_L$ = 10 kΩ, unless otherwise noted.

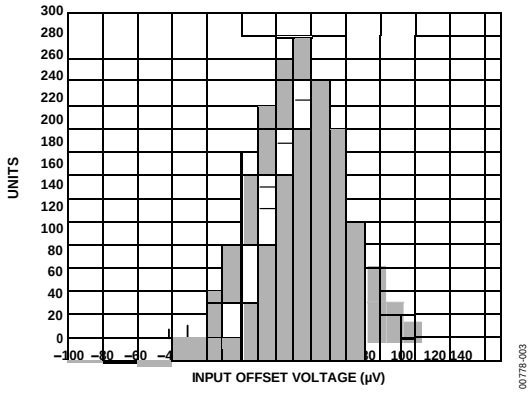



*Figure 3. Typical Distribution of Input Offset Voltage, N-8 and R-8 Package Options*

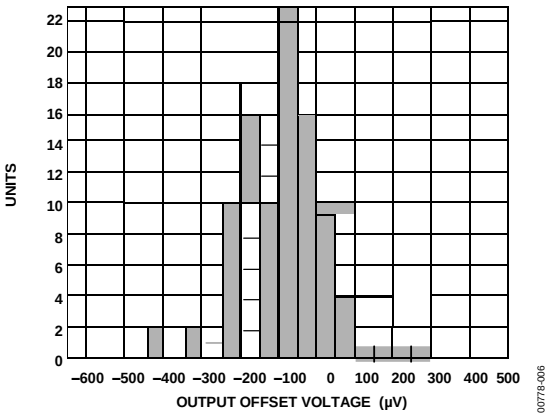



*Figure 6. Typical Distribution of Output Offset Voltage, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{REF}$ = −0.125 V, N-8 and R-8 Package Options*

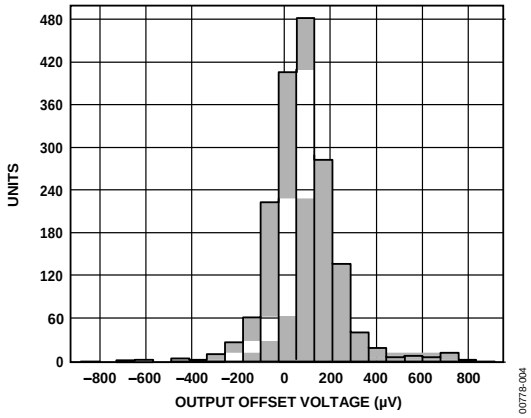



*Figure 4. Typical Distribution of Output Offset Voltage, N-8 and R-8 Package Options*

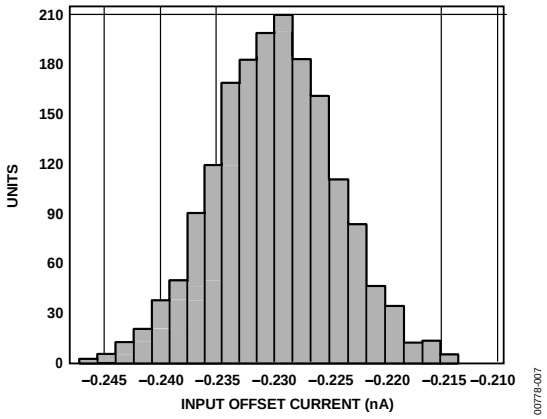



*Figure 7. Typical Distribution for Input Offset Current, N-8 and R-8 Package Options*

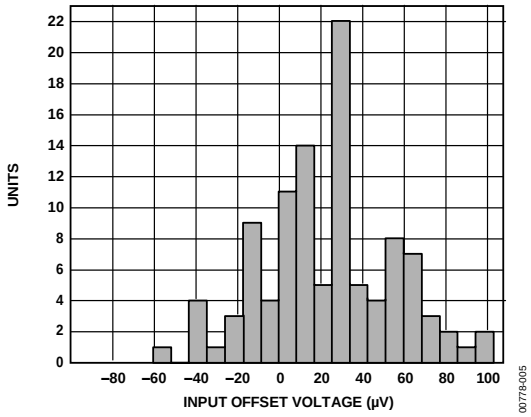



*Figure 5. Typical Distribution of Input Offset Voltage, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{REF}$ = −0.125 V, N-8 and R-8 Package Options*

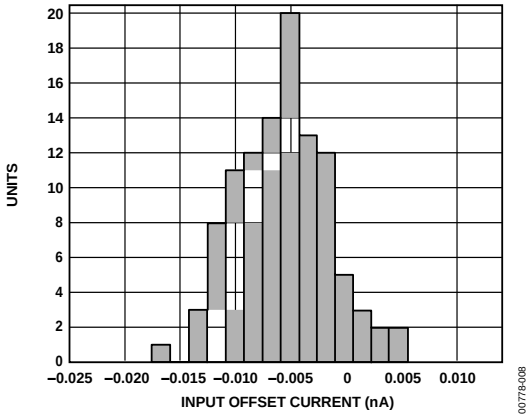



*Figure 8. Typical Distribution for Input Offset Current, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{REF}$ = −0.125 V, N-8 and R-8 Package Options*

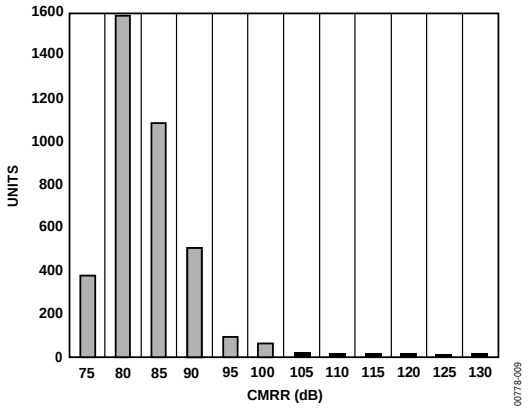



Figure 9. Typical Distribution for CMRR (G = 1)

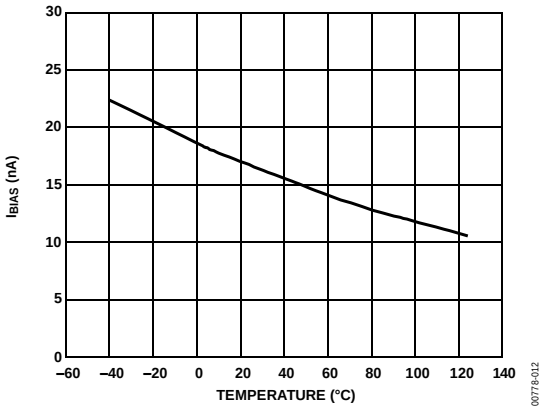



Figure 12. $I_{BIAS}$ vs. Temperature

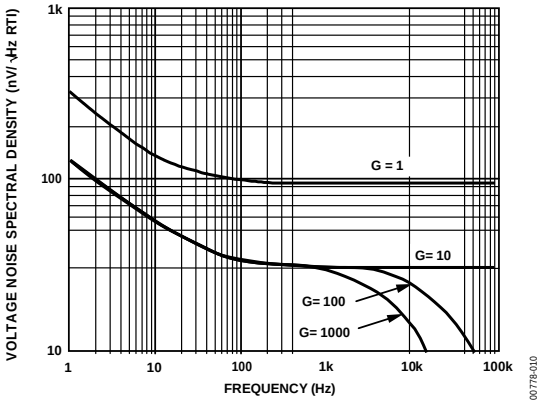



Figure 10. Voltage Noise Spectral Density vs. Frequency

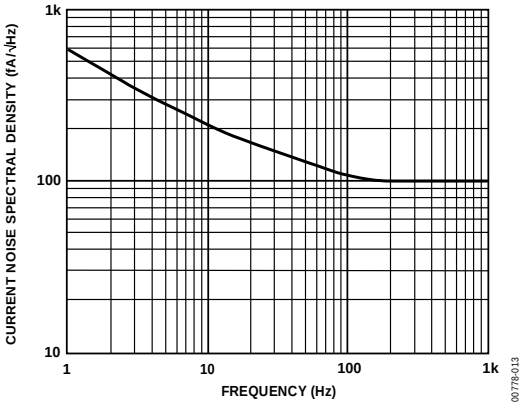



Figure 13. Current Noise Spectral Density vs. Frequency

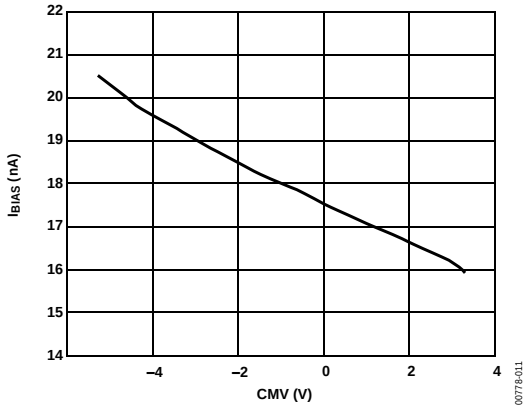



Figure 11. $I_{BIAS}$ vs. CMV

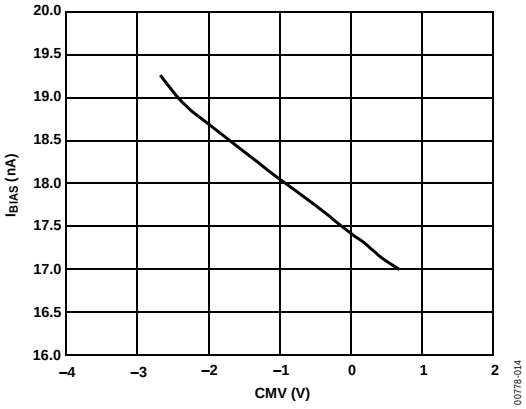



Figure 14. $I_{BIAS}$ vs. CMV, $V_S$ = ±2.5 V

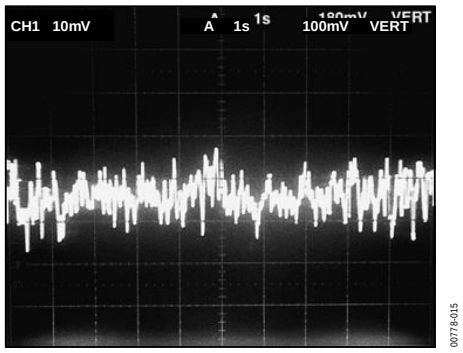



Figure 15. 0.1 Hz to 10 Hz Current Noise (0.71 pA/DIV)

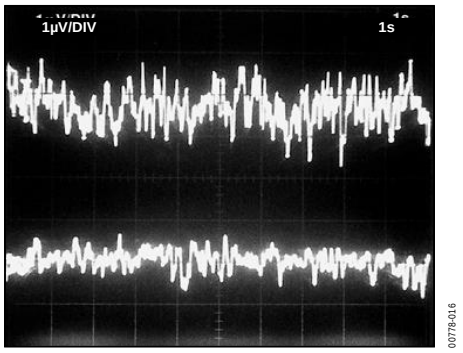



Figure 16. 0.1 Hz to 10 Hz RTI Voltage Noise (1 DIV = 1 µV p-p)

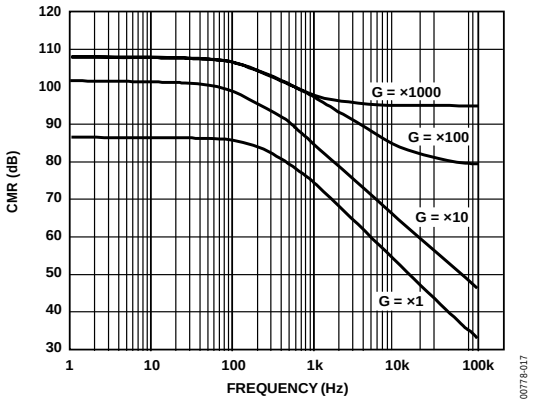



Figure 17. Common-Mode Rejection (CMR) vs. Frequency, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{REF}$ = 2.5 V, for Various Gain Settings (G)

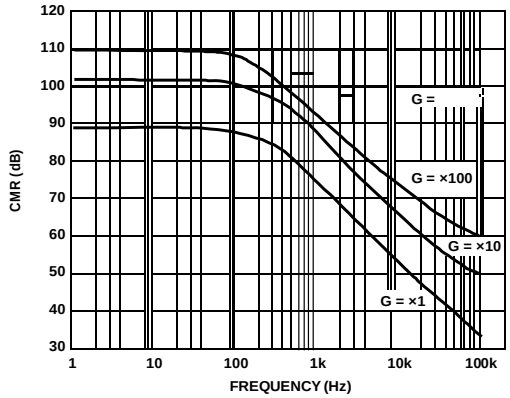



Figure 18. CMR vs. Frequency for Various Gain Settings (G)

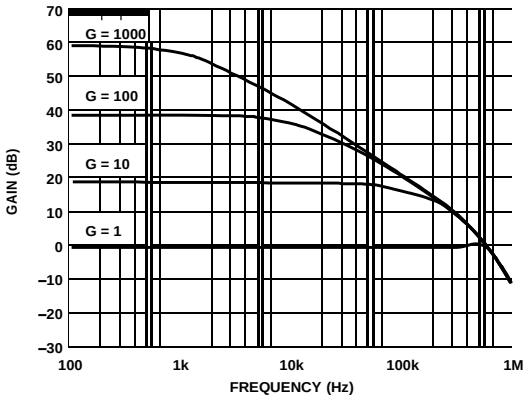



Figure 19. Gain vs. Frequency ($+V_S$ = 5 V, $-V_S$ = 0 V), $V_{REF}$ = 2.5 V, for Various Gain Settings (G)

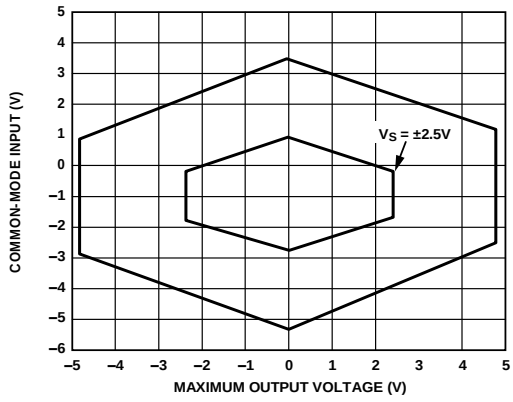



Figure 20. Maximum Output Voltage vs. Common-Mode Input, G = 1, $R_L$ = 100 kΩ for Two Supply Voltages

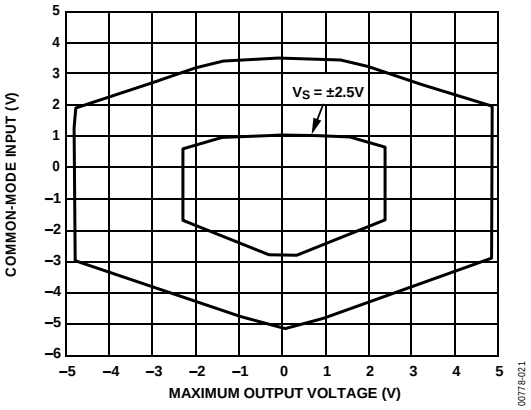



Figure 21. Maximum Output Voltage vs. Common-Mode Input, $G \geq 10$, $R_L = 100\ \Omega$, for Two Supply Voltages

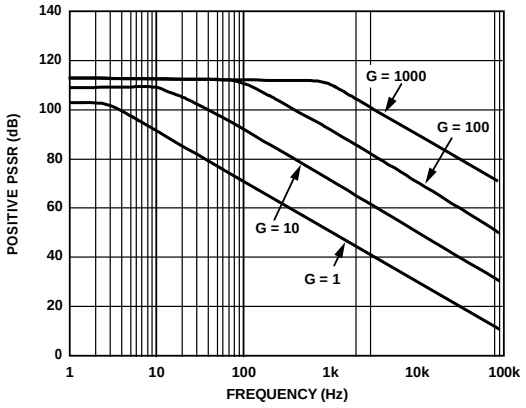



Figure 24. Positive PSRR vs. Frequency

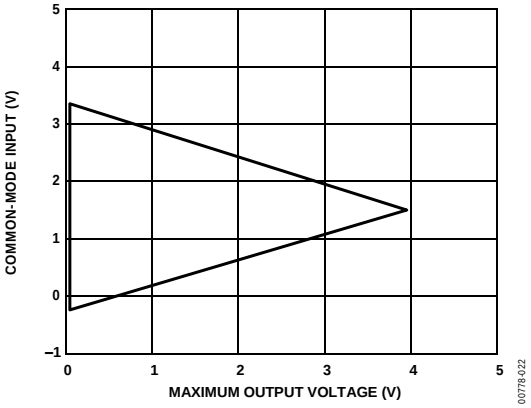



Figure 22. Maximum Output Voltage vs. Common-Mode Input, $G = 1$, $+V_S = 5\ V$, $-V_S = 0\ V$, $R_L = 100\ k\Omega$

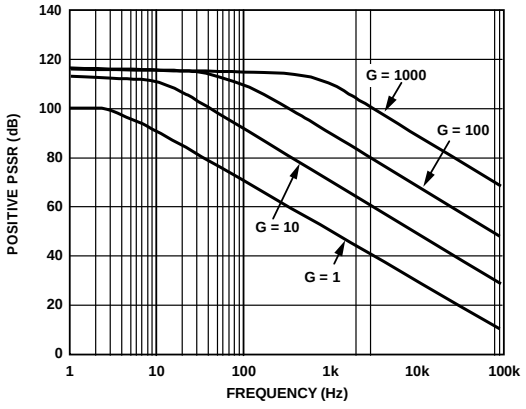



Figure 25. Positive PSRR vs. Frequency, $+V_S = 5V$, $-V_S = 0\ V$, for Various Gain Settings (G)

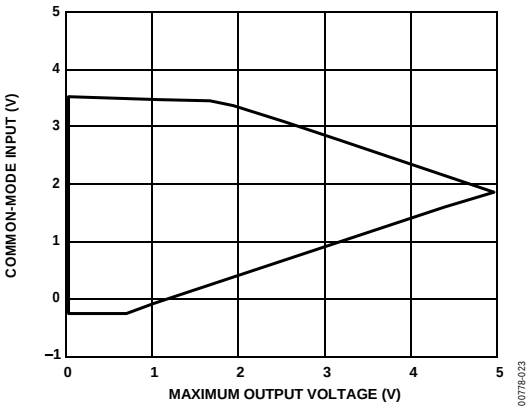



Figure 23. Maximum Output Voltage vs. Common-Mode Input, $G \geq 10$, $+V_S = 5\ V$, $-V_S = 0\ V$, $R_L = 100\ k\Omega$

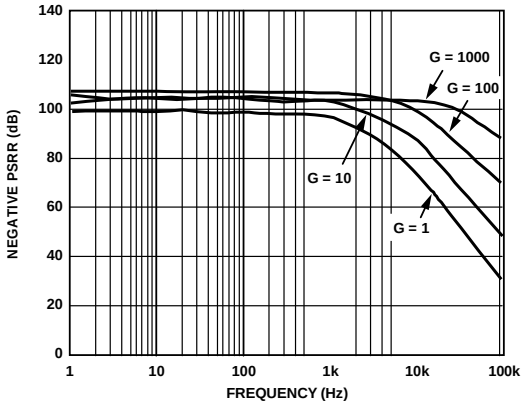



Figure 26. Negative PSRR vs. Frequency for Various Gain Settings (G)

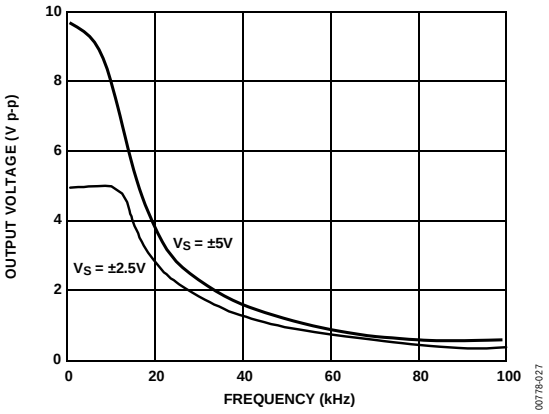



*Figure 27. Large Signal Response, G ≤ 10 for Two Supply Voltages*

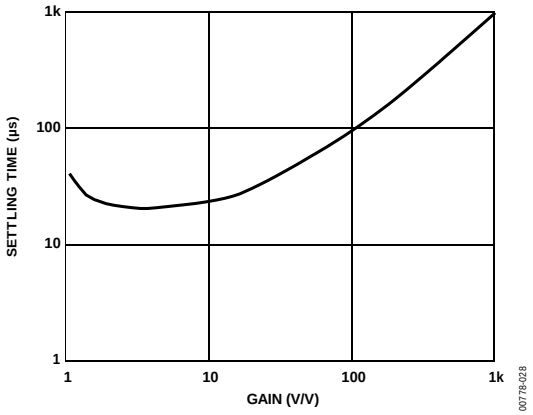



*Figure 28. Settling Time to 0.01% vs. Gain, for a 5 V Step at Output, $C_L$ = 100 pF*

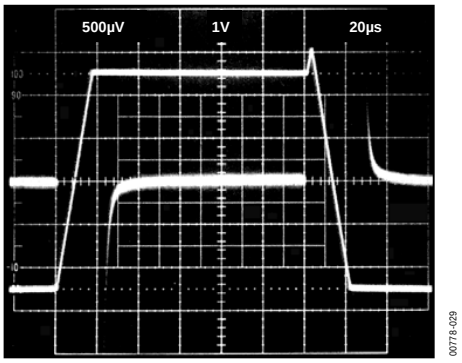



*Figure 29. Large Signal Pulse Response and Settling Time, G = −1 (0.250 mV = 0.01%), $C_L$ = 100 pF*

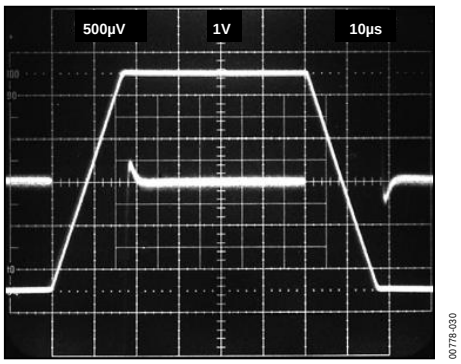



*Figure 30. Large Signal Pulse Response and Settling Time, G = −10 (0.250 mV = 0.01%), $C_L$ = 100 pF*

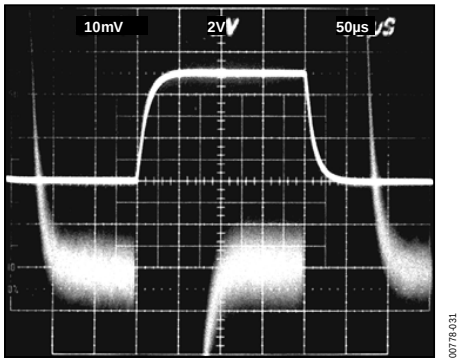



*Figure 31. Large Signal Pulse Response and Settling Time, G = 100, $C_L$ = 100 pF*

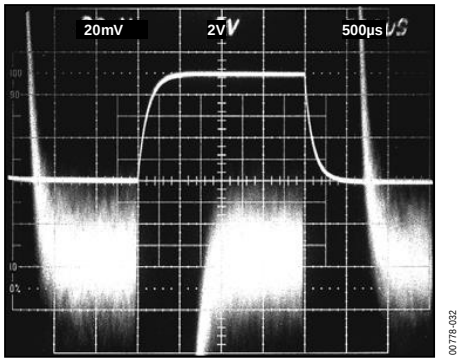



*Figure 32. Large Signal Pulse Response and Settling Time, G = −1000 (5 mV = 0.01%), $C_L$ = 100 pF*

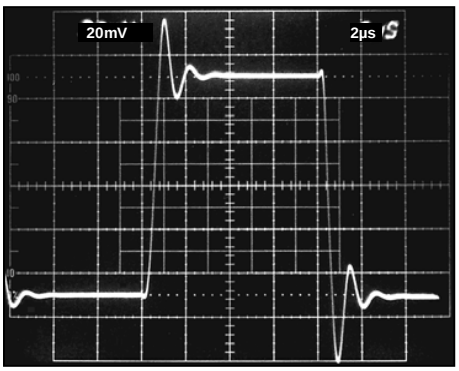



*Figure 33. Small Signal Pulse Response, G = 1, $R_L$ = 10 kΩ, $C_L$ = 100 pF*

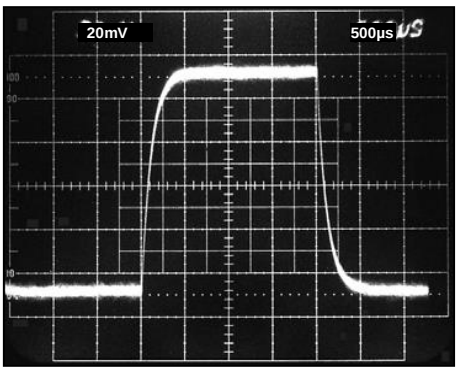



*Figure 36. Small Signal Pulse Response, G = 1000, $R_L$ = 10 kΩ, $C_L$ = 100 pF*

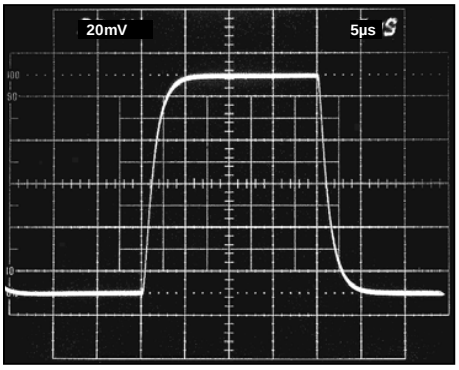



*Figure 34. Small Signal Pulse Response, G = 10, $R_L$ = 10 kΩ, $C_L$ = 100 pF*

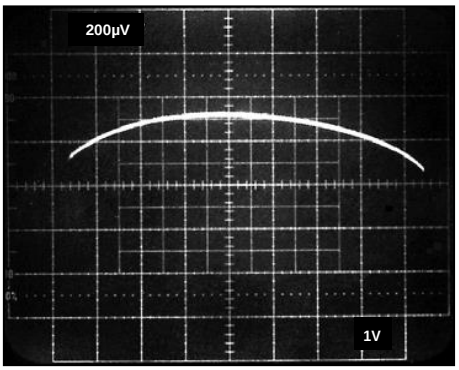



*Figure 37. Gain Nonlinearity, G = −1 (50 ppm/DIV)*

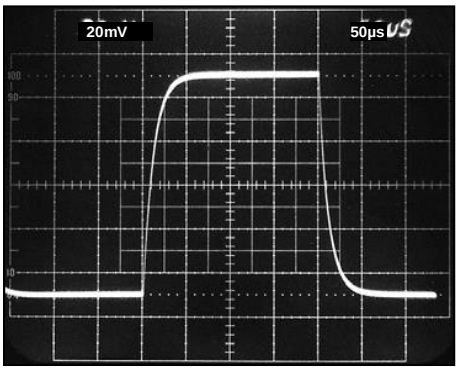



*Figure 35. Small Signal Pulse Response, G = 100, $R_L$ = 10 kΩ, $C_L$ = 100 pF*

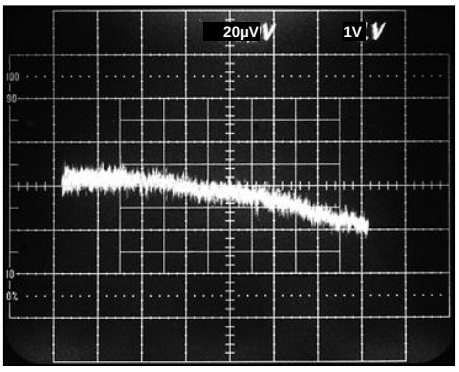



*Figure 38. Gain Nonlinearity, G = −10 (6 ppm/DIV)*

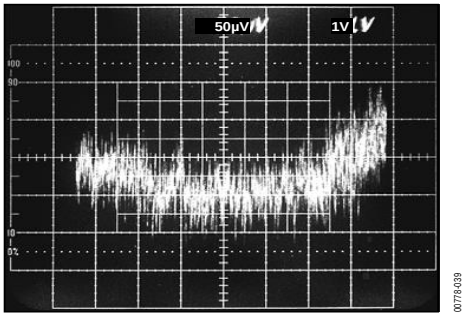



*Figure 39. Gain Nonlinearity, G = −100, 15 ppm/DIV*

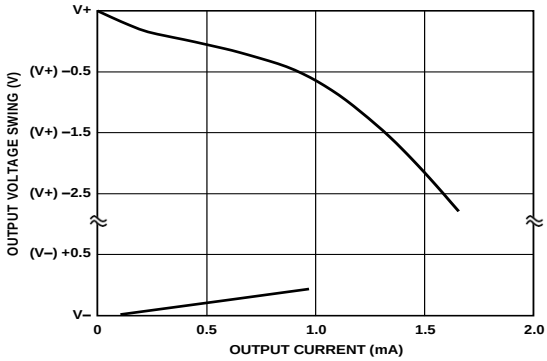



*Figure 40. Output Voltage Swing vs. Output Current*

## THEORY OF OPERATION

The HT8623 is an instrumentation amplifier based on a modified classic 3-op-amp approach, to assure single- or dual-supply operation even at common-mode voltages at the negative supply rail. Low voltage offsets, input and output, as well as absolute gain accuracy, and one external resistor to set the gain, make the HT8623 one of the most versatile instrumentation amplifiers in its class.

The input signal is applied to PNP transistors acting as voltage buffers and providing a common-mode signal to the input amplifiers (see Figure 41). An absolute value 50 kΩ resistor in each amplifier feedback assures gain programmability.

The differential output is

$$V_O = \left(1 + \frac{100\ \text{k}\Omega}{R_G}\right) V_C$$

The differential voltage is then converted to a single-ended voltage using the output amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Because the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the HT8623 can operate is further enhanced (see Figure 20 and Figure 21).

The output voltage at Pin 6 is measured with respect to the potential at Pin 5. The impedance of the reference pin is 100 kΩ; therefore, in applications requiring voltage conversion, a small resistor between Pin 5 and Pin 6 is all that is needed.

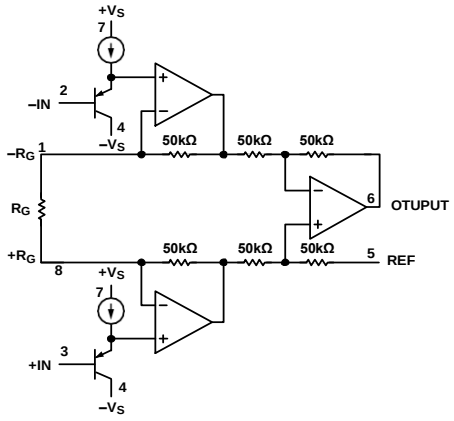



*Figure 41. Simplified Schematic*

Because of the voltage feedback topology of the internal op amps, the bandwidth of the in-amp decreases with increasing gain. At unity gain, the output amplifier limits the bandwidth.

# APPLICATIONS INFORMATION

## BASIC CONNECTION

Figure 42 and Figure 43 show the basic connection circuits for the HT8623. The $+V_S$ and $-V_S$ terminals are connected to the power supply. The supply can be either bipolar ($V_S$ = ±2.5 V to ±6 V) or single supply ($-V_S$ = 0 V, $+V_S$ = 3.0 V to 12 V). Capacitively decouple power supplies close to the power pins of the device. For best results, use surface-mount 0.1 µF ceramic chip capacitors and 10 µF electrolytic tantalum capacitors.

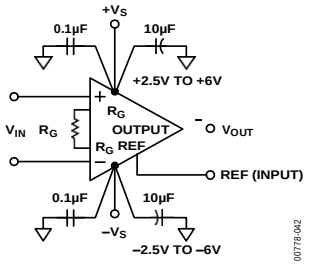



*Figure 42. Dual-Supply Basic Connection*

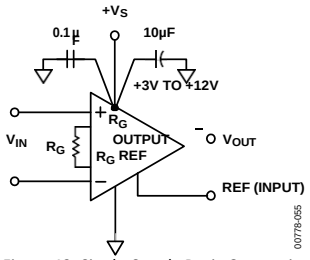



*Figure 43. Single-Supply Basic Connection*

The input voltage, which can be either single-ended (tie either −IN or +IN to ground) or differential, is amplified by the programmed gain. The output signal appears as the voltage difference between the OUTPUT pin and the externally applied voltage on the REF input. For a ground referenced output, REF must be grounded.

## GAIN SELECTION

The gain of the HT8623 is programmed by the $R_G$ resistor, or more precisely, by whatever impedance appears between Pin 1 and Pin 8. The HT8623 offers accurate gains using 0.1% to 1% tolerance resistors. Table 7 shows the required values of $R_G$ for the various gains. Note that for G = 1, the $R_G$ terminals are unconnected ($R_G = \infty$). For any arbitrary gain, $R_G$ can be calculated by

$$R_G = 100\ \text{k}\Omega/(G - 1)$$

## REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when bipolar signals are being amplified because it can be used to provide a virtual ground voltage. The voltage on the reference terminal can be varied from $-V_S$ to $+V_S$.

**Table 7. Required Values of Gain Resistors**

| Desired Gain | 1% Standard Table Value of $R_G$ | Calculated Gain Using 1% Resistors |
|---|---|---|
| 2 | 100 kΩ | 2 |
| 5 | 24.9 kΩ | 5.02 |
| 10 | 11 kΩ | 10.09 |
| 20 | 5.23 kΩ | 20.12 |
| 33 | 3.09 kΩ | 33.36 |
| 40 | 2.55 kΩ | 40.21 |
| 50 | 2.05 kΩ | 49.78 |
| 65 | 1.58 kΩ | 64.29 |
| 100 | 1.02 kΩ | 99.04 |
| 200 | 499 Ω | 201.4 |
| 500 | 200 Ω | 501 |
| 1000 | 100 Ω | 1001 |

## INPUT AND OUTPUT OFFSET VOLTAGE ERROR

The offset voltage ($V_{OS}$) of the HT8623 is attributed to two sources: those originating in the two input stages where the in-amp gain is established, and those originating in the subtractor output stage. The output error is divided by the programmed gain when referred to the input. In practice, the input errors dominate at high gain settings, whereas the output error prevails when the gain is set at or near unity.

The $V_{OS}$ error for any given gain is calculated as follows:

*Total Error Referred to Input (RTI)*
= *Input Error* + (*Output Error*/*G*)

*Total Error Referred to Output (RTO)*
= (*Input Error* × *G*) + *Output Error*

The RTI offset errors and noise voltages for different gains are listed in Table 8.

## INPUT PROTECTION

Internal supply-referenced clamping diodes allow the input, reference, output, and gain terminals of the HT8623 to safely withstand overvoltages of 0.3 V above or below the supplies. This overvoltage protection is true at all gain settings and when cycling power on and off. Overvoltage protection is particularly important because the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed this value, the current through these diodes must be limited to about 10 mA using external current limiting resistors (see Figure 44). The size of this resistor is defined by the supply voltage and the required overvoltage protection.

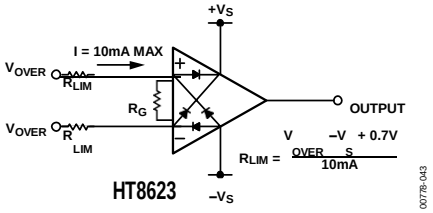



*Figure 44. Input Protection*

## RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. The circuit in Figure 45 provides good RFI suppression without reducing performance within the pass band of the in-amp. Resistor R1 and Capacitor C1 (and likewise, R2 and C2) form a low-pass RC filter that has a −3 dB bandwidth equal to f = 1/(2 π R1C1). Using the component values shown, this filter has a −3 dB bandwidth of approximately 40 kHz. The R1 and R2 resistors were selected to be large enough to isolate the input of the circuit from the capacitors, but not large enough to significantly increase the noise of the circuit. To preserve common-mode rejection in the pass band of the amplifier, the C1 and C2 capacitors must be 5% or better units, or low cost 20% units can be tested and binned to provide closely matched devices.

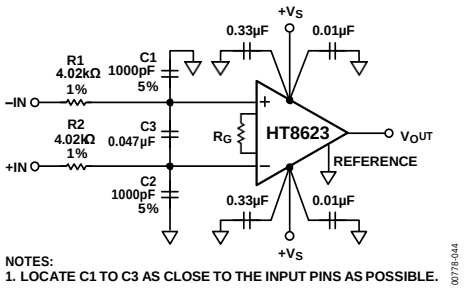



*Figure 45. Circuit to Attenuate RF Interference*

Capacitor C3 is needed to maintain common-mode rejection at low frequencies. R1/R2 and C1/C2 form a bridge circuit whose output appears across the input pins of the in-amp. Any mismatch between C1 and C2 unbalances the bridge and reduces the common-mode rejection. C3 ensures that any RF signals are common mode (the same on both in-amp inputs) and are not applied differentially. This second low-pass network, R1 + R2 C3, has a −3 dB frequency equal to 1/(2π(R1 + R2)(C3)). Using a C3 value of 0.047 µF, the −3 dB signal bandwidth of this circuit is approximately 400 Hz. The typical dc offset shift over frequency is less than 1.5 µV, and the RF signal rejection of the circuit is better than 71 dB. The 3 dB signal bandwidth of this circuit can be increased to 900 Hz by reducing R1 and R2 to 2.2 kΩ. The performance is similar to using 4 kΩ resistors, except that the circuitry preceding the in-amp must drive a lower impedance load.

**Table 8. RTI Error Sources**

| | Maximum Total Input Offset Error (µV) | | Maximum Total Input Offset Drift (µV/°C) | | Total Input Referred Noise (nV/√Hz) | |
|---|---|---|---|---|---|---|
| Gain | HT8623A | HT8623B | HT8623A | HT8623B | HT8623A | HT8623B |
| 1 | 1200 | 600 | 12 | 11 | 62 | 62 |
| 2 | 700 | 350 | 7 | 6 | 45 | 45 |
| 5 | 400 | 200 | 4 | 3 | 38 | 38 |
| 10 | 300 | 150 | 3 | 2 | 35 | 35 |
| 20 | 250 | 125 | 2.5 | 1.5 | 35 | 35 |
| 50 | 220 | 110 | 2.2 | 1.2 | 35 | 35 |
| 100 | 210 | 105 | 2.1 | 1.1 | 35 | 35 |
| 1000 | 200 | 100 | 2 | 1 | 35 | 35 |

The circuit in Figure 45 must be built using a printed circuit board (PCB) with a ground plane on both sides. All component leads must be as short as possible. The R1 and R2 resistors can be common 1% metal film units; however, the C1 and C2 capacitors must be ±5% tolerance devices to avoid degrading the common-mode rejection of the circuit. Either the traditional 5% silver mica units or Panasonic ±2% PPS film capacitors are recommended.

In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield must be properly driven. Figure 46 shows an active guard driver that is configured to improve ac common-mode rejection by bootstrapping the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

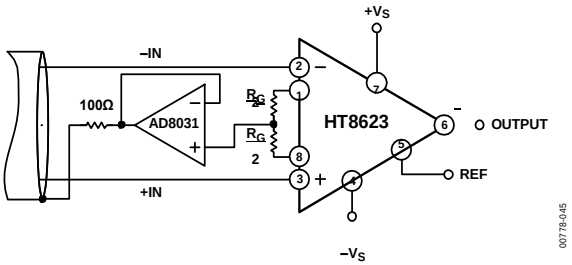



*Figure 46. Common-Mode Shield Driver*

## GROUNDING

Because the HT8623 output voltage is developed with respect to the potential on the reference terminal, many grounding problems can be solved by simply tying the REF pin to the appropriate local ground. The REF pin must, however, be tied to a low impedance point for optimal CMR.

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). To isolate low level analog signals from a noisy digital environment, many data acquisition components have separate analog and digital ground returns (see Figure 47). All ground pins from mixed signal components, such as analog-to-digital converters (ADCs), must be returned through the high quality analog ground plane. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. The digital return currents from the ADC that flow in the analog ground plane, in general, have a negligible effect on noise performance.

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 48 shows how to minimize interference between the digital and analog circuitry. As in the previous case, use separate analog and digital ground planes (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes must be connected at the ground pin of the power supply. Run separate traces from the power supply to the supply pins of the digital and analog circuits. Ideally, each device has its own power supply trace, but these can be shared by a number of devices, as long as a single trace is not used to route current to both digital and analog circuitry.

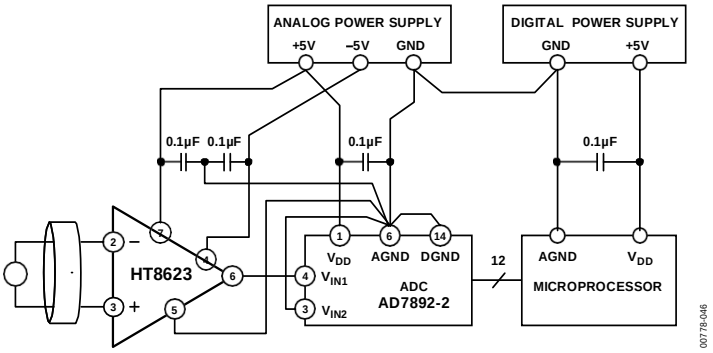
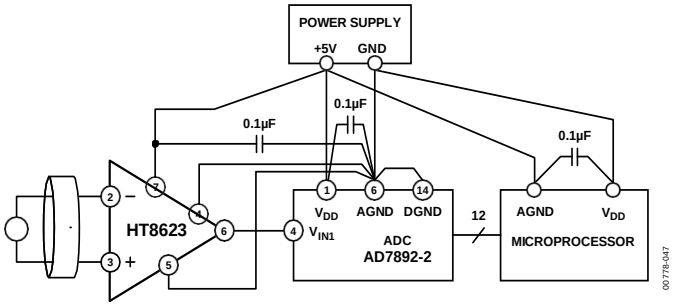



*Figure 47. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies*



### *Ground Returns for Input Bias Currents*

Input bias currents are those dc currents that must flow to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying floating input sources, such as transformers or ac-coupled sources, there must be a direct dc path into each input so that the bias current can flow. Figure 49, Figure 50, and Figure 51 show how a bias current path can be provided for the cases of transformer coupling, thermocouple, and capacitive ac coupling. In dc-coupled resistive bridge applications, providing this path is generally not necessary because the bias current simply flows from the bridge supply through the bridge into the amplifier. However, if the impedances that the two inputs see are large and differ by a large amount (>10 kΩ), the offset current of the input stage causes dc errors proportional with the input offset voltage of the amplifier.

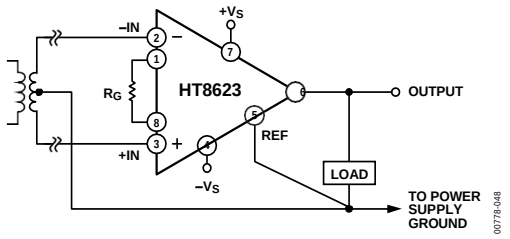



*Figure 49. Ground Returns for Bias Currents with Transformer-Coupled Inputs*

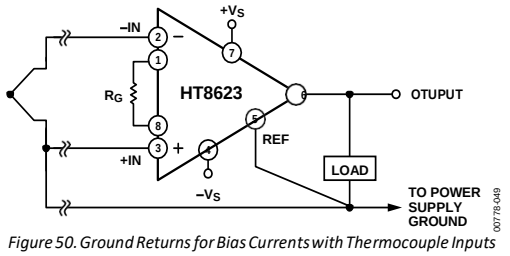



*Figure 50. Ground Returns for Bias Currents with Thermocouple Inputs*

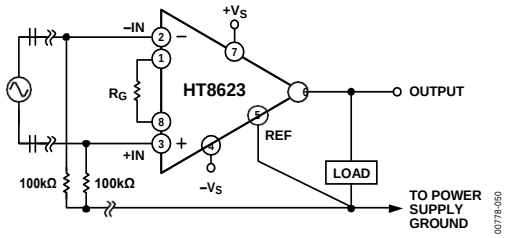



*Figure 51. Ground Returns for Bias Currents with AC-Coupled Inputs*

### *Output Buffering*

The HT8623 is designed to drive loads of 10 kΩ or greater. If the load is less than this value, the output of the HT8623 must be buffered with a precision single-supply op amp, such as the OP113. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω. Table 9 summarizes the performance of some buffer op amps.

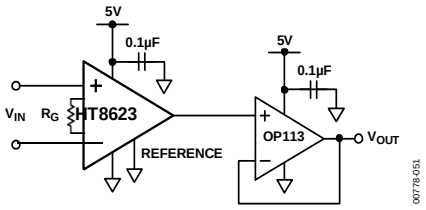



*Figure 52. Output Buffering*

**Table 9. Buffering Options**

| Op Amp | Description |
|---|---|
| OP113 | Single-supply, high output current |
| OP191 | Rail-to-rail input and output, low supply current |

### *Single-Supply Data Acquisition System*

Interfacing bipolar signals to single-supply ADCs presents a challenge. The bipolar signal must be mapped into the input range of the ADC. Figure 53 shows how this translation can be achieved.

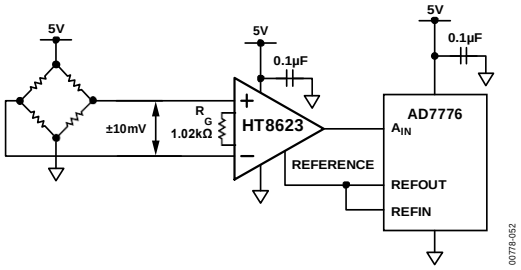



*Figure 53. A Single-Supply Data Acquisition System*

The bridge circuit is excited by a 5 V supply. The full-scale output voltage from the bridge (±10 mV) therefore has a common-mode level of 2.5 V. The HT8623 removes the common-mode component and amplifies the input signal by a factor of 100 ($R_{GAIN}$ = 1.02 kΩ), which results in an output signal of ±1 V. To prevent this signal from running into the ground rail of the HT8623, the voltage on the REF pin must be raised to at least 1 V. In this example, the 2 V reference voltage from the AD7776 ADC biases the output voltage of the HT8623 to 2 V ±1 V, which corresponds to the input range of the ADC.

### *Amplifying Signals with Low Common-Mode Voltage*

Because the common-mode input range of the HT8623 extends
0.1 V below ground, it is possible to measure small differential signals which have low or no common-mode component. Figure 54 shows a thermocouple application where one side of the J-type thermocouple is grounded.

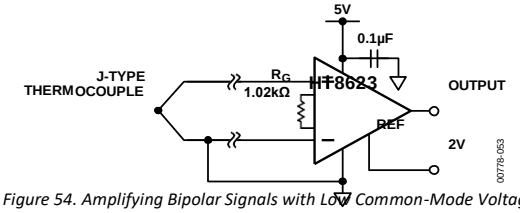



*Figure 54. Amplifying Bipolar Signals with Low Common-Mode Voltage*

Over a temperature range of −200°C to +200 ℃, the J-type thermocouple delivers a voltage ranging from −7.890 mV to +10.777 mV. A programmed gain on the HT8623 of 100 ($R_G$ = 1.02 kΩ) and a voltage on the REF pin of 2 V result in the output voltage ranging from 1.110 V to 3.077 V relative to ground.

## INPUT DIFFERENTIAL AND COMMON-MODE RANGE vs. SUPPLY AND GAIN

Figure 55 shows a simplified block diagram of the HT8623. The voltages at the outputs of Amplifier A1 and Amplifier A2 are given by

$$V_{A2} = V_{CM} + V_{DIFF}/2 + 0.6\ V + V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V + V_{DIFF} \times Gain/2$$

$$V_{A1} = V_{CM} - V_{DIFF}/2 + 0.6\ V + V_{DIFF} \times R_F/R_G$$
$$= V_{CM} + 0.6\ V - V_{DIFF} \times Gain/2$$

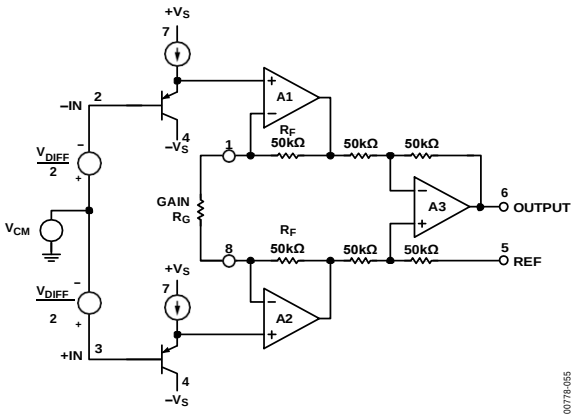



*Figure 55. Simplified Block Diagram*

The voltages on these internal nodes are critical in determining whether the output voltage is clipped. The $V_{A1}$ and $V_{A2}$ voltages can swing from approximately 10 mV above the negative supply (V− or ground) to within approximately 100 mV of the positive rail before clipping occurs. Based on this and from the previous equations, the maximum and minimum input common-mode voltages are given by the following equations:

$$V_{CMMAX} = V+ - 0.7\ V - V_{DIFF} \times Gain/2$$

$$V_{CMMIN} = V- - 0.590\ V + V_{DIFF} \times Gain/2$$

These equations can be rearranged to give the maximum possible differential voltage (positive or negative) for a particular common-mode voltage, gain, and power supply. Because the signals on A1 and A2 can clip on either rail, the maximum differential voltage is the lesser of the two equations.

$$|V_{DIFFMAX}| = 2\ (V+ - 0.7\ V - V_{CM})/Gain$$

$$|V_{DIFFMAX}| = 2\ (V_{CM} - V- + 0.590\ V)/Gain$$

However, the range on the differential input voltage range is also constrained by the output swing. Therefore, the range of $V_{DIFF}$ may need to be lower according the following equation:

$$Input\ Range \leq Available\ Output\ Swing/Gain$$

For a bipolar input voltage with a common-mode voltage that is roughly half way between the rails, $V_{DIFFMAX}$ is half the value that the previous equations yield because the REF pin is at midsupply. Note that the available output swing is given for different supply conditions in the Specifications section.

The equations can be rearranged to give the maximum gain for a fixed set of input conditions. The maximum gain is the lesser of the two equations.

$$Gain_{MAX} = 2\ (V+ - 0.7\ V - V_{CM})/V_{DIFF}$$

$$Gain_{MAX} = 2\ (V_{CM} - V- + 0.590\ V)/V_{DIFF}$$

Again, it is recommended that the resulting gain times the input range is less than the available output swing. If this is not the case, the maximum gain is given by

$$Gain_{MAX} = Available\ Output\ Swing/Input\ Range$$

Also for bipolar inputs (that is, input range = 2 $V_{DIFF}$), the maximum gain is half the value yielded by the previous equations because the REF pin must be at midsupply.

The maximum gain and resulting output swing for different input conditions is given in Table 10. Output voltages are referenced to the voltage on the REF pin.

For the purposes of computation, it is necessary to break down the input voltage into its differential and common-mode components. Therefore, when one of the inputs is grounded or at a fixed voltage, the common-mode voltage changes as the differential voltage changes. Take the case of the thermocouple amplifier in Figure 54. The inverting input on the HT8623 is grounded; therefore, when the input voltage is −10 mV, the voltage on the noninverting input is −10 mV. For the purpose of the signal swing calculations, this input voltage must be composed of a common-mode voltage of −5 mV (that is, (+IN + −IN)/2) and a differential input voltage of −10 mV (that is, +IN − −IN).

**Table 10. Maximum Attainable Gain and Resulting Output Swing for Different Input Conditions**

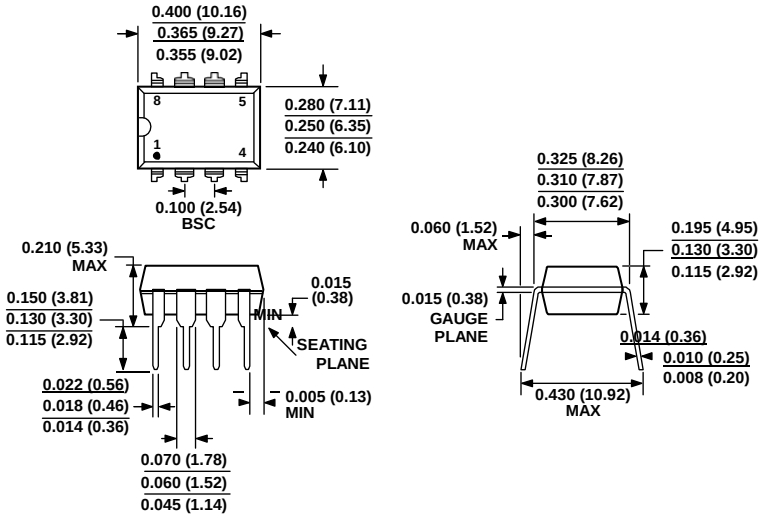
| $V_{CM}$ | $V_{DIFF}$ | REF Pin | Supply Voltages | Maximum Gain | Closest 1% Gain Resistor | Resulting Gain | Output Swing |
|---|---|---|---|---|---|---|---|
| 0 V | ±10 mV | 2.5 V | +5 V | 118 | 866 Ω | 116 | ±1.2 V |
| 0 V | ±100 mV | 2.5 V | +5 V | 11.8 | 9.31 kΩ | 11.7 | ±1.1 V |
| 0 V | ±10 mV | 0 V | ±5 V | 490 | 205 Ω | 488 | ±4.8 V |
| 0 V | ±100 mV | 0 V | ±5 V | 49 | 2.1 kΩ | 48.61 | ±4.8 V |
| 0 V | ±1 V | 0 V | ±5 V | 4.9 | 26.1 kΩ | 4.83 | ±4.8 V |
| 2.5 V | ±10 mV | 2.5 V | +5 V | 242 | 422 Ω | 238 | ±2.3 V |
| 2.5 V | ±100 mV | 2.5 V | +5 V | 24.2 | 4.32 kΩ | 24.1 | ±2.4 V |
| 2.5 V | ±1 V | 2.5 V | +5 V | 2.42 | 71.5 kΩ | 2.4 | ±2.4 V |
| 1.5 V | ±10 mV | 1.5 V | +3 V | 142 | 715 Ω | 141 | ±1.4 V |
| 1.5 V | ±100 mV | 1.5 V | +3 V | 14.2 | 7.68 kΩ | 14 | ±1.4 V |
| 0 V | ±10 mV | 1.5 V | +3 V | 118 | 866 Ω | 116 | ±1.1 V |
| 0 V | ±100 mV | 1.5 V | +3 V | 11.8 | 9.31 kΩ | 11.74 | ±1.1 V |

## ADDITIONAL INFORMATION

For an updated design of the HT8623, see the HT8223.

For a selection guide to all Analog Devices instrumentation amplifiers, see the Instrumentation Amplifiers page on the Analog Devices website at www.analog.com.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

*Figure 57. 8-Lead Plastic Dual In-Line Package [PDIP]*
*Narrow Body (N-8)*
*Dimensions shown in inches and (millimeters)*

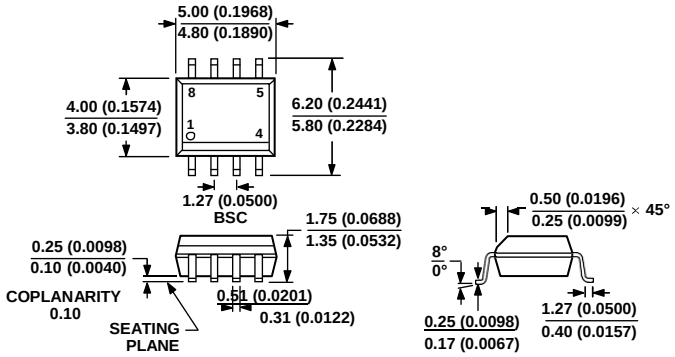



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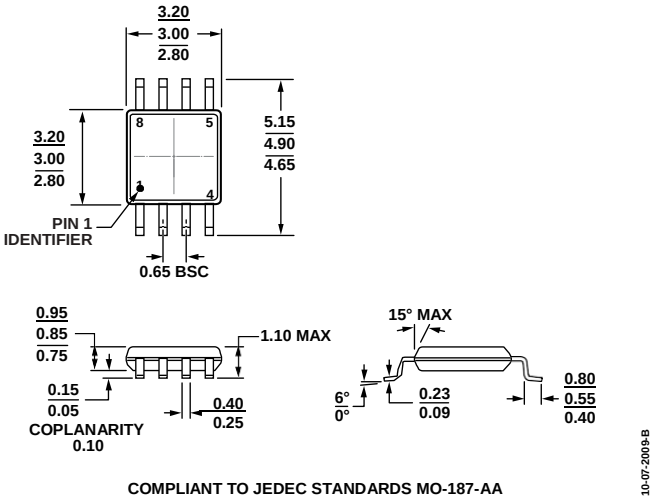
*Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body (R-8)*
*Dimensions shown in millimeters and (inches)*




**COMPLIANT TO JEDEC STANDARDS MO-187-AA**

*Figure 59. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*