Remote 8-bit I/O expander for I²C-bus

(compatible to PCF8574)

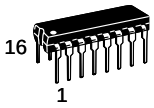
The device consists of an 8-bit quasi-bidirectional port and an I2C-bus interface. The HT8574B has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I2C-bus. This means that the HT8574B can remain a simple slave device.The HT8574B and HT8574A versions differ only in their slave address as shown in Fig.10.

1 FEATURES

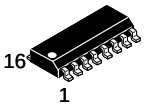
- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum • I²C-bus to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with HT8574A)

2 GENERAL DESCRIPTION

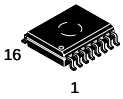
The HT8574B is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus).



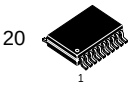
DIP16 N SUFFIX
HT8574ANZ
HT8574BNZ



SOP16 R SUFFIX
HT8574ARZ
HT8574BRZ



WSOP16 W SUFFIX
HT8574ARWZ
HT8574BRWZ



TSSOP20 T SUFFIX
HT8574ARTZ
HT8574BRTZ

SSOP16 S SUFFIX
HT8574ARSZ
HT8574BRSZ

QFN16-3*3 Q SUFFIX
HT8574ARQZ
HT8574BRQZ

T_A= from -45 to 125 °C For all packages

4 BLOCK DIAGRAM

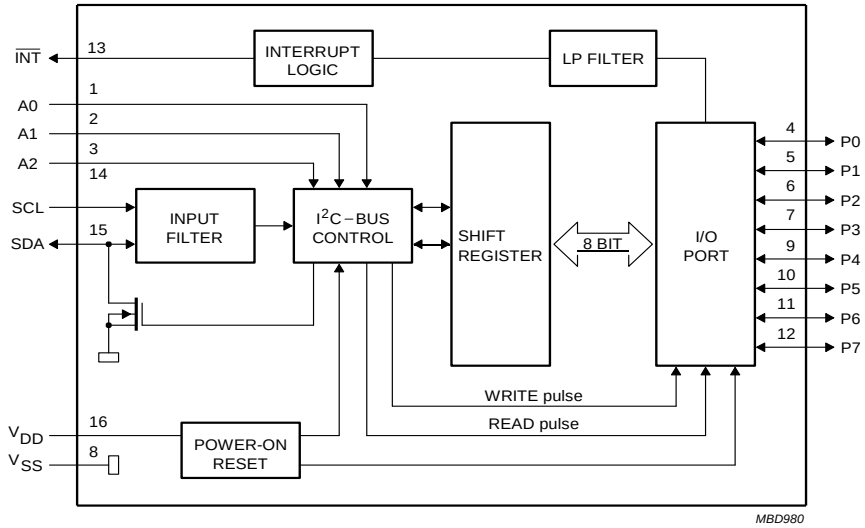


Fig.1 Block diagram (pin numbers apply to DIP16,SSOP16 and WSO16 packages).

5 PINNING

5.1 packages

SYMBOL	DESCRIPTION
A0	address input 0
A1	address input 1
A2	address input 2
P0	quasi-bidirectional I/O 0
P1	quasi-bidirectional I/O 1
P2	quasi-bidirectional I/O 2
P3	quasi-bidirectional I/O 3
V_{SS}	supply ground
P4	quasi-bidirectional I/O 4
P5	quasi-bidirectional I/O 5
P6	quasi-bidirectional I/O 6
P7	quasi-bidirectional I/O 7
INT	interrupt output (active LOW)
SCL	serial clock line
SDA	serial data line
V_{DD}	supply voltage

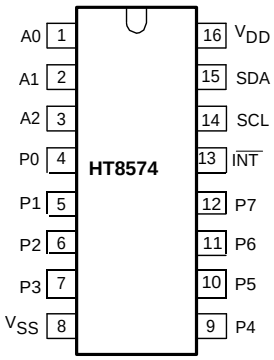


Fig.2 Pin configuration (DIP16&WSO16&SSOP16).

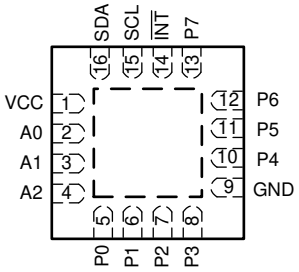


Fig.3 Pin configuration (QFN16-3*3).

5.2 TSSOP20 package

SYMBOL	PIN	DESCRIPTION
INT	1	interrupt output (active LOW)
SCL	2	serial clock line
n.c.	3	not connected
SDA	4	serial data line
V_{DD}	5	supply voltage
A0	6	address input 0
A1	7	address input 1
n.c.	8	not connected
A2	9	address input 2
P0	10	quasi-bidirectional I/O 0
P1	11	quasi-bidirectional I/O 1
P2	12	quasi-bidirectional I/O 2
n.c.	13	not connected
P3	14	quasi-bidirectional I/O 3
V_{SS}	15	supply ground
P4	16	quasi-bidirectional I/O 4
P5	17	quasi-bidirectional I/O 5
n.c.	18	not connected
P6	19	quasi-bidirectional I/O 6
P7	20	quasi-bidirectional I/O 7

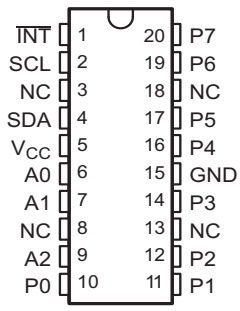


Fig.4 Pin configuration (TSSOP20).

6 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.5).

6.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.6).

6.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.7).

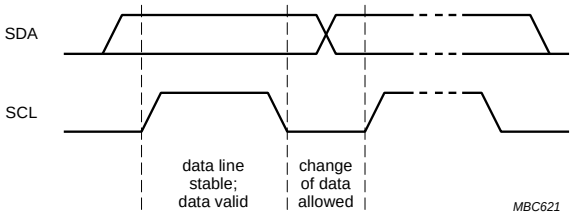


Fig.5 Bit transfer.

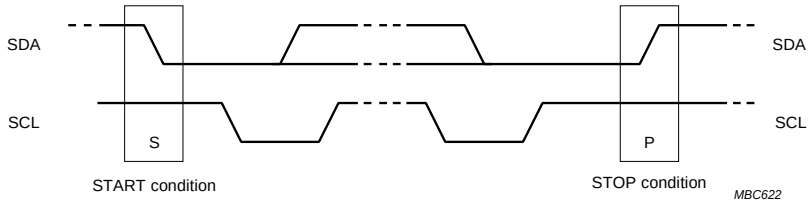


Fig.6 Definition of start and stop conditions.

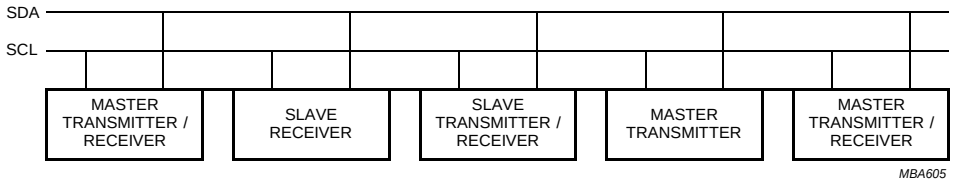


Fig.7 System configuration.

6.4 Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Fig.8). The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

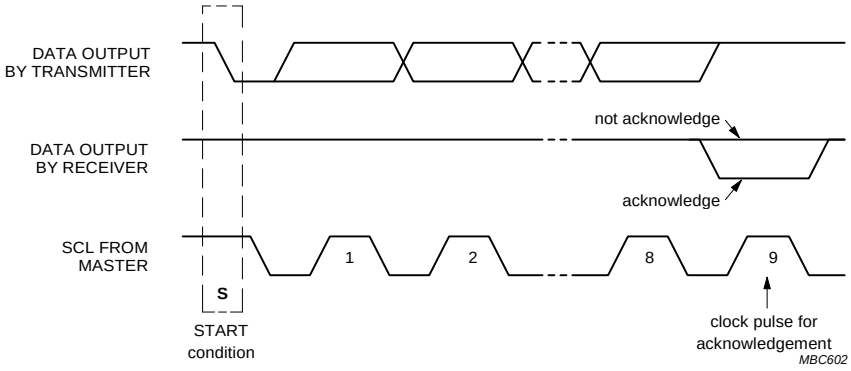


Fig.8 Acknowledgment on the I^2C-bus.

7 FUNCTIONAL DESCRIPTION

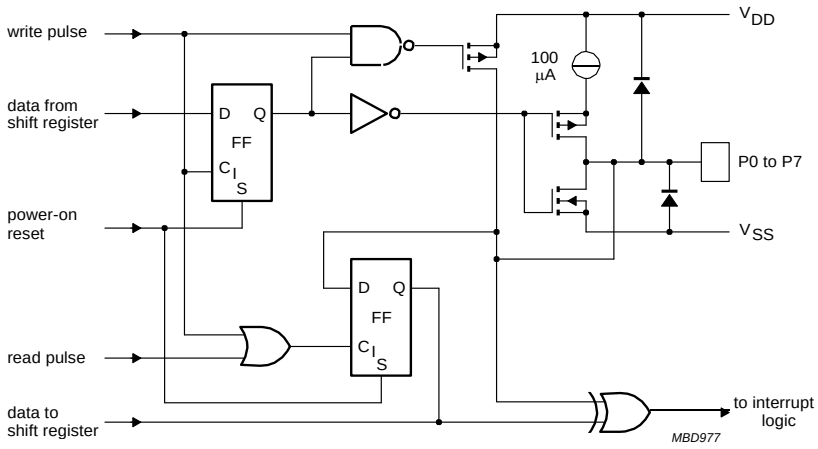


Fig.9 Simplified schematic diagram of each I/O.

7.1 Addressing

For addressing see Figs 10, 11 and 12.

a. HT8574B. b. HT8574A.

Fig.10 HT8574B and HT8574A slave addresses.

Each of the HT8574B's eight I/Os can be independently used as an input or output. Input data is transferred from the port to the microcontroller by the READ mode (see Fig.12). Output data is transmitted to the port by the WRITE mode (see Fig.11).

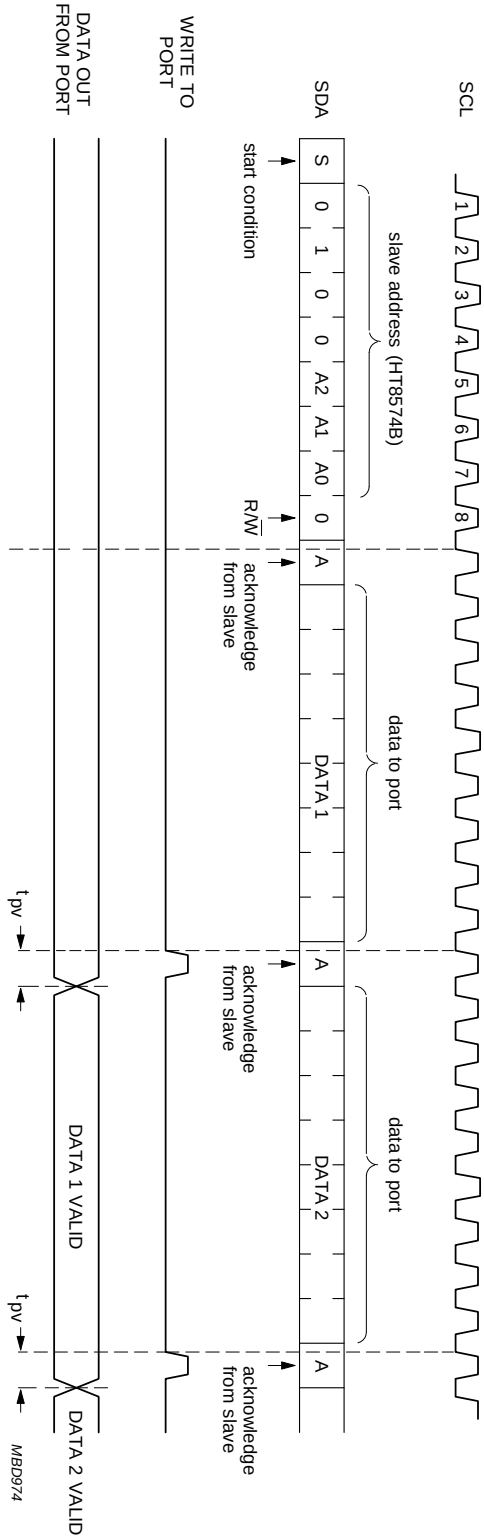
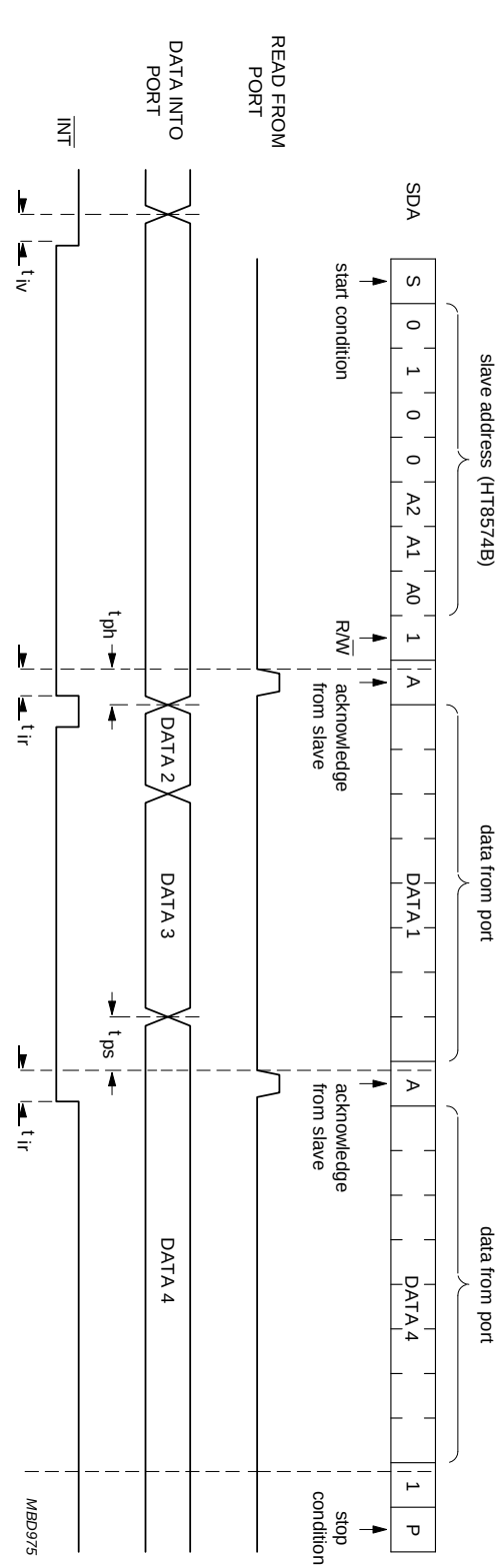


Fig.11 WRITE mode (output).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.12 READ mode (input).

7.2 Interrupt output

The HT8574B provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller (see Figs 13 and 14). This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the I/Os after resetting will be detected and, after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

7.3 Quasi-bidirectional I/Os

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction (see Fig.15). At power-on the I/Os are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs.

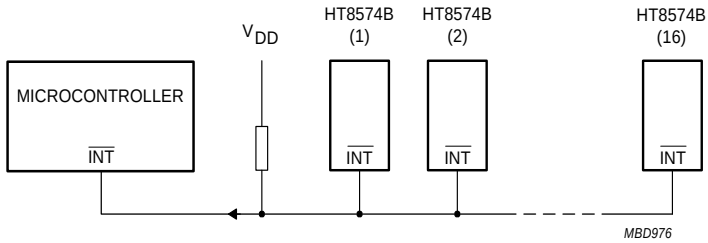


Fig.13 Application of multiple HT8574Bs with interrupt.

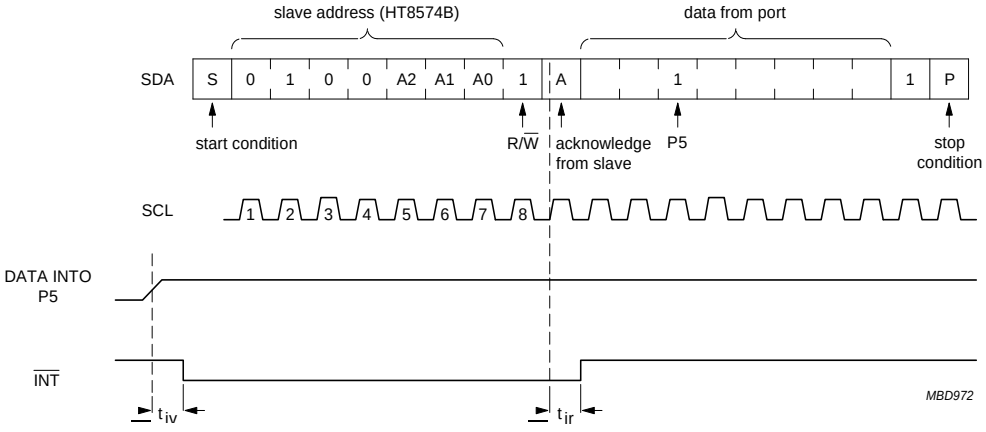


Fig.14 Interrupt generated by a change of input to I/O P5.

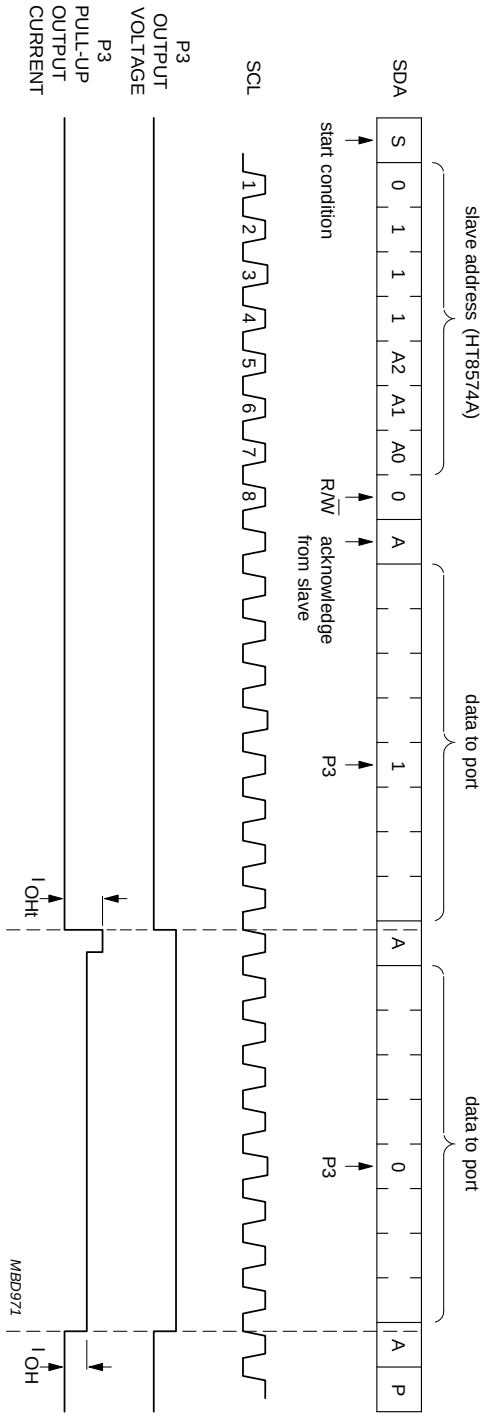


Fig.15 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7.0	V
V_I	input voltage	V_{SS} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–	±20	mA
I_O	DC output current	–	±25	mA
I_{DD}	supply current	–	±100	mA
I_{SS}	supply current	–	±100	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	ambient temperature	–45	+125	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	–	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}	–	2.5	10	µA
V_{POR}	Power-on reset voltage	V_{DD} = 6 V; no load; V_I = V_{DD} or V_{SS}; note 1	–	1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		–0.5	–	+0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	µA
C_i	input capacitance	V_I = V_{SS}	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/Os						
V_{IL}	LOW level input voltage		–0.5	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.5	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	–	–	±400	μA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25	–	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{SS}$	30	–	300	μA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.15); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	–	–1	–	mA
C_i	input capacitance		–	–	10	pF
C_o	output capacitance		–	–	10	pF
Port timing; $C_L \leq$ 100 pF (see Figs 11 and 12)						
t_{pv}	output data valid		–	–	4	μs
t_{su}	input data set-up time		0	–	–	μs
t_h	input data hold time		4	–	–	μs
Interrupt $\overline{INT}$ (see Fig.14)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	–	–	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	μA
TIMING; $C_L \leq$ 100 pF						
t_{iv}	input data valid time		–	–	4	μs
t_{ir}	reset delay time		–	–	4	μs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage		–0.5	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.5	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	–250	–	+250	nA

Note

1. The Power-on reset circuit resets the I^2C-bus logic at $V_{DD} < V_{POR}$ and sets all I/Os to logic 1 (with current source to V_{DD}).

11 I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.16; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

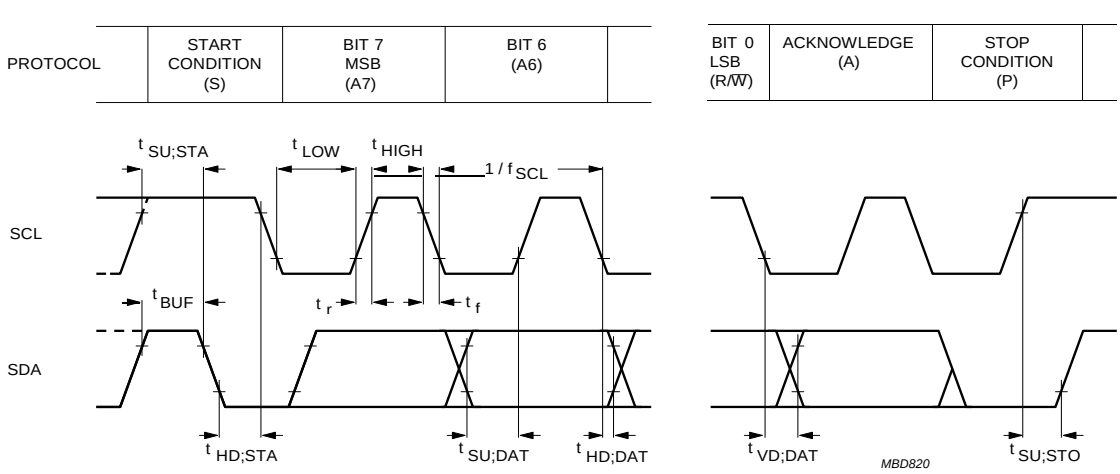
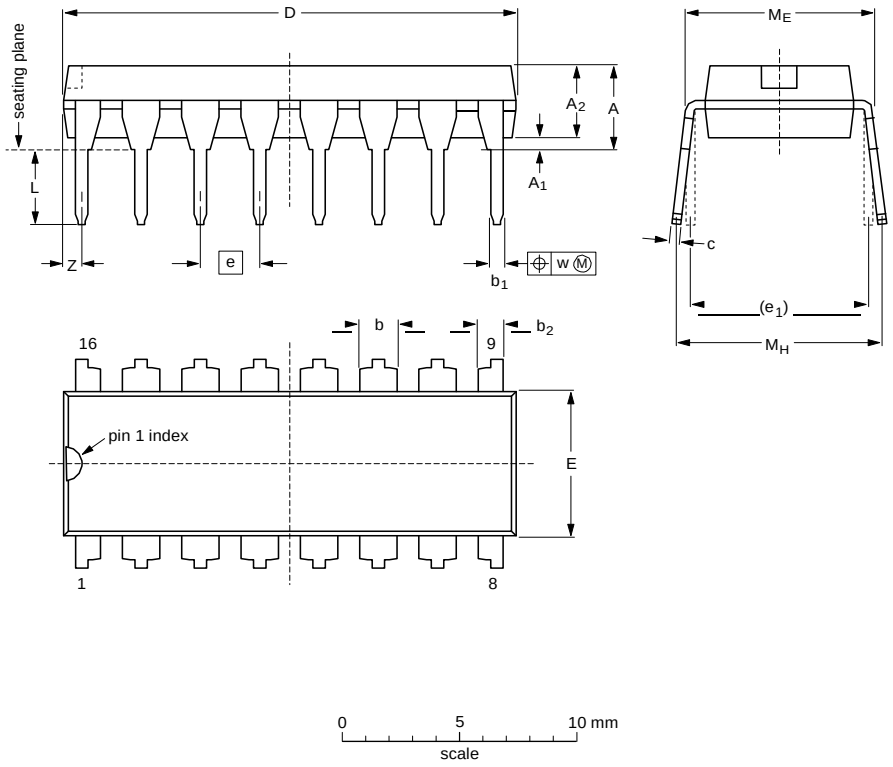


Fig.16 I²C-bus timing diagram.

12 PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

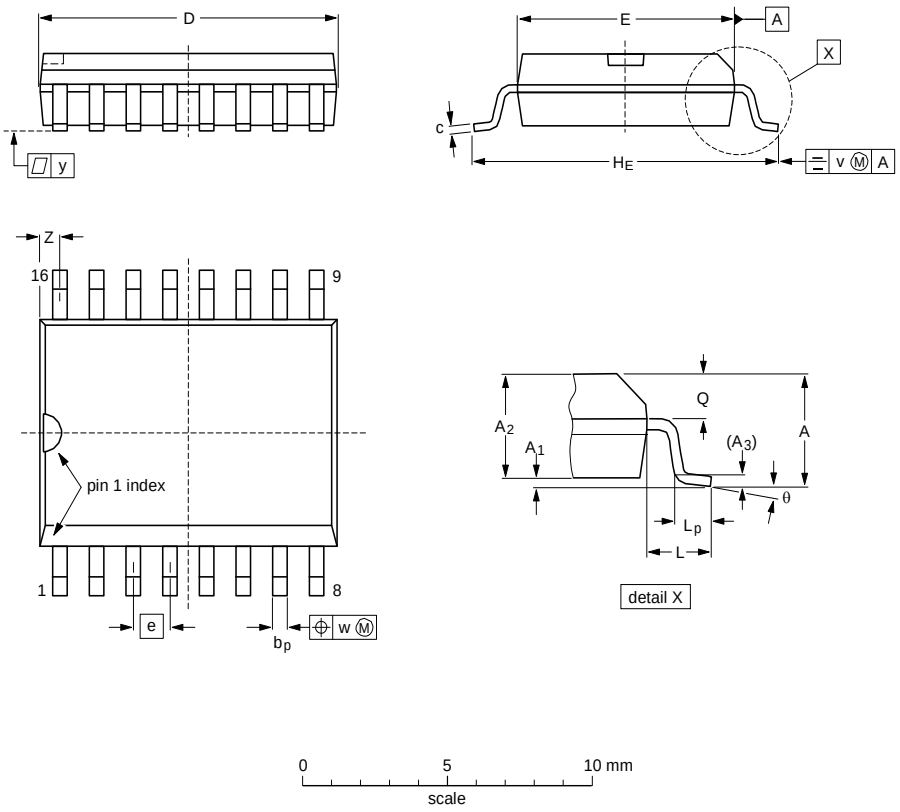
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

WSOP16: plastic small outline package; 16 leads; body width 7.5 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

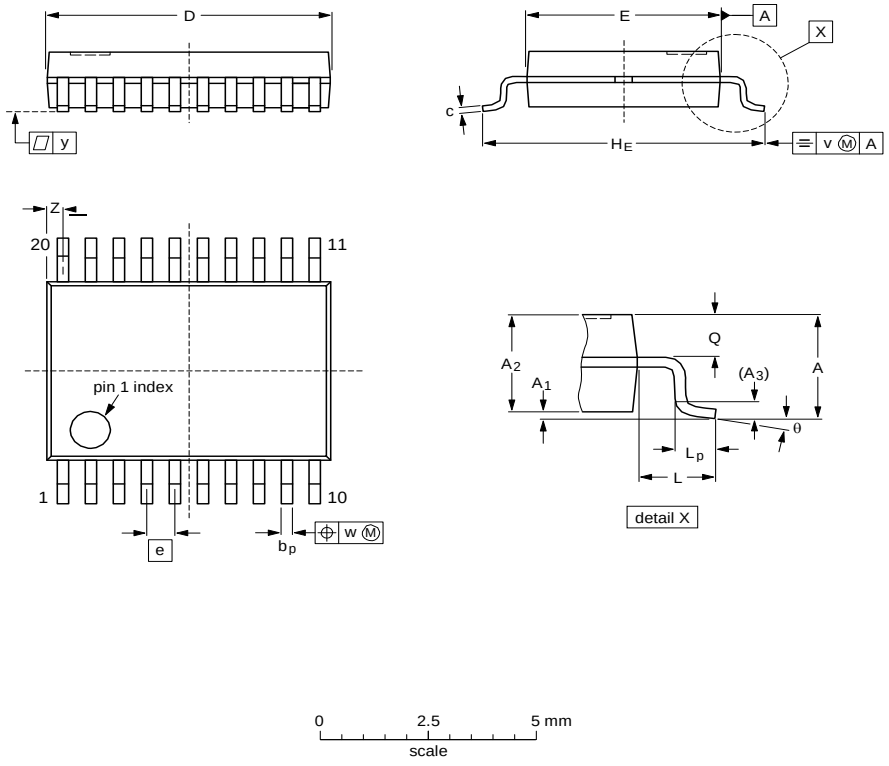
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013				~~97-05-22~~ 99-12-27

TSSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

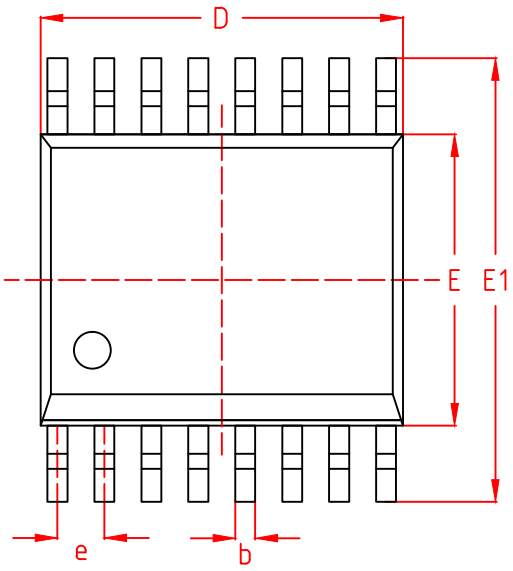
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

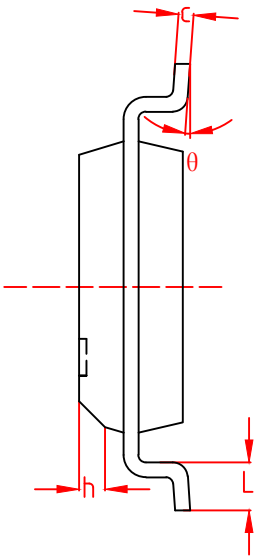
OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1		MO-152					~~95-02-22~~ 99-12-27

SSOP16: plastic small outline package; 16 leads; body width 3.9 mm

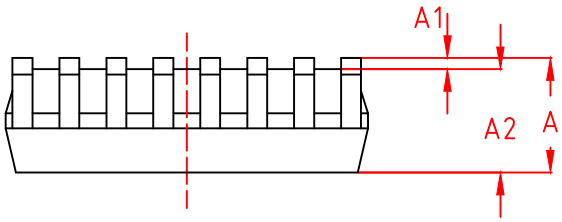
TOP VIEW
正视图



SIDE VIEW
侧视图

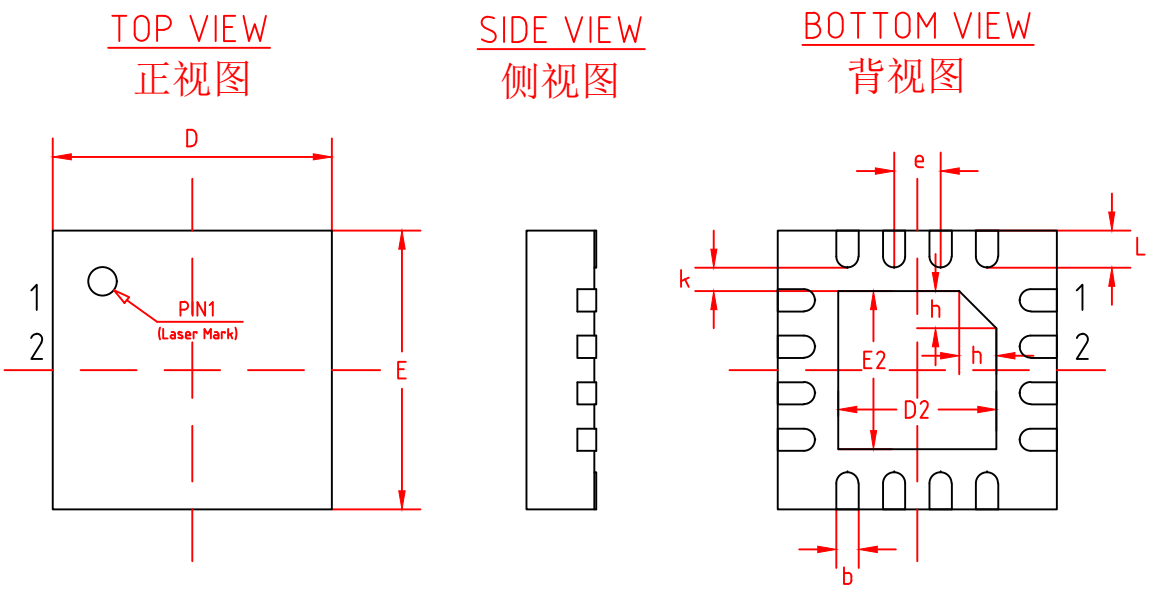


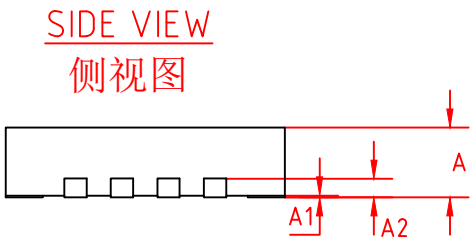
SIDE VIEW
侧视图



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
b	0.23	–	0.31
c	0.19	–	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	0.635 BSC		
h	0.30	–	0.50
L	0.50	–	0.80
θ	0°	–	8°

QFN16-3x3x0.75-P0.5





机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.203 REF	
b	0.18	0.24	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e		0.50 BSC	
D2	1.6	1.7	1.8
E2	1.6	1.7	1.8
K	0.20	0.25	0.30
L	0.30	0.40	0.50
h	0.35	0.40	0.45