

## IRFPF50PBF-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

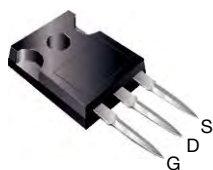
$V_{DS}$ (V)	950	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	2.0
$Q_g$ (Max.) (nC)	190	
$Q_{gs}$ (nC)	23	
$Q_{gd}$ (nC)	110	
Configuration	Single	

#### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


 Available  
**RoHS\***  
 COMPLIANT

TO-247AC



Top View



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	950	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	6.1	A
		T <sub>C</sub> = 100 °C		3.9	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	24	
Linear Derating Factor				1.5	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	800	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	6.0	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	19	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	190	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	1.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	
				1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 40\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 6.1\text{ A}$  (see fig. 12).
- $I_{SD} \leq 6.1\text{ A}$ ,  $dI/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

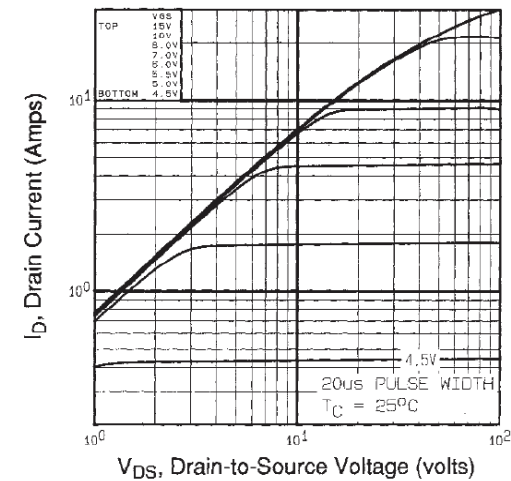
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		950	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	1.2	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 950 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 760 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.6 A <sup>b</sup>	-	2.0	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 3.6 A <sup>b</sup>		5.4	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	2800	-	pF
Output Capacitance	C <sub>oss</sub>			-	250	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	84	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6.1 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	190	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	23	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	110	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 500 V, I <sub>D</sub> = 6.1 A, R <sub>g</sub> = 6.2 Ω, R <sub>D</sub> = 81 Ω, see fig. 10 <sup>b</sup>		-	19	-	ns
Rise Time	t <sub>r</sub>			-	35	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	130	-	
Fall Time	t <sub>f</sub>			-	36	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.1	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	24	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 6.1 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 6.1 A, dI/dt = 100 A/μs <sup>b</sup>		-	630	950	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.5	5.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

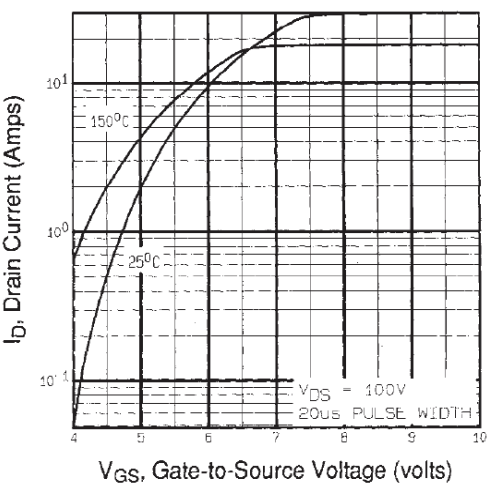
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

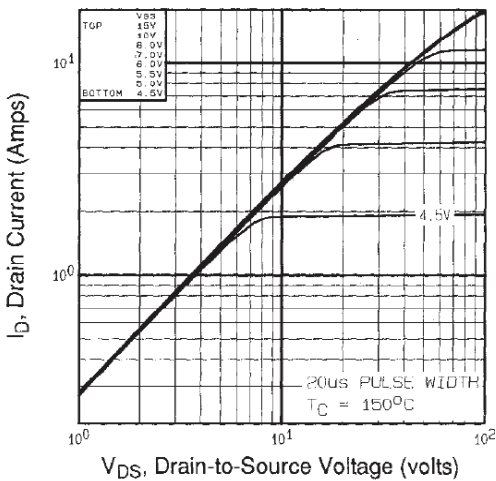
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



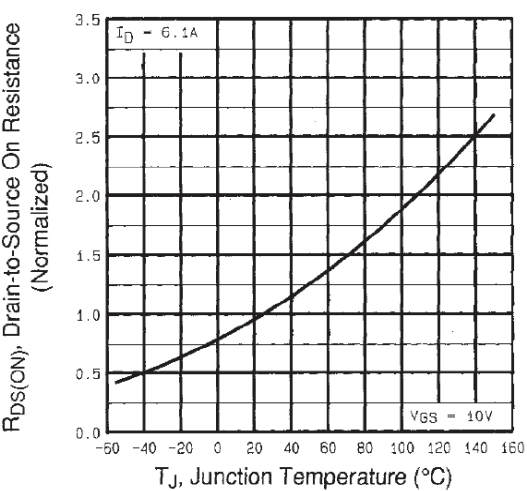
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

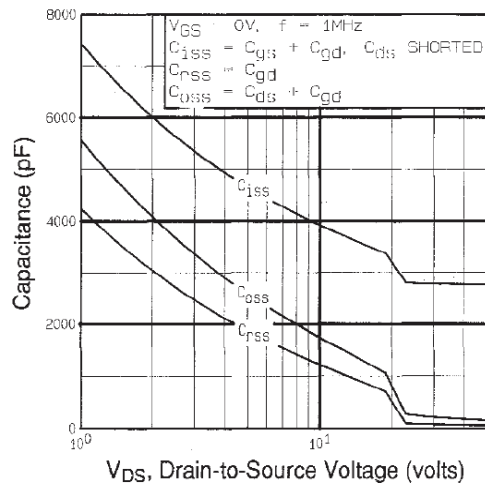


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

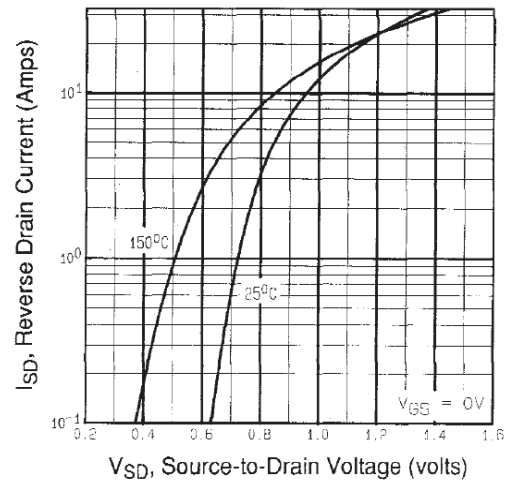


Fig. 7 - Typical Source-Drain Diode Forward Voltage

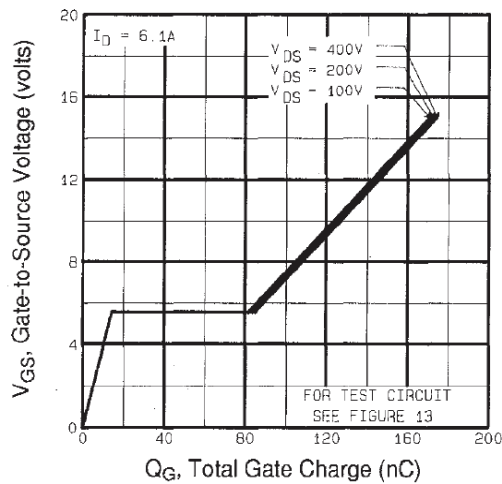


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

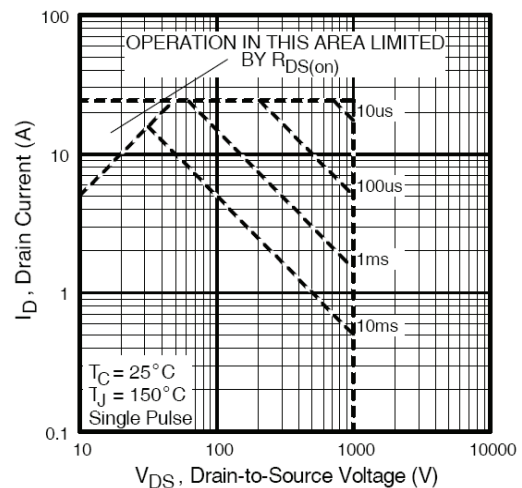


Fig. 8 - Maximum Safe Operating Area

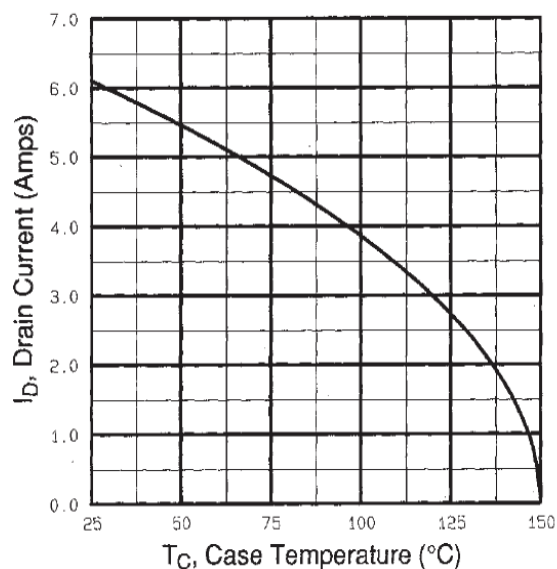


Fig. 9 - Maximum Drain Current vs. Case Temperature

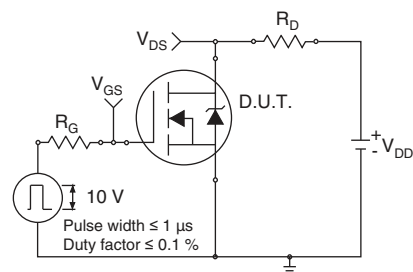


Fig. 10a - Switching Time Test Circuit

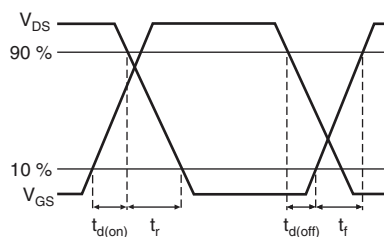


Fig. 10b - Switching Time Waveforms

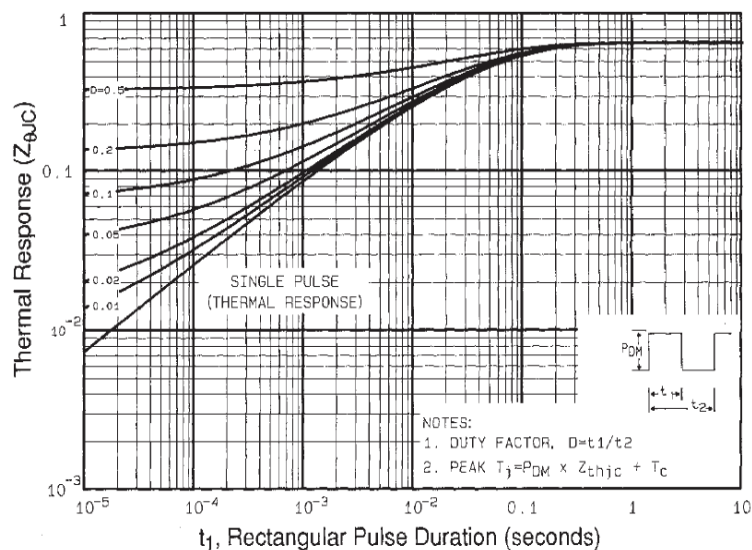


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

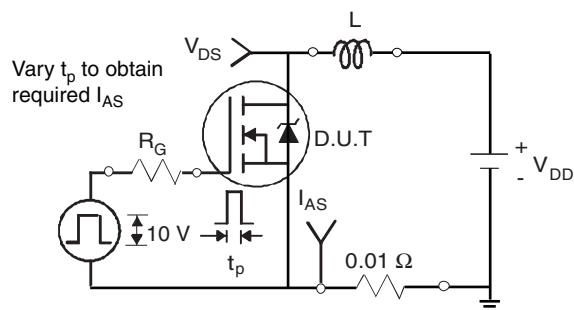


Fig. 12a - Unclamped Inductive Test Circuit

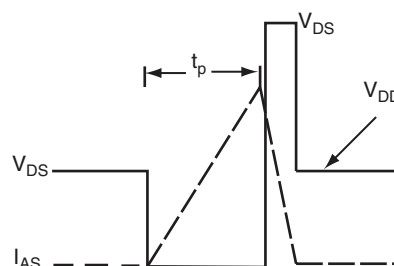


Fig. 12b - Unclamped Inductive Waveforms

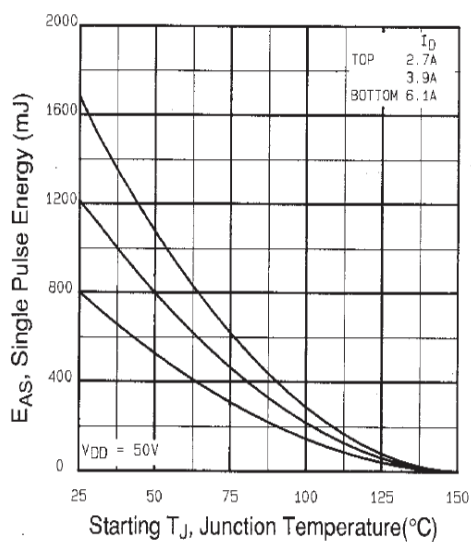


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

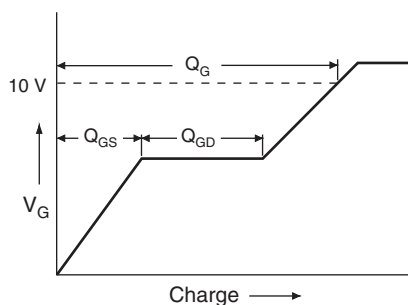


Fig. 13a - Basic Gate Charge Waveform

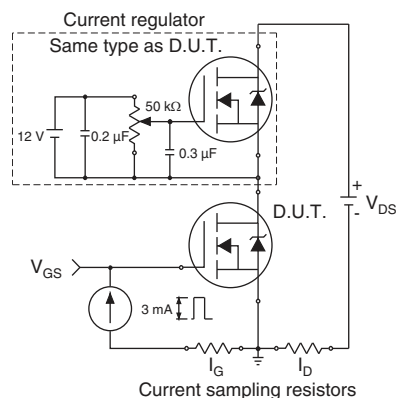
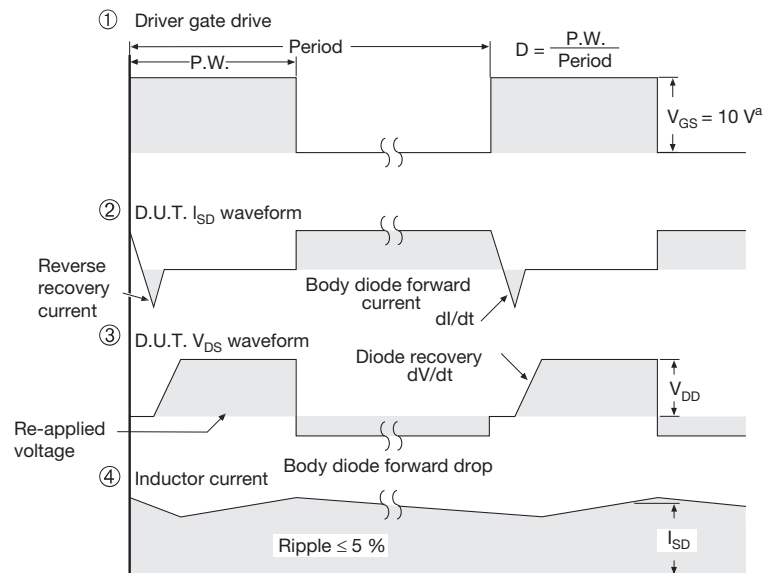
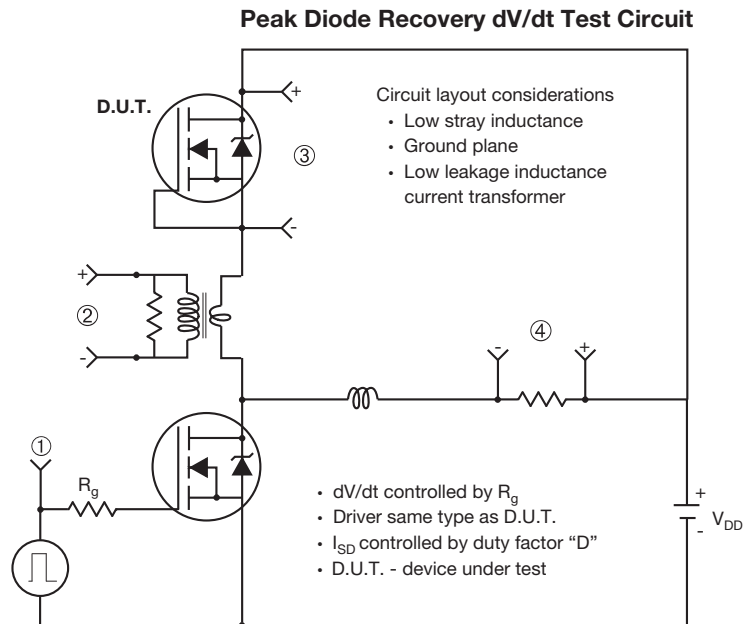


Fig. 13b - Gate Charge Test Circuit

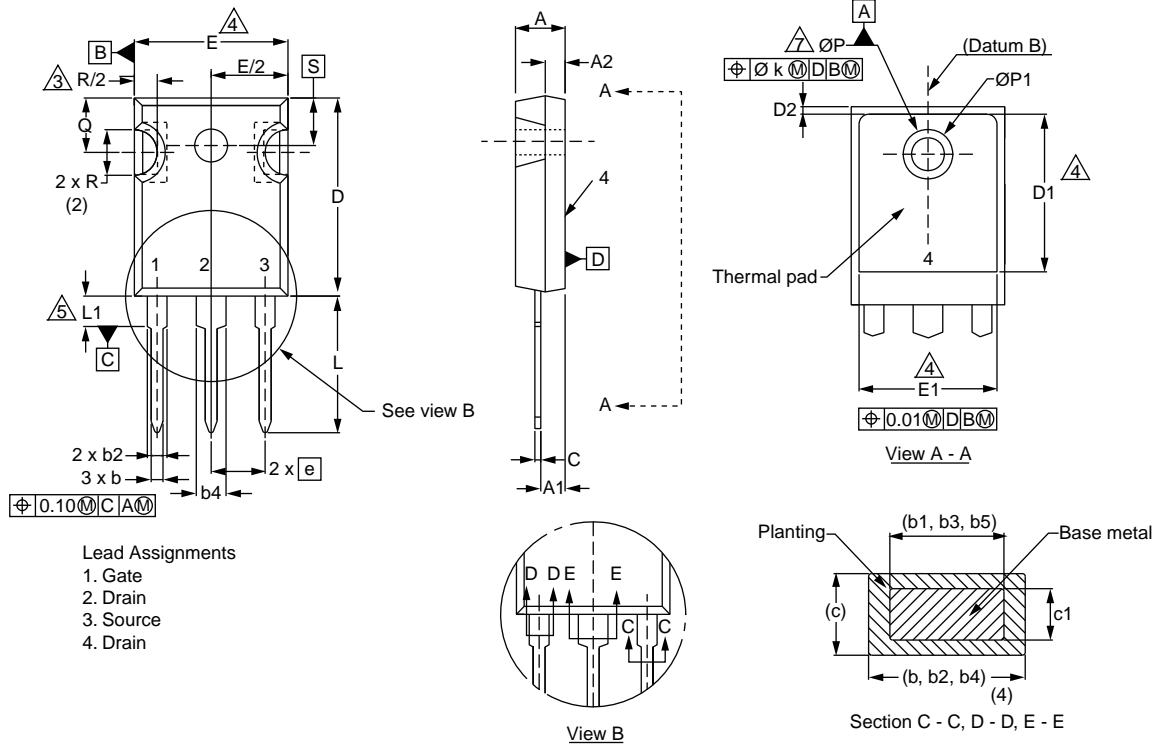


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

## TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	



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