Digital Totem Pole PFC Controller with I2C & UART Interfaces

Hynetek Semiconductor Co., Ltd.

HP1010

FEATURES

Highly flexible digital Totem Pole PFC controller

High flexibility digital PWM

- PWM frequency ranges from 20 kHz to 200 kHz
- PWM soft start during AC line zero-crossing
- Switching frequency spread spectrum for improved EMI

High performance control loop

- 25 MHz sigma-delta ADC for line voltage and current sense, 12.5 MHz sigma-delta ADC for output voltage
- Enhanced dynamic loop response
- Input voltage feedforward to avoid reverse current during AC drop
- Support HVDC input

Multi−mode operations

- Continuous Conduction Mode (CCM) in heavy load Conditions
- Discontinuous Conduction Mode (DCM) in light load conditions
- Burst mode in the zero load conditions

Advanced control functions

- True RMS power metering
- Inrush current control with programming relay delay
- Two channels X-cap discharge during shut down

Extensive fault protections

- Fast over-voltage protection
- Bulk under-voltage protection and over-voltage protection
- External NTC thermal protection
- Cycle−by−cycle current limit
- Average switching current protection
- Built-in 1 kBit MTP to store custom configurations

Low power consumption

I^2C and UART interfaces

Programming via easy-to-use Graphical User Interface (GUI)

Available in QFN-24L packages

-40°C to 125°C operating temperature

APPLICATIONS

Ultra−High Efficiency Power Supplies

LED Lighting

Industrial Power Supplies

Server/Telecom

EV/E-Bike Charger

Supercomputing

Variable-Frequency Drivers (VFD)

GENERAL DESCRIPTION

The HP1010 is a highly flexible digital Power Factor Correction (PFC) controller designed to drive a totem pole PFC power stage.

Totem-pole PFC composes of a fast-leg using the third-generation semiconductor (GaN or SiC MOSFET) switching at PWM frequency and a slow-leg operating at the AC frequency. This design allows for a considerable increase in efficiency and power density by removing the diode bridge that is present at the input of a traditional PFC circuit.

The HP1010 offers RMS values of input voltage, current, and power. Through the I^2C and UART interfaces, this information can be communicated to a microcontroller.

The HP1010 operates from a single 3.3 V supply. The device is available in 4 mm x 4 mm QFN-24L package specified over an ambient temperature range of −40°C to +125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE
HP1010	QFN-24L	4 mm x 4 mm

TYPICAL APPLICATION CIRCUIT

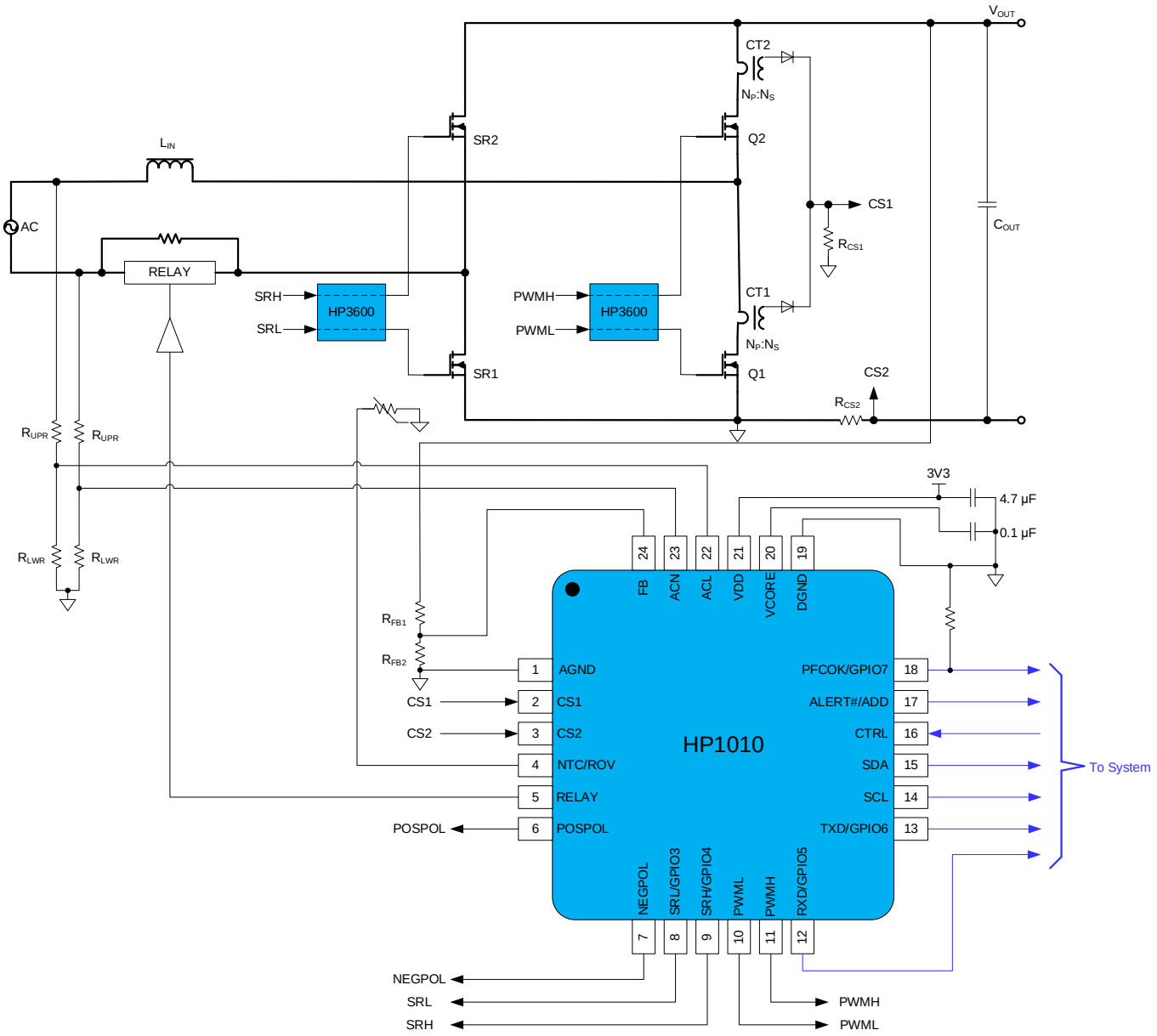

Figure 1 Typical Application Circuit

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REVISION HISTORY

Version	Date	Owner	Descriptions
Rev. 1.0	03/2024	Eric Liu	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

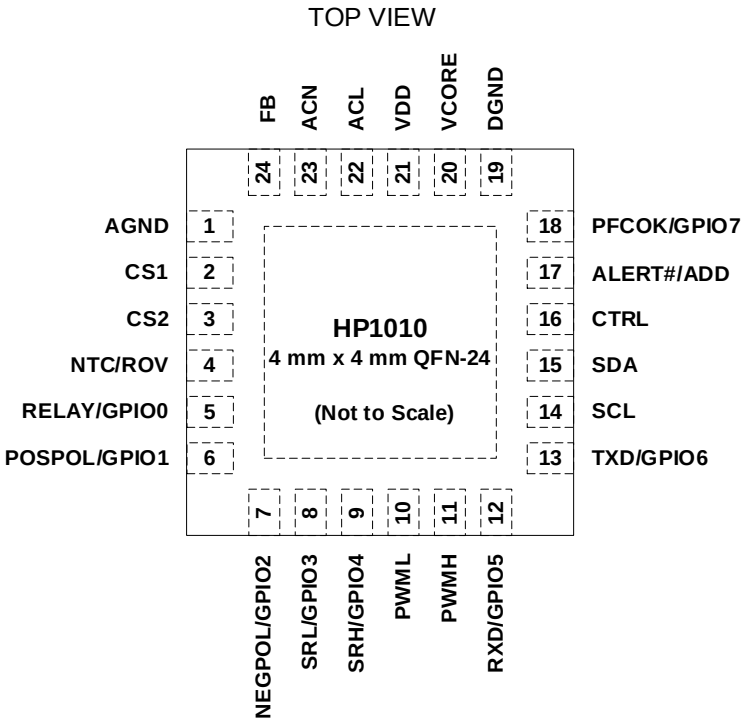


Figure 2 HP1010-BA000-QN24R Pin Assignment

Table 1. Pin Function Descriptions

Pin No.	Name	Type[1]	Description	GPIO
1	AGND	P	Analog ground. AGND should be connected directly to DGND.	
2	CS1	AI	This pin senses the inductor current upslope through current sense transformers in the TPPFC topology. It is used to reconstruct the inductor current. It is also used for cycle−by−cycle current limiting. The signal is referred to AGND.	
3	CS2	AI	The pin optionally senses the inductor current downslope. The signal is referred to AGND.	
4	NTC/ROV	AI	Dual function for this pin. NTC: Temperature sense input, which is inverse proportional to the temperature, triggers the comparator when OTP happens. ROV: redundant OVP comparator with a programmable reference. The signal is referred to AGND.	
5	RELAY/GPIO0	DO	Relay control output. The turn-on delay can be programmed. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
6	POSPOL/GPIO1	DO	Output of the internal AC polarity detection circuit. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
7	NEGPOL/GPIO2	DO	Inverted output of the internal AC polarity detection circuit. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
8	SRL/GPIO3	DO	Control signal for low side slow leg device. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
9	SRH/GPIO4	DO	Control signal for high side slow leg device. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
10	PWML	DO	PWM logic output for control of low side fast leg switch. The signal is referred to DGND.	

Pin No.	Name	Type[1]	Description	GPIO
11	PWMH	DO	PWM logic output for control of high side fast leg switch. The signal is referred to DGND.	
12	RXD/GPIO5	DIO	UART_RX pin. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
13	TXD/GPIO6	DIO	UART_TX pin. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
14	SCL	AIO	I^2C serial clock line. The SCL signal is referred to DGND.	
15	SDA	AIO	I^2C serial data line. The SDA signal is referred to DGND.	
16	CTRL	DI	Remote control pin. The signal is referred to DGND.	
17	ALERT#/ADD	DIO	I^2C alert pin. The signal is referred to DGND. During the power on reset, the state of this pin is sampled as address select input for I^2C bus. Note: a 900 kΩ resistor should be used when connecting to VDD or DGND to reduce standby current. HIGH = I^2C address is 0x67 LOW = I^2C address is 0x47	
18	PFCOK/GPIO 7	DIO	The PFCOK/GPIO supports dual functions. The PFCOK function is held low when the PFC output voltage is out of regulation and during fault conditions. It is a push−pull output. It can be re-used as GPIO pin.	Yes
19	DGND	P	Digital Ground. DGND should be connected directly to AGND.	
20	VCORE	P	1.8 V VDD for digital core. The VCORE signal is referred to DGND. Connect a 100 nF capacitor from VCORE to DGND.	
21	VDD	P	3.3 V main supply input. The VDD signal is referred to AGND. Connect a 4.7 μF capacitor from VDD to AGND.	
22	ACL	AI	AC line voltage sense. The signal is referred to AGND.	
23	ACN	AI	AC neutral voltage sense. The signal is referred to AGND.	
24	FB	AI	PFC output voltage sense for loop regulation. The signal is referred to AGND.	

[1] Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{DD} = 3.3 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25 °C for typical specifications, unless otherwise noted.

Table 2. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Operating Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3	3.3	3.6	V
Supply Current	I_{DD}	Normal operation		10.0		mA
Peak Supply Current	I_{DD_PK}	V_{DD} = 4.0 V while programming			7.5	mA
Shutdown Current	I_{DD_SD}	PFC off state		8.1		mA
Sleep Mode Current	I_{DD_SM}	Sleep mode enabled.		1.0		mA
POWER-ON RESET						
Power-on Reset	V_{DD_POR}	V_{DD} rising	2.7	2.8	2.9	V
UVLO	V_{DD_UVLO}	V_{DD} falling	2.55	2.65	2.75	V
VCORE PIN						
Output Voltage	V_{CORE}	100 nF capacitor connected to DGND	1.7	1.8	1.9	V
OSCILLATOR, CLOCK, PLL						
Oscillator Frequency	f_{OSC}		11.875	12.5	13.125	MHz
PLL Frequency	f_{PLL}		190	200	210	MHz
Digital PWM Resolution	t_{PWM_RES}	For PWML and PWMH pins		5		ns
PWMH, PWML, SRH, SRL, POSPOL, NEGPOL, RELAY PINS						
Output Low Voltage	V_{PWMOL}	Sink current = 10 mA			0.4	V
Output High Voltage	V_{PWMOH}	Source current = 10 mA	V_{DD}-0.4			V
Rise time	t_{RISE}	C_{LOAD} = 50 pF		4.0		ns
Fall time	t_{FALL}	C_{LOAD} = 50 pF		4.0		ns
Output Source Current	I_{OL}		-10			mA
Output Sink Current	I_{OH}				10	mA
SWITCHING FREQUENCY						
Frequency Range	f_{SW}	See Table 8	20		195	kHz
Accuracy			-3		3	%
ACN AND ACL PINS						
External Divider Ratio	$K_{AC\_DIV\_EXT}$			1/200		
Input Voltage Range	V_{AC}		0		2.8	V
Amplifier Gain	G_{AC_OP}			0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Data updating frequency 25 kHz		10		Bits
Voltage Sense Accuracy		10% to 90% of usable range	-1.3		2.0	%FSR
Positive Comparator for VIN On						
Threshold Range[1]	V_{AC_POS}		200	320	480	mV
Threshold Accuracy		Factory trimmed at 320 mV	280	320	355	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution				3		Bits
LSB				40		mV
Hysteresis			30	45	70	mV
Propagation Delay					1.0	μs
Negative Comparator for VIN On						
Threshold Range[1]	V_{AC_NEG}		-480	-320	-200	mV
Threshold Accuracy		Factory trimmed at -320 mV	-340	-318	-297	mV
Resolution				3		Bits
LSB				40		mV
Hystersis Width				40		mV
Propagation Delay					1.0	μs
Positive Comparator for Surge						
Threshold Range[1]	V_{AC_PSUR}		1.6	1.9	2.2	V
Threshold Accuracy		Factory trimmed at 1.9 V	-2.32		1.16	%
Resolution				4		Bits
LSB				40		mV
Hysteresis			110	135	165	mV
Propagation Delay					1.0	μs
AC Line Frequency Monitor						
High Threshold	f_{5060_H}		68	70	72	Hz
Lower Threshold	f_{5060_L}		37	40	43	Hz
Detection Timer	N_{LINE_DET}			4		cycles
Exceed Timer	$N_{LINE\_FREQ\_EXC}$			4		cycles
Brown-out and SAG						
Vin On Threshold	V_{IN_ON}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	0	78	255	VAC
Vin Off Threshold	V_{IN_OFF}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	0	71	255	VAC
Brown-out Debounce	t_{BO_DEB}		-	0.5	-	cycles
Line Sag Timeout Range	t_{SAG_TO}	Programmable 4 to 32 AC cycles	4	12	32	cycles
High/Low Line Detection						
High Threshold	V_{HLINE}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	120	168	180	VAC
Low Threshold	V_{LLINE}	Programmable, $K_{AC\_DIV\_EXT}$=1/200	120	156	180	VAC
High Line to Low Line Debounce Time	t_{H2L_DED}		20	25	30	ms
VAC ZERO CROSSING DETECTION						
VAC Zero Detection Comparator		Between ACL Pin to ACN pin				
Threshold	V_{POL_DET}		-0.01	0	0.01	V
Hysteresis Width	V_{POL_HYS}			10		mV
Propagation Delay	t_{POL_PD}				1.0	μs
Digital Polarity Detection						
Digital Propagation Delay				5		μs
VIN_POL Detection Debounce	t_{POL_DEB}		20	200	320	μs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN_POL Detection LSB				20		µs
Main PWM Drive Control						
Main PWM On Threshold	V_{PWM_ON}		0		66	V
Main PWM Off Threshold	V_{PWM_OFF}		0		66	V
SYNC PWM Drive Control						
SYNC On Threshold	V_{SYN_ON}		0		66	V
SYNC Off Threshold	V_{SYN_OFF}		0		66	V
Slow Leg (SR) Drive Control						
SR On Threshold	V_{SR_ON}		0		66	V
SR Off Threshold	V_{SR_OFF}		0		66	V
SYNC PWM Drive Control 2						
SYNC On Threshold	$I_{SYN\_ON\_CS}$	Low-line Mode	0.2		3.5	A
		High-line Mode	0.1		1.75	A
SYNC Off Threshold	$I_{SYN\_OFF\_CS}$	Low-line Mode	0.2		3.5	A
		High-line Mode	0.1		1.75	A
Slow Leg (SR) Drive Control 2						
SR On Threshold	I_{SRON_CS}	Low-line Mode	0.2		3.5	A
		High-line Mode	0.1		1.75	A
SR Off Threshold	I_{SROFF_CS}	Low-line Mode	0.2		3.5	A
		High-line Mode	0.1		1.75	A
FB PIN						
External Divider Ratio	$K_{FB\_DIV\_EXT}$			1/200		
Input Voltage			0		2.8	V
Input Impedance			500			kΩ
Amplifier GBW				2		MHz
Amplifier Gain				0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				12.5		MHz
Equivalent Resolution				11		Bits
Voltage Sense Accuracy		10% to 90% of usable range	-1.3		1.5	%FSR
Fast Over-Voltage Protection						
Threshold Range[1]	$V_{FB\_FOV\_LIM}$		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-0.86		1.64	%
Resolution				6		Bits
Hysteresis			110	135	160	mV
Propagation Delay	$t_{FB\_FOV\_PD}$				160	ns
Debounce Time	$t_{FB\_FOV\_DB}$	Programmable in 4 steps	40		100	µs
Blanking time	$t_{FB\_FOV\_BK}$			10		µs
Open Loop Protection						
Sink Current	I_{FB_SNK}			250		nA
Threshold	V_{FB_OL}		20		88	V
Hysteresis	V_{FB_OLHYS}			18		V
Debounce Time	t_{FB_OLDB}	Programmable in 4 steps	0		30	ms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slow Over-Voltage Protection						
Threshold	$V_{FB\_SOV\_LIM}$		V_{REF}		V_{REF}+68	V
Resolution				5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SOV\_DB}$		0		30	ms
Slow Under-Voltage Protection						
Threshold			V_{REF}-68		V_{REF}	V
Resolution	$V_{FB\_SUV\_LIM}$			5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SUV\_DB}$		0		30	ms
CS1 AND CS2 PINS						
Input Voltage			0		1.4	V
Input Impedance			1			MΩ
Amplifier						
GBW				2		MHz
Gain				1		
ADC						
High Input Voltage Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Updating frequency at 100 kHz		8		Bits
Current Sense Accuracy		10% to 90% of usable range	-1.5		2.0	%FSR
CS1 Fast Over Current Protection						
Threshold Range[1]	$V_{CS1\_OC\_LIM}$		1.0	1.25	1.5	V
Threshold Accuracy		Factory trimmed at 1.25 V	-1.2		0.48	%
Resolution				6		Bits
LSB				7.8		mV
Hysteresis			15	25	35	mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	480		1920	ns
Debounce Time		Programmable in 4 steps	40		160	ns
CS2 Zero Crossing Detection						
Threshold Range[1]	V_{CS2_ZCD}		-100	22.4	48	mV
Threshold Accuracy		Factory trimmed at 22.4 mV	12.5	22.4	33.5	mV
Resolution				6		Bits
LSB				3.2		mV
Hysteresis			35	50	75	mV
Propagation Delay					100	ns
CTRL PIN						
Input High Voltage	V_{CTRL_IL}				0.8	V
Input Low Voltage	V_{CTRL_IH}		2.0			V
Debounce Time	t_{CTRL_DEB}			10		μs
Leakage Current	i_{CTRL_LK}				1.0	μA
PFCOK PINS						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low Level					0.8	V
Output High Level			2.0			V
Debounce Time			0		600	ms
OVER AVERAGE SWITCHING CURRENT PROTECTION						
Average OCP Threshold		CS1 Sense ratio is 10:1	0		7	A
Resolution				7		Bits
Accuracy			-2		+2	%
Debounce				2		Switch cycle
NTC/ROV PIN						
Current Source	I_{NTC}		43	46	49	μA
Over-temperature Threshold	V_{NTC_OT}		0.36	0.4	0.41	V
OT Recover Threshold	V_{NTC_REC}		0.78	0.8	0.82	V
Debounce Time	t_{NTC_DEB}	Programmable in 2 steps		500	1000	ms
Redundant Over-Voltage Protection						
Threshold Range[1]	V_{ROV_LIM}		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-2.00		1.64	%
Resolution				6		Bits
Hysteresis			115	135	160	mV
Propagation Delay					160	ns
Debouncing Time		Programmable in 4 steps	40		100	μs
Blanking Time				10		μs
SDA/SCL PINS						
Input Voltage Low					0.8	V
Input Voltage High			2.2			V
Output Voltage Low					0.4	V
Pull-Up Current			100		350	μA
Leakage Current			−5		+5	μA
SERIAL BUS TIMING						
Clock Frequency	f_{IIC}				400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			μs
Start Setup Time	t_{SU_STA}		4.7			μs
Start Hold Time	t_{HD_STA}		4			μs
SCL Low Time	t_{LOW}		4.7			μs
SCL High Time	t_{HIGH}		4			μs
SCL, SDA Rise Time	t_{R_I2C}				1000	ns
SCL, SDA Fall Time	t_{F_I2C}				300	ns
Data Setup Time	t_{SU_DAT}		250			ns
Data Hold Time	t_{HD_DAT}		300			ns
TXD/RXD PINS (UART)						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Baud Rate	f_{UART}	Programmable with (0:9600; 1: 1200; 2: 57600; 3: 115200)	1200	9600	115200	bps
Data Length				8		
Stop Bits				1		
Polarity Check Bit				1		
EEPROM RELIABILITY						
Endurance		T_A = 85°C	10,000			Cycles
		T_A = 125°C	1000			Cycles
Data Retention		T_A = 85°C	20			Years
		T_A = 125°C	15			Years

[1] The final range of thresholds will be determined by factory trimmed result.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum ratings

Parameter	Rating
VDD (Continuous)	4.2 V
ACL, ACN, FB, CS1, CS2, RELAY/GPIO0, NTC/ROV, POSPOL/GPIO1, NEGPOL/GPIO2, SRL/GPIO3, SRH/GPIO4, PWML, PWMH, RXD/GPIO5, TXD/GPIO6, SCL, SDA, CTRL, PFCOK/GPIO7	-0.3 V to V_{DD} + 0.3 V
VCORE	2 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	±6000 V
Charge Device Model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN4x4-24L	46	23	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

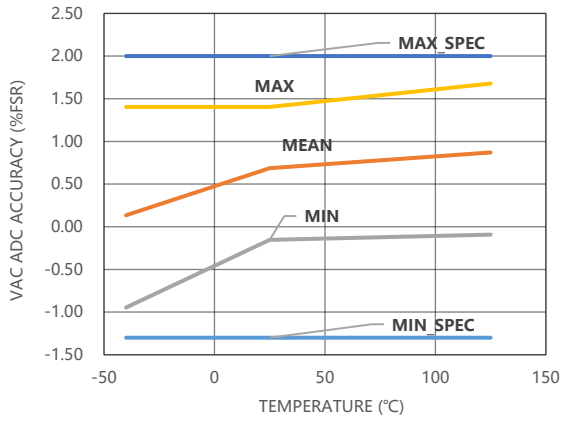


Figure 3 VAC ADC Accuracy vs. Temperature (from 10% to 90%)

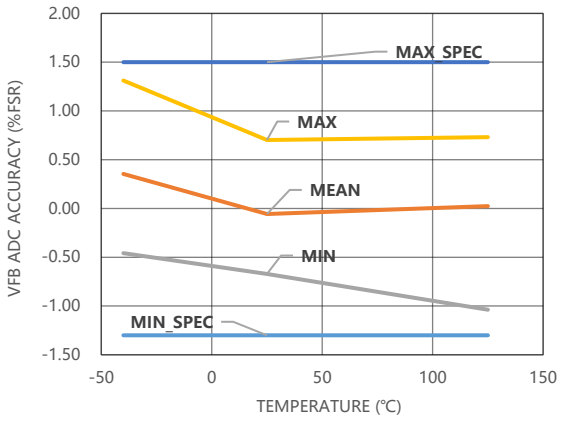


Figure 4 VFB ADC Accuracy vs. Temperature (from 10% to 90%)

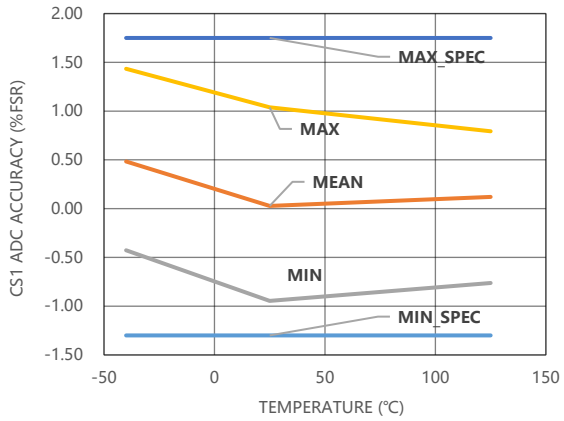


Figure 5 CS1 ADC Accuracy vs. Temperature (from 10% to 90%)

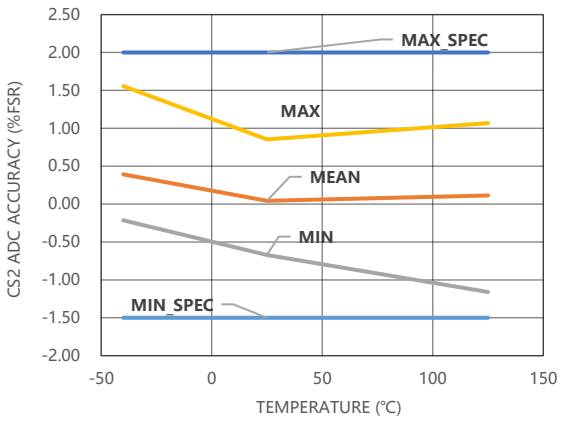


Figure 6 CS2 ADC Accuracy vs. Temperature (from 10% to 90%)

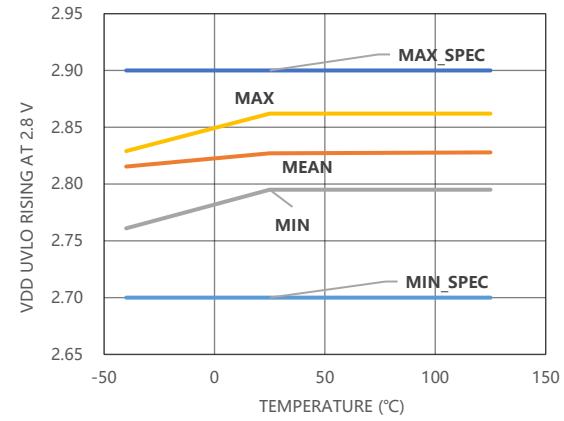


Figure 7 VDD UVLO Rising at 2.8 V vs. Temperature

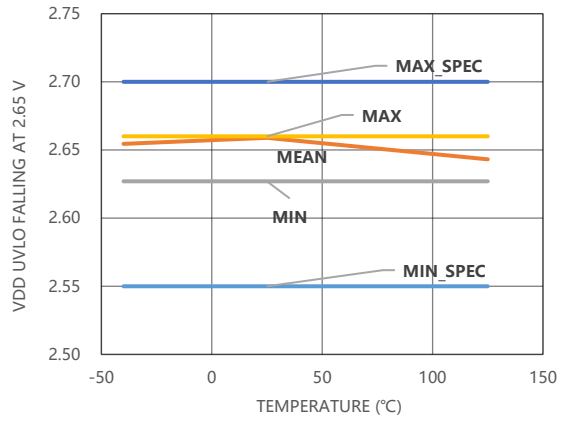


Figure 8 VDD UVLO Falling at 2.65 V vs. Temperature

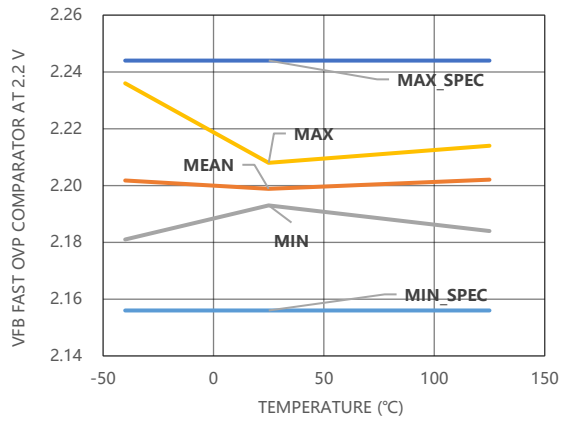


Figure 9 VFB Fast OVP Comparator at 2.2 V vs. Temperature

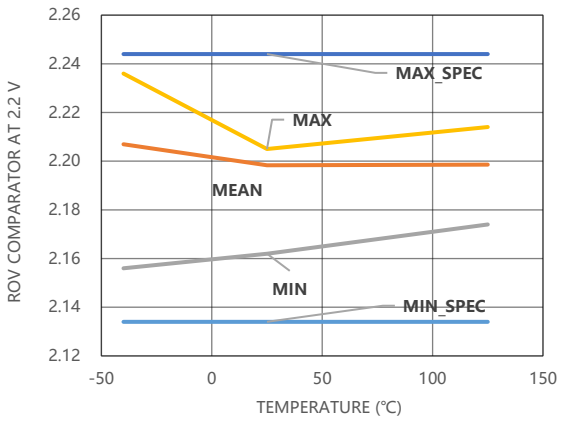


Figure 10 ROV Comparator at 2.2 V vs. Temperature

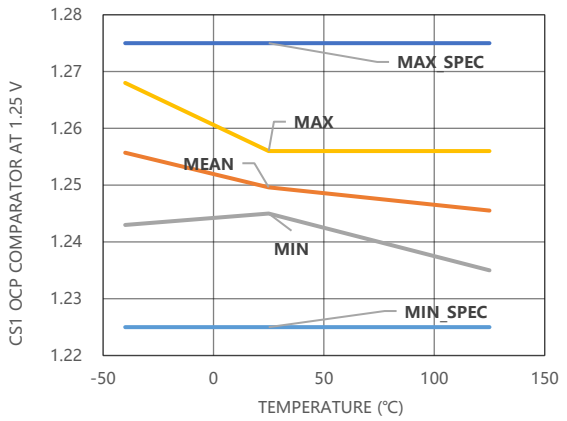


Figure 11 CS1 OCP Comparator at 1.25 V vs. Temperature

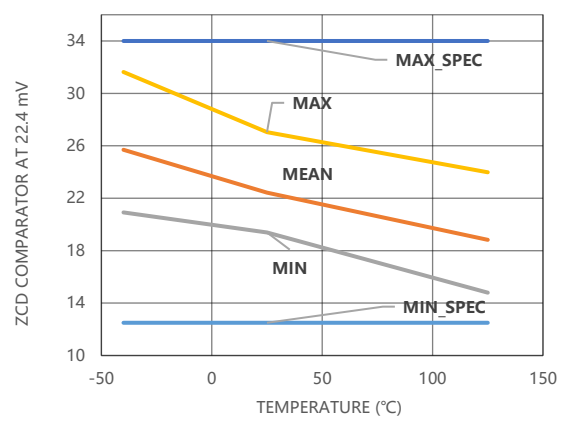


Figure 12 CS2 ZCD Comparator at 22.4 mV vs. Temperature

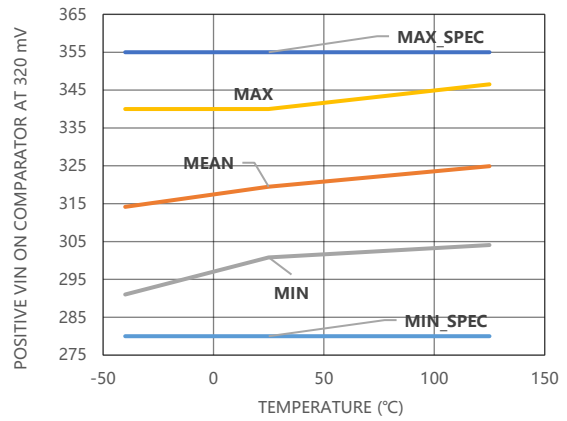


Figure 13 Positive VIN ON Comparator at 320 mV vs. Temperature

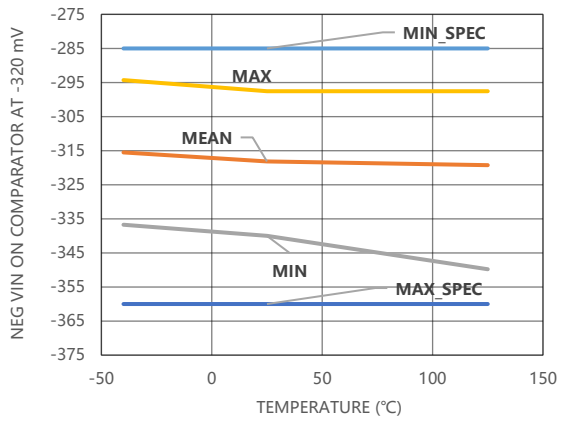


Figure 14 Negative VIN ON Comparator at -320 mV vs. Temperature

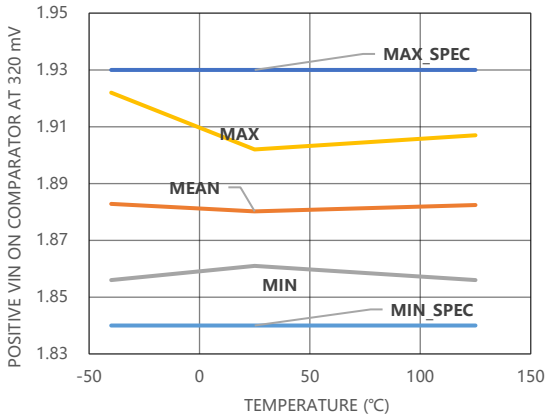


Figure 15 Positive Surge Comparator at 1.9 V vs. Temperature

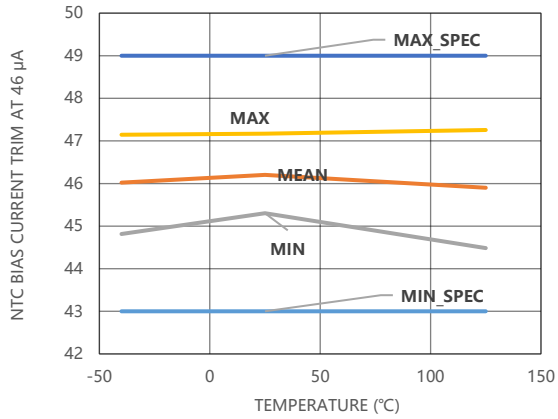


Figure 16 NTC Bias Current at 46 µA vs. Temperature

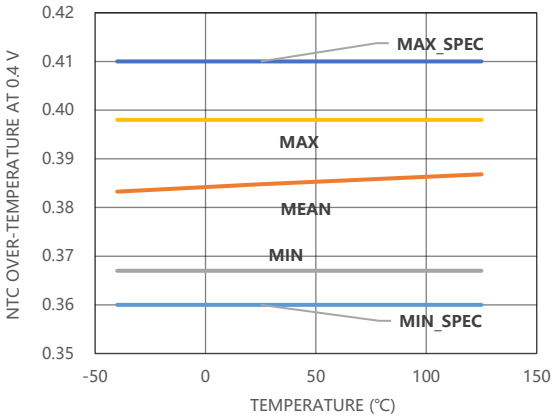


Figure 17 NTC Over-Temperature at 0.4 V vs. Temperature

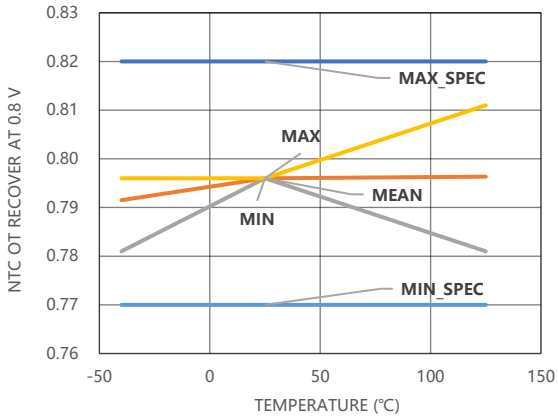


Figure 18 NTC Over-Temperature Recover at 0.8 V vs. Temperature

THEORY OF OPERATION

Figure 19 shows the overall control diagram for the totem-pole power factor correction (TPPFC) with MOSFET for synchronized line rectification. The voltage and current loop control are the same as conventional boost PFC converter. The feedback signals from the PFC power stage are the V_{FB}, V_{ACL}, V_{ACN}, I_{CS1} and I_{CS2}. The input voltage polarity and RMS value are determined from V_{ACL} and V_{ACN}. The outer voltage loop output multiplied by |VAC| gives sinusoidal current reference. Current loop gives the proper duty-ratio for boost circuit. The polarity determines how the PWM signal is distributed for switches Q1 and Q2. The soft-start duty ratio is used for a short period after the zero-crossing.

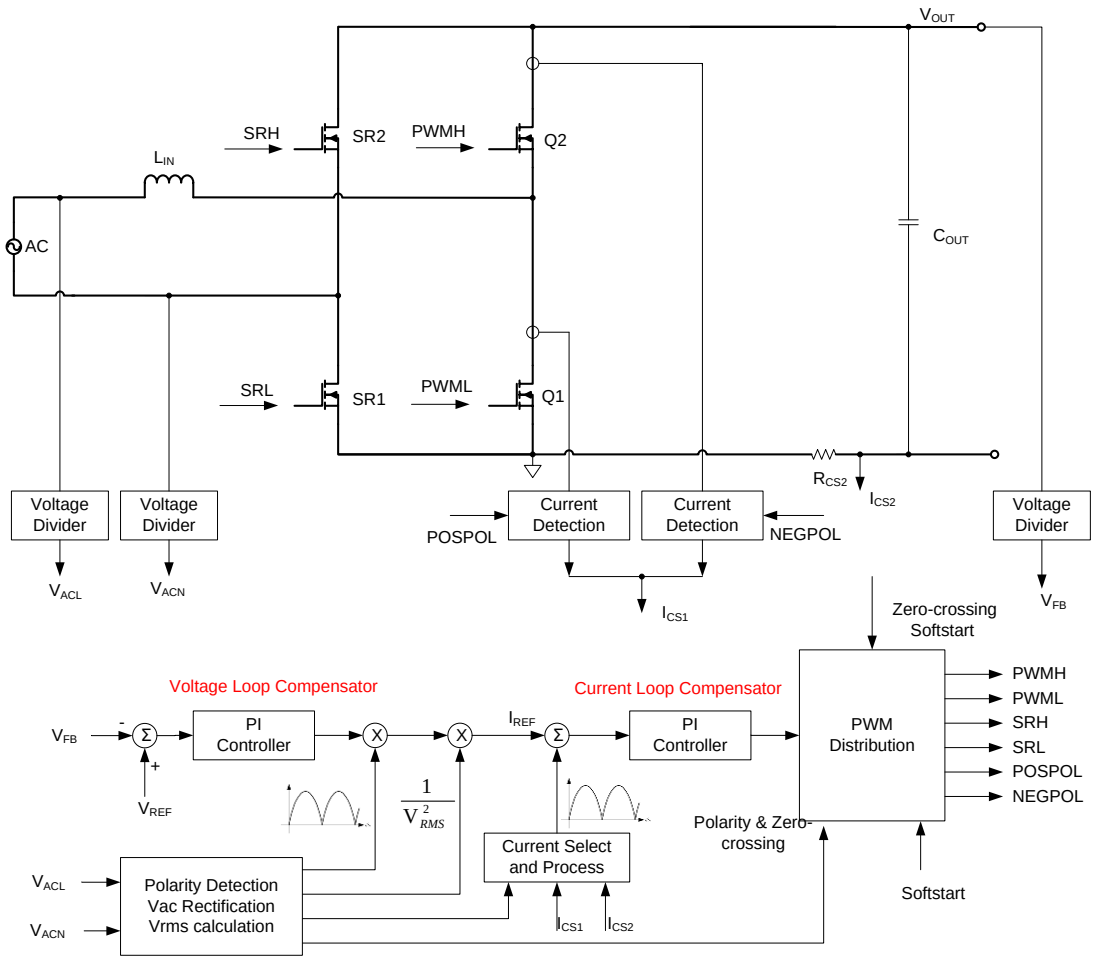


Figure 19 HP1010 Control Loop Scheme

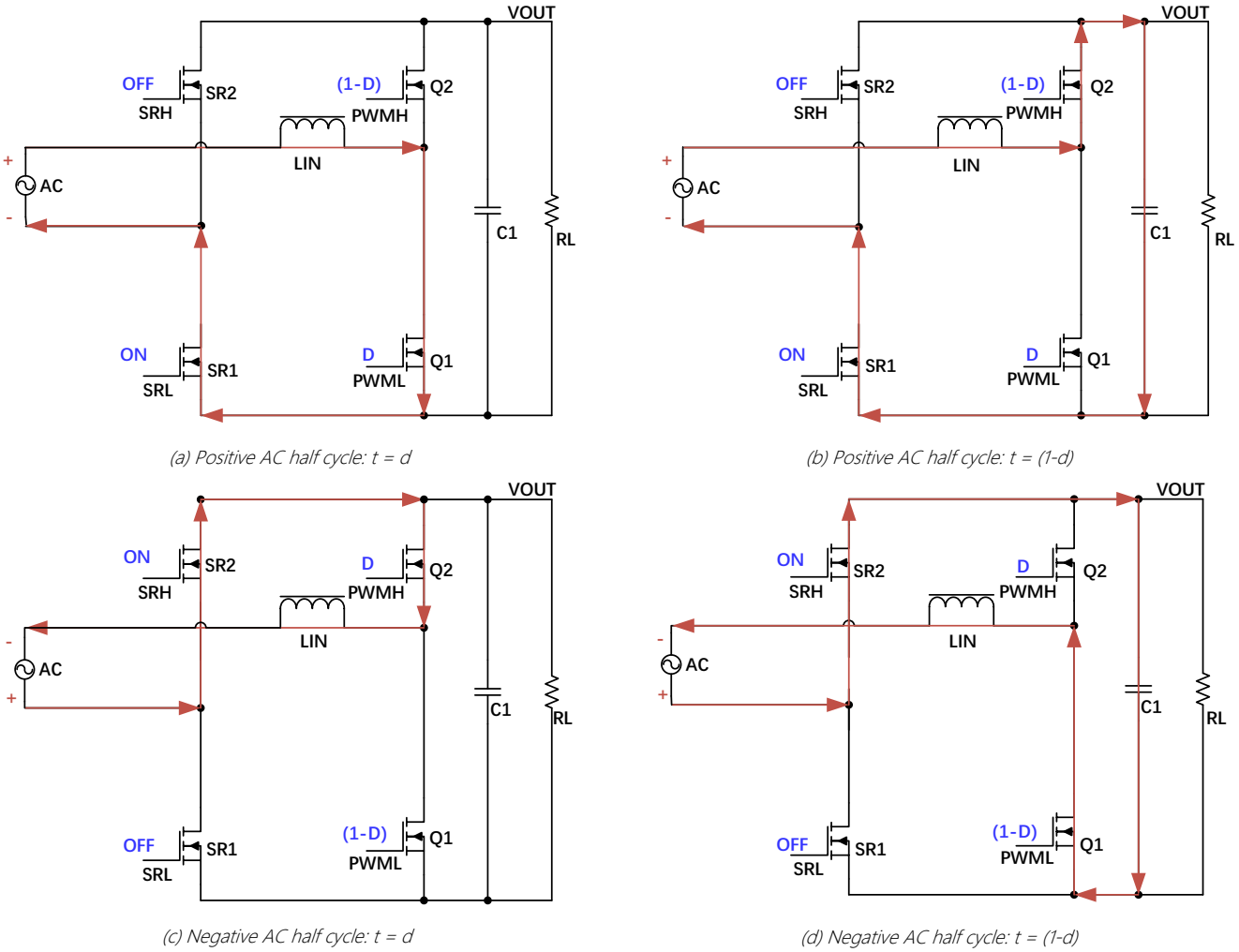
BASIC OPERATING PRINCIPLE

The Totem-Pole PFC topology operates in two modes depending on the polarity of input AC voltage, as shown in the Figure 20. During the positive half cycle (line > neutral): Q1 is the main switch and Q2 is driven with a complementary PWM signal. Q1/Q2 and L_{IN} form the boost DC/DC stage. During this positive half cycle, half bridge leg SR1 is turned on and SR2 is always inactive. During the time when the main switch Q1 is turned on, current flows from L_{IN} ->Q1->SR1 and back to neutral. During the period of (1-d) when Q1 is turned off, Q2 is turned on and current flows through Q2 and back to N via SR1. The DC bus ground VDC- is tied to neutral potential as SR1 is conducting all the time.

During negative half cycle (neutral > line): the operation in the negative half cycle is similar except the role of top and bottom switches are swapped. Now Q2 becomes the main switch and Q1 is free-wheeling, and SR2 is turned on and SR1 is inactive.

Compared to the conventional bridgeless PFC, the TPPFC has the following advantages:

- Improved efficiency: main current only flows through two switches at a time. Q1/Q2 are driven synchronously with complimentary PWM signals and the SR1/SR2 on the slow line frequency legs can be low Rds(on) Si MOSFETs to further reduce the conduction loss.
- Lower part counts, higher power density and lower BOM cost. It uses fewer parts and has a simpler circuit: It needs only one inductor and neither SiC diodes nor AC return diodes are required.
- Bidirectional power flow. TPPFC is inherently capable of bidirectional operation, which is ideal for applications which may require power flow in both directions, such as Energy Storage System (ESS) and on-board bidirectional battery chargers (OBC).



(a) Positive AC half cycle: t = d

(b) Positive AC half cycle: t = (1-d)

(c) Negative AC half cycle: t = d

(d) Negative AC half cycle: t = (1-d)

Figure 20 Totem-pole PFC Operation

VDD AND VCORE PINS

When the voltage of the VDD pin is applied (VDD), there is a delay before the part can regulate the power supply. When VDD voltage rises above the power-on reset and UVLO levels, it takes ~20 μs for the VCORE pin (Pin 23) to reach its operational point of 1.8 V. The EEPROM contents are then downloaded to the registers. After the EEPROM contents are downloaded, the HP1010 is ready for operation; however, it takes a maximum of 20 ms for the HP1010 to complete initialization of the address after a power-on reset. Therefore, it is recommended that the master device access the HP1010 at least 20 ms after power-on reset.

CTRL PIN AND SOFTWARE ENABLE

The HP1010 is in the PFC off state upon power-on reset. PFC_ON configuration can be enabled in one of four ways, depending on the setting:

- Always on whenever the input voltage is ready.
- Hardware CTRL only. Power on whenever the CTRL pin is pulled high, and the input voltage is ready.
- Software ENABLE only. Power on whenever the ENABLE bit is set and the input voltage is ready.
- Both hardware CTRL being pulled high, and software ENABLE bit being set to turn on the PFC when the input voltage is ready.

Once the PFC_ON flag is set, the HP1010 follows the state machine as shown in section Operation for details.

The CTRL pin has a control debounce of t_{CTRL_DEB}, which is 10 μs, for both the rising edge and falling edge. The CTRL pin is used to control the HP1010 from the second side controller via an optical coupler, as shown in Figure 21. The remote signal is generated from the second-side controller.

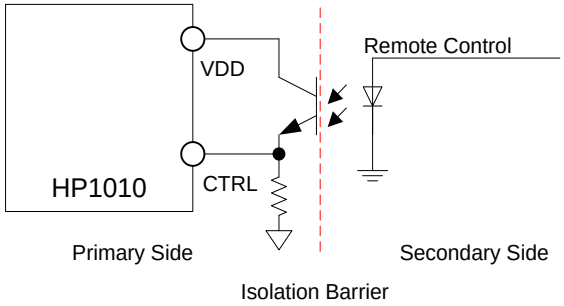


Figure 21 Remote Control Signal to Enable HP1010

INPUT AC VOLTAGE (ACL AND ACN PINS)

External resistor dividers are required to divide down two high voltage nodes to perform differential line sensing. The recommended divide down factor for universal input consumer applications is $K_{AC\_DIV\_EXT}$, typically 1/200.

$$K_{AC\_DIV\_EXT} = \frac{R_{LWR}}{R_{UPR}+R_{LWR}} \quad (1)$$

The ACL pin is intended to interface with the low-frequency node of the main boost inductor, L_{IN}, and the ACN pin is intended to interface with the bridge voltage of the slow-leg power switches. The internal line detector circuit is designed with substantially high input impedance, allowing for large external resistors to minimize the power dissipation in the dividers, enabling the application to achieve low no-load power consumption. Typical values for R_{UPR} can be in the range of 993 kΩ, while R_{LWR} can be 4.99 kΩ. In practice, the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

Since there is an additional amplifier U2 with a gain of $K_{AC\_DIV\_INT}$ = 1/2. The total gain of line voltage sense to the ADC is:

$$K_{AC\_DIV} = K_{AC\_DIV\_EXT} \times K_{AC\_DIV\_INT} \quad (2)$$

Therefore K_{AC_DIV} = 1/400.

POLARITY DETECTION

The ACL and ACN pins sense signals are compared directly against each other to determine when they cross. The crossover of the two signals indicates that the AC line voltage has changed polarity. When the AC line is in a positive cycle, POSPOL is high and NEGPOL signal is low. When the AC line is in a negative cycle, POSPOL is low and NEGPOL signal is high.

External filter capacitance may be needed to improve the noise immunity of the polarity detection circuitry; the recommended time constant of the RC filter is about 20 to 200 μs, enough to provide noise immunity from the switching frequency of the power supply but not such a large time constant to introduce significant lag in the line sense signals.

The output of the polarity comparison circuit is passed through a digital debounce filter, which will provide additional immunity if the comparison circuit is toggling due to the noise. The debounce filter has a programmable debounce time, typical 200 μs.

AC LINE FREQUENCY MONITORING

The HP1010 supports different input line types, including 50 Hz/ 60 Hz AC input and DC input.

BROWN−OUT AND LINE SAG PROTECTION

The HP1010 features line voltage Brown−out (BO) and Line sag (SAG) detection. These detection circuits' function works as a line voltage UVLO, enabling drive pulses when the RMS voltage exceeds the V_{IN_ON} threshold, typically 78 VAC, and disabling drive pulses when the line voltage falls below the V_{IN_OFF} threshold, typically 71 VAC, for a given timer duration.

When the line voltage VAC voltage drops below VIN_OFF for a debounce of t_{BO_DEB}, which is half an AC cycle, the BROWN-OUT flag is trigged. The SAG timer, programmable from 4-cycle to 32-cycle from the BROWN-OUT flag being triggered, allows the application to sustain a line voltage dropout for a single or multiple AC line cycles while the controller continues to deliver drive pulses. Within the timer, if the output voltage drops below the output under-voltage limit, the VOUT_UV_FAULT will trigger protection action. If the input current exceeds the input peak current limit or the input average current limit, the IIN_PK_OC fault or the IIN_AV_OC fault will trigger protection actions. If the protection action is selected as fault recovery, since the BROWN_OUT flag is triggered, the HP1010 resets to Mode 0. If the SAG timer expires, the controller will reset to Mode 0 for a new start-up. Figure 22 shows the timing diagram for the Brown-out and SAG. The missing cycle between t_1 to t_0 is smaller than t_{BO_DEB}, the BROWN_OUT flag is not triggered.

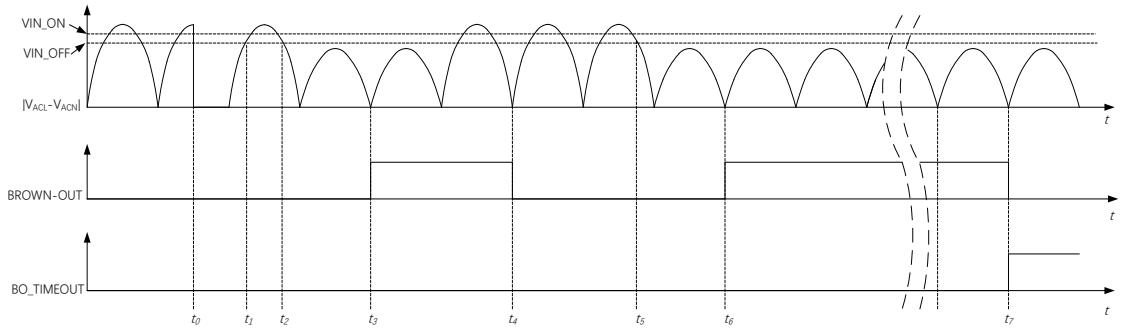


Figure 22 Brown-out and Sag Timing Diagram

LINE RANGE DETECTION

The HP1010 features input voltage range detection, which distinguishes between high line (nominally 230 VAC) and low line (nominally 115 VAC) input voltages. The input voltage range is detected based on the RMS value calculated with the VAC line signal. By default, the controller will power up into low line mode. If VAC exceeds the high line threshold, V_{HLINE}, typically 168 V, for one half cycle, the controller transitions to high line mode. Once in high line mode the peak line voltage must fall below V_{LLINE}, typically 156 VAC, to enter back into the low line mode for one half cycle. The debounce duration, t_{H2L_DEB}, typically 25 ms is set long enough to allow the controller to remain in high line mode in the event of a single line cycle dropout.

AC ZERO CROSSING MANAGEMENT

AC zero crossing management is the feature in the HP1010 that determines when to enable and disable the various drive signals at the beginning and end of each of the half line cycles. This feature is critical to the robustness and performance of the TPPFC topology. The 4 drive signals that can be divided into three classes: 1) The primary or *d* controlled PWM drive signal; 2) The synchronous (sync) PWM drive signal that occurs during the (1 − *d*) portion of the switching period; and 3) The slow leg "rectifier" or SR drive signal that switches once per half line cycle. Each drive signal has a respective stop and start threshold, which is a function of the line voltage amplitude, $|V_{ACL}-V_{ACN}|$.

OPEN LOOP DRIVE PULSES

Another critical feature of the HP1010 is the open-loop drive pulses that are issued immediately following a polarity transition. After the AC line zero crossing, the slow leg bridge maintains a residual voltage charge from the previous half line cycle and must be transitioned from V_{OUT} to 0 V (or vice versa) during the upcoming half line cycle.

Considering that PWM-controlled drive pulses near an AC line zero crossing would typically operate with a high duty cycle, using these pulses to transition the slow bridge voltage can result in excessively high current spikes in the

inductor; hence, it is beneficial to use shorter drive pulses with a smaller, fixed duty cycle to initiate the slow leg bridge node transition.

OUTPUT VOLTAGE (FB PIN)

REGULATION BLOCK

The bulk voltage is divided down via a resistor divider and input to an ADC, which converts the feedback voltage to a digital signal. This digital signal compares against a digital reference voltage. The recommended divide-down factor for universal output voltage sense is K_{FB_DIV}, typically 1/200.

$$K_{FB\_DIV\_EXT} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \quad (3)$$

Typical values for R_{FB1} can be in the range of 993 kΩ while R_{FB2} can be 4.99 kΩ. In practice the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

Since there is an additional amplifier with a gain of $K_{FB\_DIV\_INT}$ = 1/2. The total gain of output voltage sense to the ADC is:

$$K_{FB\_DIV} = K_{FB\_DIV\_EXT} \times K_{FB\_DIV\_INT} \quad (4)$$

Therefore K_{FB_DIV} = 1/400. During nominal condition, the output voltage is 400 V, resulting in FB pin sense voltage of 2 V and ADC input voltage of 1 V.

OUTPUT VOLTAGE REGULATION

In the HP1010, the output voltage can be regulated with a low line and a high line separately. As low-line and high-line references, the regulation range is from 250 V to 505 V, with a nominal voltage of 400 V.

OUTPUT VOLTAGE PROTECTION FEATURES

The HP1010 features multiple protection and enhancement features for improved performance and robustness of the application. The slow OVP, fast OVP, slow UVP, and fast loop blocks monitor the sampled FB pin voltage.

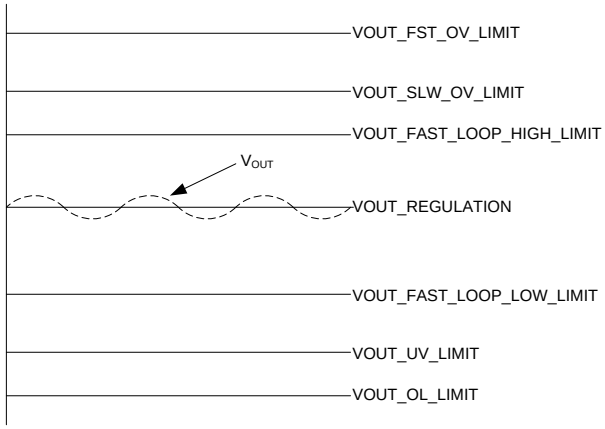


Figure 23 Output Voltage Protection Thresholds

CURRENT SENSE (CS1 AND CS2 PINS)

CURRENT SENSE METHODS

In CCM mode, the HP1010 implements average current mode control that requires the controller to receive an accurately sensed average value of the inductor current. This is a challenge with the TPPFC topology because the inductor and each of the fast leg switches conduct current bidirectionally, as shown in Figure 24. Depending on the line cycle polarity, the inductor current flows in either the 1st or 3rd quadrant, while the duty-controlled fast leg device conducts current from drain to source, and the (1−d) fast leg device conducts current from source to drain.

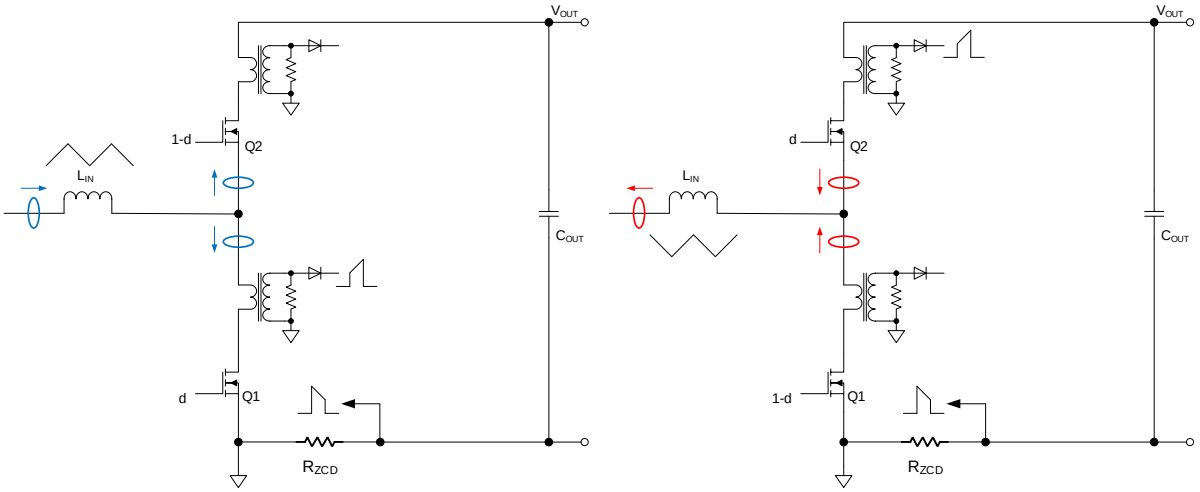


Figure 24 Current Flow in Positive and Negative Half Line Cycles

The purpose of the current sense is to obtain the input and output currents. The input current is the inductor current, which is used in the control and the input power metering. The output current is used in the output power metering. Figure 24 shows the current sense block diagram in HP1010.

For the TPPFC topology, the HP1010 supports current sense schemes as following:

- Two current transformers + one sense resistor (2*CT+1*R_{sen})

To achieve input and output current sense monitoring and protection, the CS1 and CS2 can be configured as Table 5 for correctly sense the input and output current.

Table 5. Input and Output Current Sense

Topology	Current Sense Scheme	Input Current Sense	Output Current Sense
TPPFC	Scheme 1: 2*CT+1*R_{sen}	CS1+CS2	CS2

Since different current sense components are used, the CS1 and CS2 current sense equivalent resistances can be selected as 6.25 mΩ, 12.5 mΩ, 25 mΩ, 50 mΩ, 100 mΩ, 200 mΩ, and 400 mΩ. The goal of adopting different equivalent resistances is to optimize the usage of 1.4 V full-range input ADC and achieve power savings. For example, in the current transformer method, if the turn ratio of CT1 and CT2 (NP:NS) is 1:100 and the R_{CS1} is 10 Ω, then the CS1 equivalent resistance is 1/100*10=100 mΩ.

CURRENT SENSE SCHEME: TWO CURRENT TRANSFORMERS + ONE SENSE RESISTER FOR TPPFC TOPOLOGY

The HP1010 incorporates a novel current sensing scheme utilizing two inputs: one for sensing inductor current during the duty-controlled portion (d portion) of the switching cycle and one for sensing inductor current during the (1−d) portion of the switching cycle. These two signals are summed together inside the controller to reconstruct an image of the inductor current. The current sense configuration used in a typical application is illustrated in Figure 25.

The CS1 and CS2 inputs sense the inductor current during the duty-controlled portion of the switching cycle. This can be referred to as the inductor current upslope. The recommended scheme for the CS input requires two current sense transformers (CT1 and CT2), one in series with each of the fast leg switches, a diode OR'ed output from the secondary side of CTs, a single current sense resistor, and an RC filter to mitigate noise pickup on the sense circuit. Additionally, a "blanking" circuit is required across each secondary to selectively shunt with the CT output to ground.

Each of the CTs is active during the half line cycle when the respective switch is duty controlled. When the respective switch is (1−d) controlled then the blanking circuit is active, and the CT secondary is blocked. In Figure 25 the blocking circuits are shown. CT1 is blocked during negative AC cycle by the NEGPOL signal as Q1 switch is (1−d) controlled during negative AC cycle. CT2 is blocked during positive AC cycle by the POSPOL signal as Q2 switch is (1−d) controlled during positive AC cycle. The POSPOL and NEGPOL timing diagram is shown in Figure 26.

The CS1 pin is also utilized for cycle-by-cycle peak current limiting and overload protection. It protects the power devices from destructive damage due to inductor saturation, output power overload, or thermal overstress by immediately terminating the duty-controlled drive pulse when the peak current limit threshold is reached.

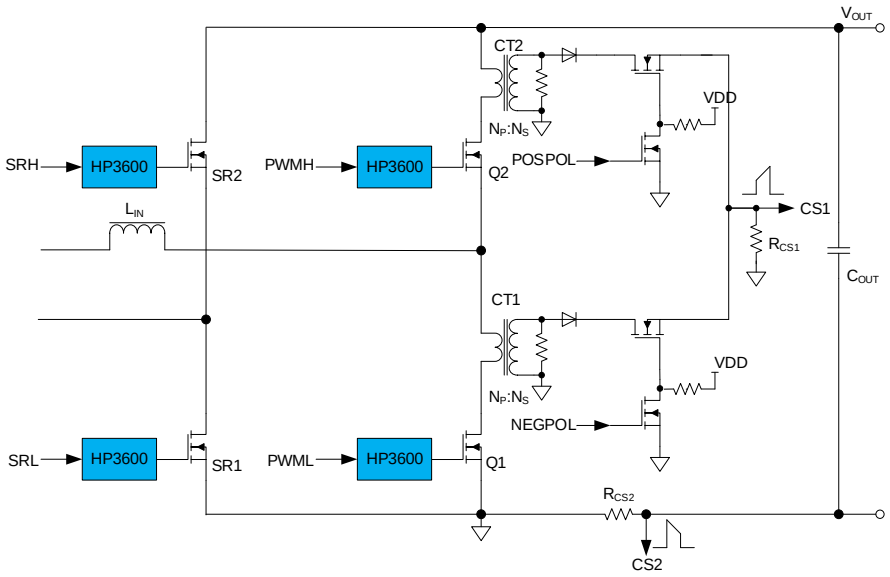


Figure 25 Two Current Transformers + one Sense Resistor Scheme

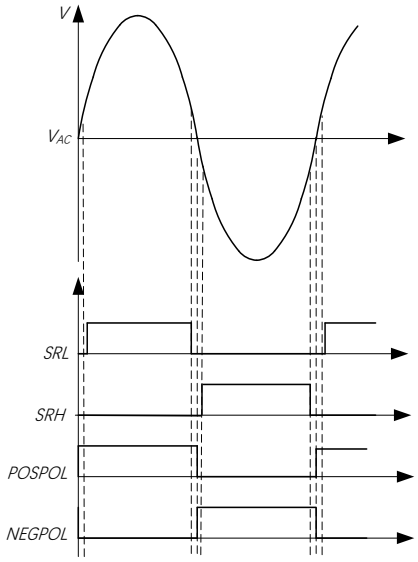


Figure 26 POSPOL and NEGPOL Timing to Control Current Transformers Signal

The R_{CS1} resistor value is calculated based on peak current limiting. The maximum peak inductor current is calculated in the application using Equation (3) where P_O is output power, η is efficiency, V_{AC} is the RMS input voltage, L_{IN} is the inductance of the boost, f_{SW} is the CCM switching frequency, and D_{PK} is duty cycle at the peak AC line voltage. Once the maximum peak current is determined, Equation (4) is used to find an upper limit on the CS1 resistor based on the CS1 current limit threshold, V_{CS1_OCP}, and the turns ratio of the current sense transformers. This calculation should be done at the minimum AC input voltage, usually 90 VAC, and may also need to be repeated at the minimum high line voltage in the application, typically 180 VAC, depending on the application's output power requirements.

$$I_{L\_PK} = \frac{\sqrt{2}\times P_O}{\eta\times V_{AC}} + \frac{\sqrt{2}\times V_{AC}\times D_{PK}}{2\times L_{IN}\times f_{SW}} \quad (5)$$

$$R_{CS1} < \frac{N_S}{N_P} \times \frac{V_{CS1\_OCP}}{I_{L\_PK}} \quad (6)$$

The CS2 senses the voltage across a sense resistor, which senses the inductor current during the (1−d) portion of the switching cycle. This can be referred to as the inductor current downslope or demagnetization. The recommended sensing element for the CS2 is a high-power, low-inductance, current sense resistor. The HP1010 converts the CS1 and CS2 inputs separately and sums their digital values together to obtain the digital value of the inductor current. This inductor current signal is critical to optimizing THD performance in the application. Since the CS2 resistor causes some power loss, a smaller resistor value is preferred. As shown in Table 6, a half of the CS1 CT gain is chosen to be the CS2 resistor value. In the internal a gain of 2x is applied to the digital CS2 to ensure that CS1 and CS2 have the equal magnitude.

Same as before, the CS1 and CS2 sense gain is calculated based on the output power level.

Table 6. Recommended Equivalent Resistance Selection

Output Power(W)	200	400	800	1600	3200	6400
Input current RMS value @ VAC = 85 VAC (A)	2.35	4.71	9.41	18.82	37.65	75.29
Input current Peak value @ VAC = 85 VAC (A)	3.33	6.65	13.31	26.62	53.23	106.47
CS1 equivalent resistance (N_P/N_S*R_{CS1}) (mΩ)	0.4	0.2	0.1	0.05	0.025	0.0125
CS1 peak voltage (V)	1.33	1.33	1.33	1.33	1.33	1.33
CS2 resistance (R_{CS2}) (mΩ)	0.2	0.1	0.05	0.025	0.125	0.0625
CS2 peak voltage (V)	0.67	0.67	0.67	0.67	0.67	0.67

CS1 AND CS2 COMPARATORS

For the TPPFC topology and current sense schemes 1, the HP1010 has a programmable cycle-by-cycle current limit threshold (V_{CS1_OC}) for the CS1 pin, which can be set based on the power level. The cycle-by-cycle current limit is triggered by an analog comparator that compares the CS1 signal and the set threshold V_{CS1_OC}. When the threshold is crossed, the PWM pulse is terminated. The next switching cycle resumes normally.

The cycle-by-cycle current limit comparator also features programmable blanking and debounce times. See Table 7 for the debounce and blanking time option.

Table 7. Debounce and Blanking Time for CS1 and CS2 Cycle-by-cycle Limit

Parameter	Values or Options
Debounce Time	40 ns, 80 ns, 120 ns, 160 ns
Blanking Time	480 ns, 960 ns, 1440 ns, 1920 ns
Propagation Delay	100 ns maximum
Threshold Value	Programmable from 1.0 V to 1.5 V with 7.8 mV step for V_{CS1_OC} and V_{CS2_OC} (positive)
Actions for Protection	Terminate ‘d’ drive signal and turn on the ‘1−d’ drive signal earlier (dead time remain unchanged) for 16 consecutively switching cycles, and then trigger IIN_PK_OC fault.

SYNCHRONOUS PWM DRIVE CONTROL

The synchronous PWM of the fast leg in the TPPFC topology enables higher efficiency performance but proper gating of the device is necessary for optimizing efficiency and ensuring robustness. A diagram of the sync control methodology is shown in Figure 27. First, a dead time, T_{DT1}, typically 100 ns, follows the falling edge of the PWM duty−controlled drive to prevent cross conduction. At the same time, the current measured through CS1 or CS1+CS2 needs to exceed a threshold to enable the sync drive. In lighter loads, the current may never exceed this threshold, and the sync device will never enable. This is done to prevent switching of the sync device at light loads where the associated switching losses could negatively impact the overall efficiency of the application.

At increasing loads, the current will exceed the threshold, and the sync drive will remain enabled until the current falls below the threshold. It is noted that the Sync PWM cannot let the inductor current reverse polarity. If the sync device remains on for too long, the inductor current would reverse polarity and begin cycling energy from the bulk capacitor. This would lead to increased RMS currents in the system and could diminish overall efficiency.

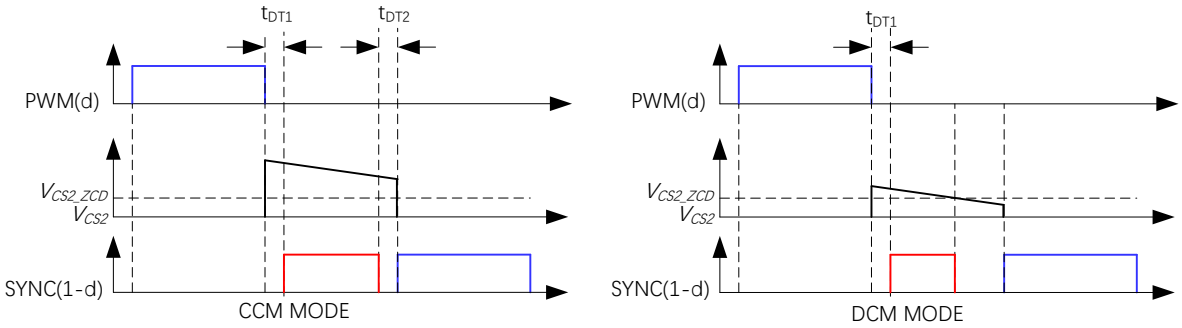


Figure 27 Synchronous PWM Drive Control

POWER FACTOR CORRECTION CONTROL LOOP

The HP1010 implement the average current mode power factor correction control loop. The implementation of the loop is digital, and all the signals are converted from analog to digital before they are processed by the control loop. Σ-Δ ADCs are used to achieve high performance, cost-effective implementation. The diagram of the current loop and voltage loop is shown in Figure 28.

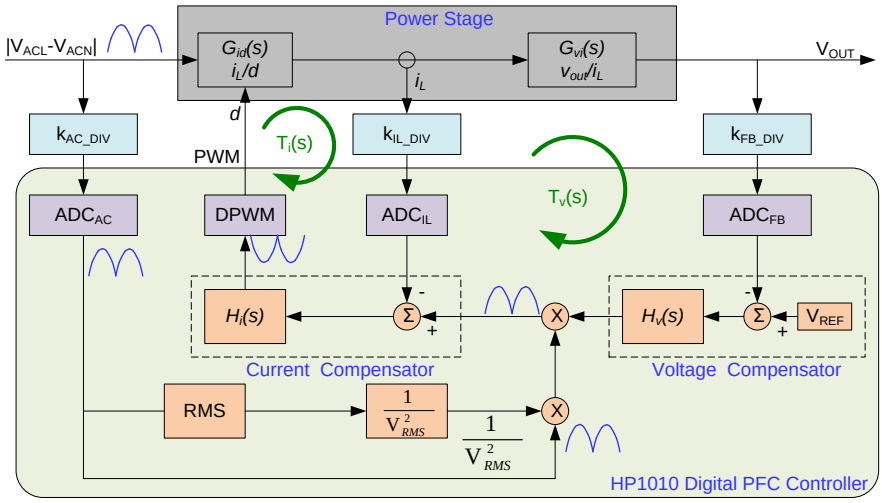


Figure 28 Current and Voltage Control Loops Diagram

FAST LOOP MODE

During transients, a fast loop mode is enabled in order to provide quicker loop responses. Typical timing can be seen in Figure 29. Fast loop mode has separate settings that can be programmed to respond quickly to load transients. The fast loop mode can be disabled by the user if it is not necessary by the application.

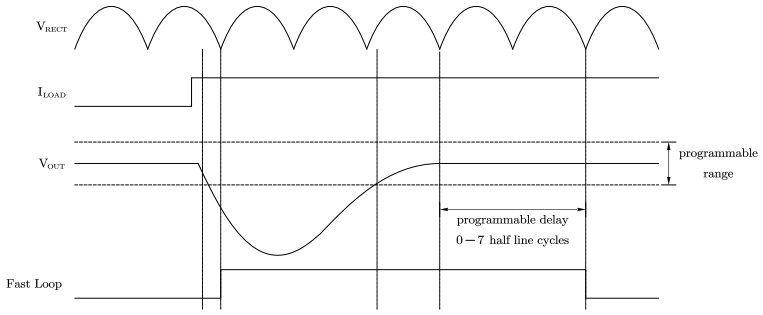


Figure 29 Fast Loop for Transient Response Improvement

DIGITAL PULSE MODULATION

The switching frequency is programmed in the SWTICHING_FREQ command. The switching frequency options are list in Table 8.

Table 8. Switching Frequency Options

Frequency setting #	Frequency setting (kHz)	Real Frequency (kHz)	Division of 25MHz
0	20	20.00	1250
1	30	30.05	832
2	45	44.96	556
3	65	65.10	384
4	90	89.93	278
5	120	120.19	208
6	160	160.26	156
7	195	195.31	128

PULSE-WIDTH MODULATION

Using the HP1010, only trailing edge modulation may be used. When utilized with downstream converter synchronization, trailing edge modulation can lower the rms ripple current in the bulk capacitors.

DUTY CYCLE MINIMUM/MAXIMUM LIMITS

The HP1010 allows the user to program the minimum off time and the minimum on time for the PWM outputs separately, thereby allowing the minimum and maximum duty cycles to be set. The minimum on-time is the smallest PWM pulse that the modulator generates on the PWM output. The minimum on-time of the main PWM and Sync PWM can be programmed from 40 ns to 320 ns in steps of 40 ns. The dead time Td1 between main PWM off and Sync PWM on is programmed from 40 ns to 320 ns, and the dead time Td2 between Sync PWM off and main PWM on is programmed from 40 ns to 320 ns. The maximum on-time of PWM is ($T_{sw}-T_{d1}-T_{d2}$).

FREQUENCY DITHERING (SPREAD SPECTRUM)

The PWM signal can be altered digitally to optimize for EMI reduction. For a wider but lower EMI spectrum, the switching frequency varies with the rectified line voltage. The switching cycle changes linearly with time from 87.5% to 112.5% of the nominal value, resulting in a frequency variation of 114% to 89% of the nominal value.

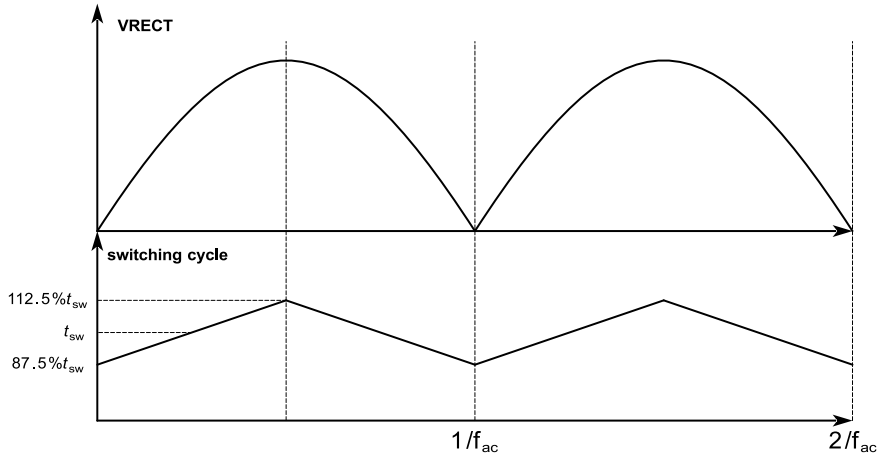


Figure 30 Frequency Dithering

OPERATION MODES

OPERATION MODE SUMMARY

The system can run in different modes. In each mode, the four PWM signals operates differently. The mode transition is triggered by events. These events may be from the ADC output, like OTP, OVP, zero-crossing, etc. It can also be from the measurement (monitoring block), like light load detection or HVDC.

The HP1010 supports normal AC input (the frequency is between 40 and 70 Hz). With the AC input, they have the same operation. However, in HVDC mode, the system works as a boost converter; the main PWM switch is selected based on the input DC polarity.

START-UP SEQUENCE

When the user turns on the power factor correction, the following start-up procedure occurs, as shown in Figure 31.

1. Polarity detection. When the AC input voltage or the DC input voltage reach a threshold, the polarity detection starts and the POL_DET flag is triggered. The POSPOL and NEGPOL pins start to output signals indicating the input voltage polarity. Then the HP1010 enters the AC line frequency detection state.
2. AC line frequency detection. It takes four consecutively half-AC cycles for line frequency detection. When the AC line frequency is within the range (50/60 Hz AC or HVDC), the HP1010 enters the brown-out detection state.
3. Brown-out detection. The HP1010 takes one AC cycle to complete the brown-out detection. If the AC line voltage is higher than the VIN_ON threshold, the brown-out flag is cleared. The HP1010 enters a turn-on delay state.
4. Turn-on delay. During this period, the relay is turned on, CS Short Detection is processed. The polarity detection comparator is then changed for surge detection.
5. Soft-start. The soft start PWM always begins at 0° of the AC cycle. During this period, the PWML and PWMH operate in duty-controlled mode (‘d’ drive) only. The (1−d) controlled mode (‘1−d’ drive) is still disabled. The SRL and SRH output signals, and the output voltage ramps up. After the HP1010 finishes the soft start and enters the normal operation state, the PFCOK flag is triggered and the PFCOK pin is pulled high.
6. Normal operation. During normal operation, the PWML and PWMH operate in duty-controlled mode and (1−d) controlled mode, respectively. The PFC may switch between CCM mode, DCM mode, and burst mode.

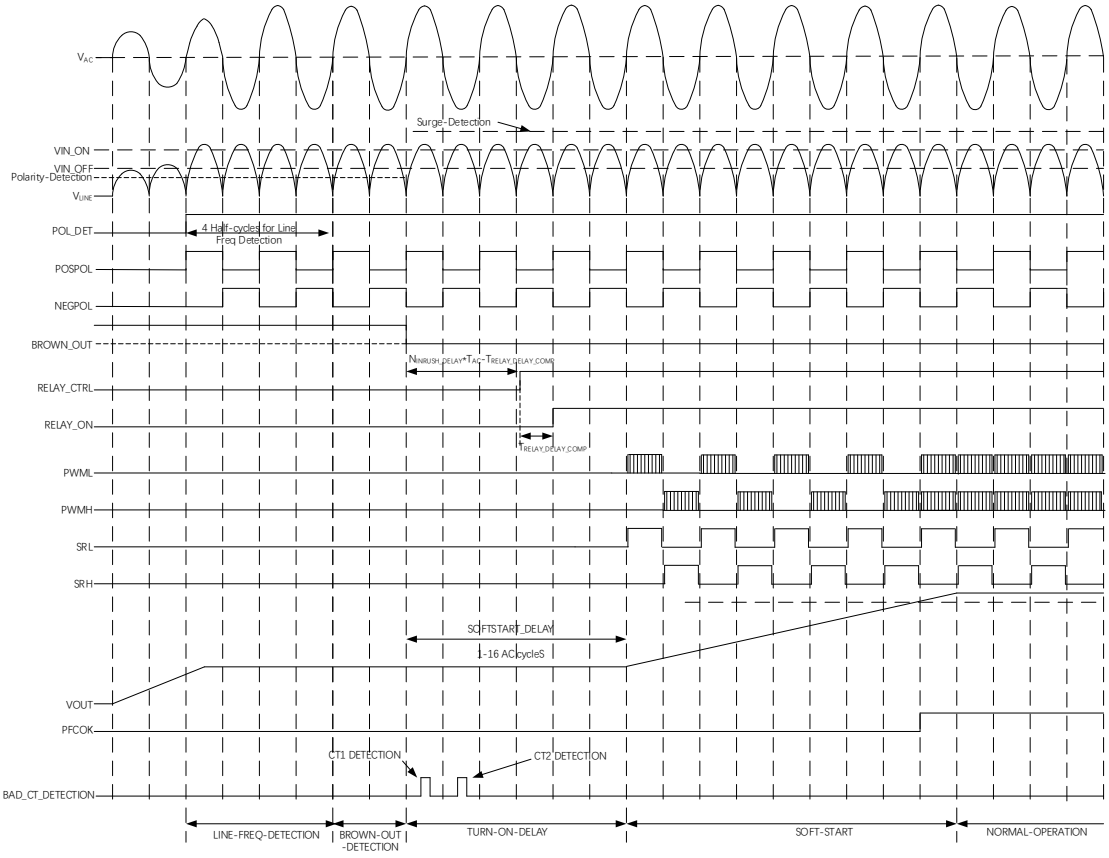


Figure 31 Start-up Sequence

GPIO PINS & FUNCTIONS

The pins of RELAY/GPIO0, POSPOL/GPIO1, NEGPOL/GPIO2, SRL/GPIO3, SRH/GPIO4, RXD/GPIO5, TXD/GPIO6, and PFCOK/GPIO7 support the general-purpose digital IO function.

RELAY CONTROL

By controlling the power factor of the power drawn from the input, the PFC circuit generates a controlled, high voltage DC output while ensuring that the current is always proportional to the input voltage. High peak currents are drawn at the time of applying power to the input, though, as a result of the presence of a sizable "bulk" capacitor across the output. As "inrush" current, which is a PFC converter typically needs an inrush protection circuit to avoid circuitry damage.

Current protection techniques typically only work at initial power startup. Resistive current limiting is a widely used technique. It employs a resistor with the proper rating linked in series with the PFC circuit's primary power connection. This resistor is eliminated (i.e., shorted via a relay contact) following the charging of the output capacitor. Usually, once the initial inrush fades and the PFC converter turns to normal operation mode, the relay driving circuit needs a low power supply (typical 12V) to shut the relay contact. At this point, the PFC initiates its own current-limiting features, such as a "soft-start" or "peak-current detection".

Relays from various vendors exhibit varying delay times. To ensure proper operation, the relay should be closed at the beginning of the positive half cycle. Accounting for the relay delay time (t_{delay_relay}), the RELAY signal controlling the relay should be activated t_{delay_relay} time before the zero-crossing point of the positive half cycle (0° of the AC cycle).

Therefore, the actual delay time from the brown-out flag cleared to the RELAY pulling high is $N_{INRUSH\_DELAY}*T_{AC}-T_{REDELAY\_DELAY\_COMP}$. In the case of Figure 32, N = 2.

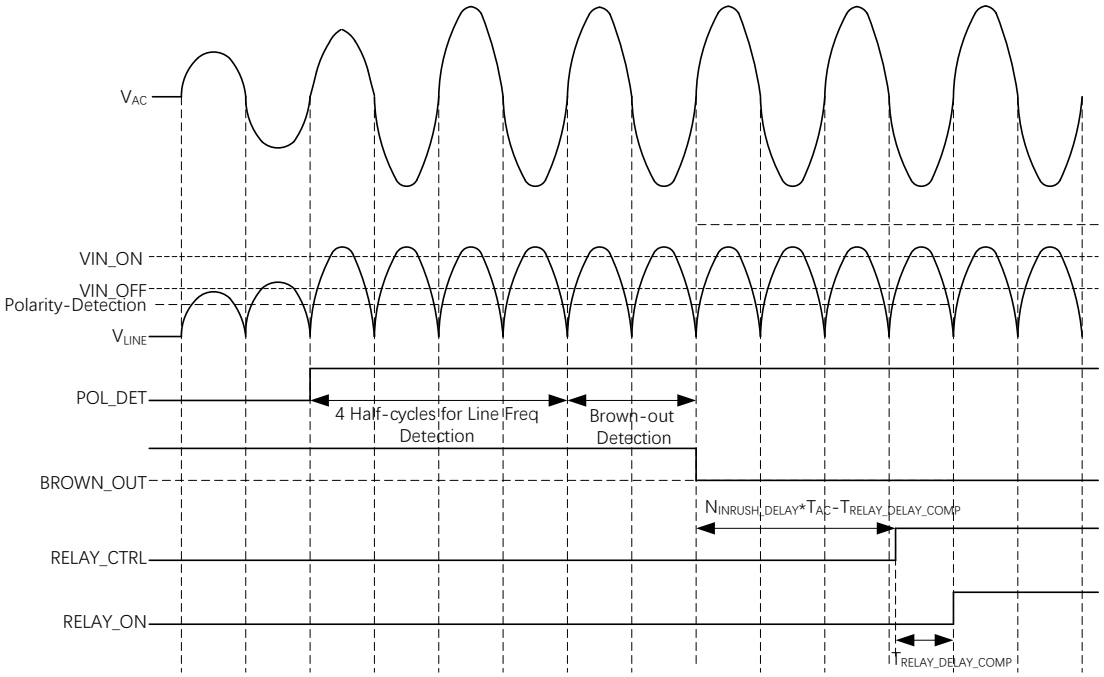


Figure 32 Relay Control Timing

During the normal operation of the PFC, the relay is closed to shorten the inrush resistor. It reduces the power loss on this resistor. But with a very light load or a zero load, the input current is almost zero. The power loss over the resistor can be ignored compared to the power consumption of the relay circuit. In this situation, disabling the relay can save more power. Thus, the RELAY signal for the relay control can be set to be low at this moment. The recovery hysteresis is 5 Watts.

X-CAPACITOR DISCHARGE

Consumer equipment must comply with safety regulations like IEC 61010-1, IEC 62368-1, and others. When the mains power is disconnected, the EMI filter capacitors (X-capacitors) connected between the phase and neutral must be discharged to a safe level. This prevents any risk of electrical shock to the user due to stored energy in the capacitors. This discharge is mandatory when the total capacitance before the input bridge exceeds 100 nF.

Typically, this function is performed by means of a resistor in parallel, but this method cannot be applied in cases where the converter requires very low power consumption during the light-load or no-load operation because the losses of the X-cap discharging resistor would be too high.

To overcome this issue, HP1010 offers a control signal to discharge the voltage across the X-cap without the traditional X-cap on-line discharge resistor. The HP1010 internal circuits detect the AC power disconnection by sensing the voltage on the ACL and ACN pins. After a detection time (typically 30 ms), the X-cap discharge operation is triggered, and the external high voltage switches are turned on. A discharge current (a few mA) is drawn from the phase and the neutral wires, ensuring the X-capacitor discharge with a constant discharging time of 250 ms. Typically, GPIO0-GPIO7 pins can be configured to turn on the discharge circuit, as shown in Figure 33.

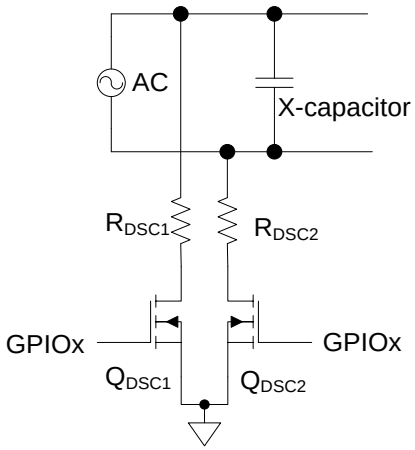


Figure 33 X-cap Discharge Circuit

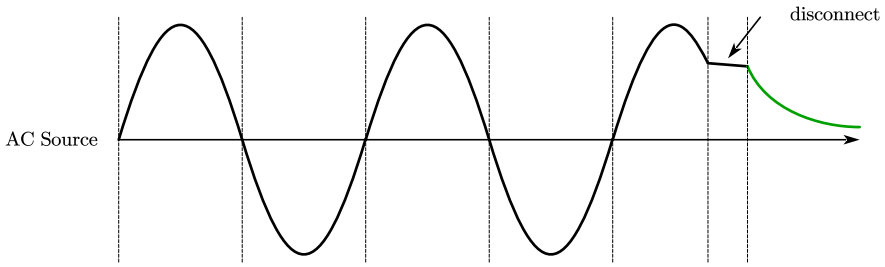


Figure 34 AC Disconnection (unplug) and X-cap Discharge Operation

As shown in Figure 34, normally the AC main voltage is applied to the X-cap. When the AC power is suddenly unplugged, the voltage across the X-cap maintains its value at that moment. In HP1010, the ADC continuously measures the voltage between ACL and ACN, which is equivalent to the voltage across the X-cap. If it detects a transition to DC voltage, one GPIO signal will be triggered to become active. This GPIO signal will be connected to the X-cap discharge circuit as shown in Figure 33, which includes the two resistors (R_{DSC1} and R_{DSC2}) and two power FETs (R_{DSC1} and R_{DSC2}) typically. In normal operation, these two power FETs are off. Consequently, the equivalent resistance of this branch is extremely high, resulting in virtually no current flow. Upon detection of AC disconnection by the HP1010, the GPIO signal activates the power switches, allowing the resistors R_{DSC1} and R_{DSC2} to discharge the X-capacitor's stored voltage.

When the input voltage is DC input, the X-capacitor discharge is not functional.

FAULT, PROTECTIONS AND MONITORINS

The HP1010 offers advanced fault and system monitoring capabilities. It includes voltage, current, and power readings in its system monitoring features. Current, voltage, power, and temperature out-of-limits are among the fault conditions that can be programmed. These variables, flags, and thresholds are read through an I^2C interface, and all the threshold settings can be stored in the on-chip EEPROM.

FAULT FLAGS AND PROTECTIONS

An extensive set of flags is programmable when certain thresholds or limits are exceeded, these flags are described in Table 9.

The NTC/ROV is a dual-function pin. Once the NTC function is selected by default, the over-temperature condition is able to trigger the NTC_OT flag. Conversely, if the redundant OVP is selected, the open loop condition can trigger the ROVP flag. Additional information is provided in Section OTP & Redundant OVP (NTC/ROV Pin) .

Table 9. Summary of Flags

Flag	Descriptions	Debounce	Protection Action
VIN_MODE	0: fault, 1: 40 Hz ~ 70 Hz, 3 = DC		None
BROWN_OUT	VIN exceed VIN_ON to clear flag	0.5 cycle	See Table 10
IIN_PK_OC	CS1 cycle-by-cycle current limit timeout	2, 4, 8, 16, 32,48,64	See Table 10
IIN_AV_OC	Input average over-current fault	2 switching cycle	See Table 10
SURGE	Surge detection		See Table 10
VIN_OV	Input over-voltage fault		See Table 10
INRUSH	RELAY signal is high	None	None
HIGH_LINE	0: low line; 1: high line	1 AC cycle	None
VOUT_SLW_UV	Output under-voltage fault	0~30 ms	See Table 10
VOUT_SLW_OV	Output slow over-voltage fault	0~30 ms	See Table 10
VOUT_FST_OV	Output Fast over-voltage fault	40~100 µs	See Table 10
FAST_LOOP	Fast loop operation	None	None
NTC_OT	NTC over-temperature fault	500, 1000 ms	See Table 10
PFCOK	Combination of eight fault flags	None	PFCOK pin is high
ALERT#	Combination of eight fault flags	None	ALERT# pin is low
CS_SHORT	CS Short fault	None	Wait for 1s and retry
FREQ_NOK	Line frequency not OK	4 cycles	See Table 10
VOUT_OL	Output open-loop fault	0~30 ms	See Table 10
3V3_UVLO	VDD Supply UVLO		HW reset and restart
ROV	Redundant OVP	40~100 µs	See Table 10
AUTO_PFC_OFF	Turn off PFC at low load		Turn-off PFC

Table 10 provide summary of fault protection actions.

Table 10. Summary of Fault Protection Actions

Flag	Type	Protection action
BROWN_OUT FAULT	3	Enter sag operation then go back to PFC off state
IIN_PK_OC	1	Ignore, latch, or fault recover
IIN_AV_OC	1	Ignore, latch, or fault recover
SURGE	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover
VIN_OV	1	Ignore, latch, or fault recover
VOUT_SLW_UV	1	Ignore, latch, or fault recover

VOUT_SLW_OV	1	Ignore, latch, or fault recover
VOUT_FST_OV	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover
VOUT_OL	1	Ignore, latch, or fault recover
NTC_OT	1	Ignore, latch, or fault recover
FREQ_NOK	3	Enter LINE_FREQ_EXCEED mode for 4 ac cycles, if fault still exist, goes to PFC off state
ROV	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover

PFCOK AND ALERT# PINS

The HP1010 features two digital status pins: PFCOK and ALERT#. The PFCOK is designed to manage the operation of a downstream DC−DC converter by acting as an enable or UVLO signal. The PFCOK output goes to high when the application is in nominal operation and low when the device detects a fault condition. The ALERT# is pulled low to notify the I^2C master when the device detects a fault condition. When the I^2C master reads the fault flags, the relevant fault flags will be cleared, the ALERT# flag is reset.

Both signals provide an OR function for a programmable list of internal flags, as depicted in Figure 35. Users have the ability to mask certain flags to customize the behavior of the PFCOK and ALERT# signals according to their requirements. If the signals on the PFCOK and ALERT# pins are asserted, the associated internal flag will be set as well.

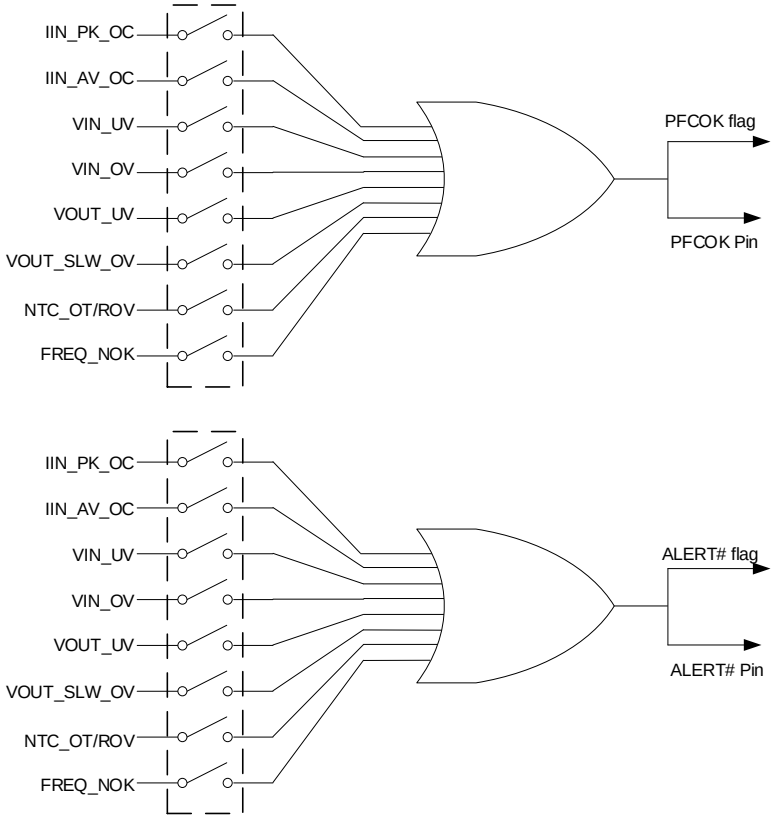


Figure 35 PFCOK Signals

OTP & REDUNDANT OVP (NTC/ROV PIN)

The NTC/ROV pin is a dual-function pin for over-temperature protection (OTP) and redundant over-voltage protection (Redundant OVP). When utilized as OTP, a source current I_{NTC_SRC} (typically 46 μA) is applied to the NTC/ROV pin. The HP1010 detects an NTC over-temperature fault when the NTC/ROV pin voltage falls below the lower fault threshold, V_{NTC_OT}, which is typically 0.4 V. The hysteresis is 0.4 V. The protection actions include a reset from brown-

out and latch mode. Once operating in latch mode, the line frequency detection and VAC detection continue. A PFC_ON signal from the CTRL pin and/or the ENABLE bit can trigger a reset from the brown-out state.

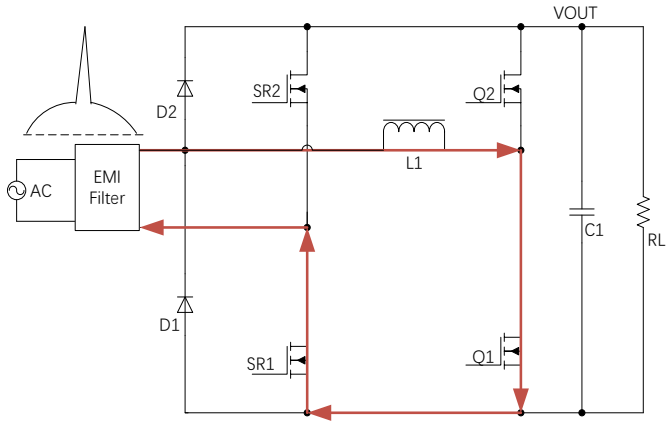
Alternatively, the NTC/ROV pin can be configured to serve as a redundant OVP function. The redundant OVP is utilizing an analog comparator and directly monitors the feedback pin voltage to immediately blank the drive pulses if necessary. The reference of the redundant OVP comparator is programmable from 1.9 V to 2.5 V with a 9.4 mV step. This represents that the actual redundant OVP limit is programmable from 380 V to 500 V with a 1.87 V step. If the output voltage surpasses the redundant OVP limit, a ROV fault is activated. When the redundant OVP is active, the source current I_{NTC_SRC} is disabled. The protection actions include all ignore, latch mode, and going to fault recovery mode. While in latch mode, the line frequency detection and VAC detection persist. A PFC_OFF signal will reset the HP1010 to a PFC off state.

SURGE PROTECTION

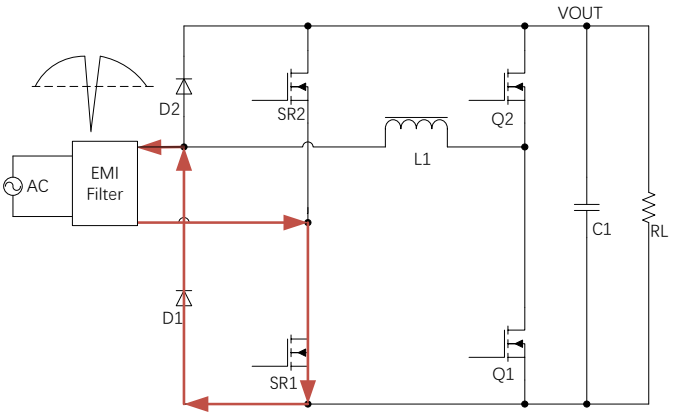
In an AC circuit, a voltage spike is a transient event, typically lasting 1 to 30 ms, that may reach over 1,000 volts. Lightning that hits a power line could induce several thousands, sometimes 100,000 volts or more. Spikes can degrade wiring insulation and destroy electronic devices like light bulbs, battery chargers, modems, TVs, and other consumer electronics.

Figure 36 shows the surge test scenarios. During the positive AC cycle, the HP1010 detects the V_{AC} positive voltage and V_{AC} zero crossing. Once the HP1010 detects the surge fault through V_{AC} exceeding a programmed positive limit, typically 400 V, or V_{AC} zero crossing, HP1010 disables the PWML, PWMH, SRL and SRH signals immediately. When the fault disappears, HP1010 recovers all PWM signals without a soft start.

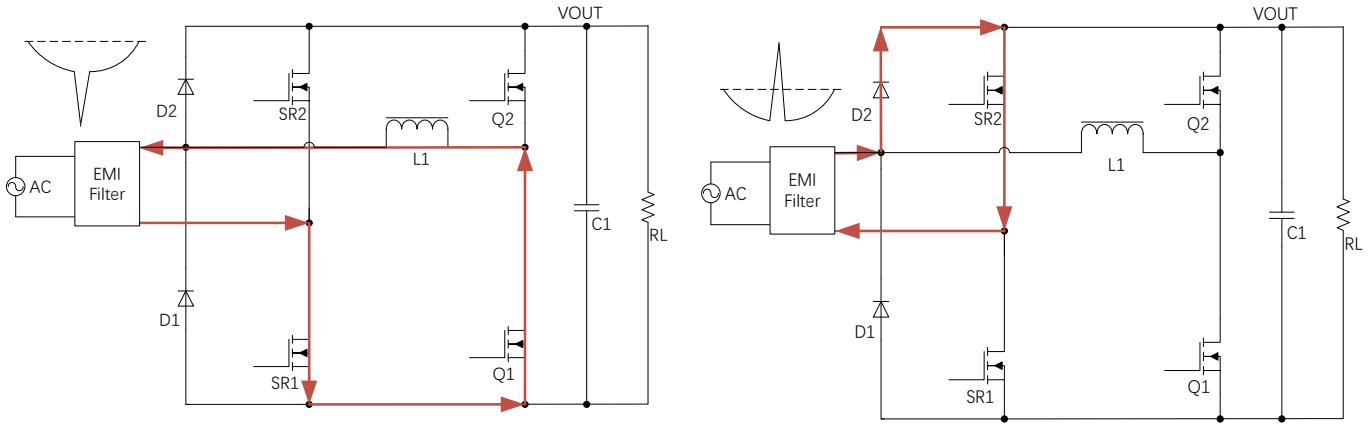
During the negative AC cycle, the HP1010 detects the V_{AC} positive voltage and V_{AC} zero crossing. Once the HP1010 detects the surge fault through V_{AC} exceeding a programmed negative limit, typically -400 V, or V_{AC} zero crossing, HP1010 disables the PWML, PWMH, SRL and SRH signals immediately. When the fault disappears, HP1010 recovers all PWM signals without a soft start.



a) Positive AC cycle with in-phase surge



b) Positive AC cycle with inverted-phase surge



c) Negative AC cycle with in-phase surge

d) Negative AC cycle inverted-phase surge

Figure 36 Surge Test Waveforms

POWER METERING

True RMS values are calculated at the end of each half AC cycle by integrating the instantaneous values across each line cycle. The averaging window is programmable from 64, 128, 256, and 512 AC cycles. For the DC input, the averaging window is programmable for 1.28 seconds, 2.56 seconds, 5.12 seconds, and 10.24 seconds. At the end of each averaging period, the new average values are written to the registers and are available to be read out through the interface until they are overwritten by the next averaged value at the end of the next averaging period.

Figure 37 shows the block diagram of power monitoring. The IIN_SENSE_METHOD should be correctly selected.

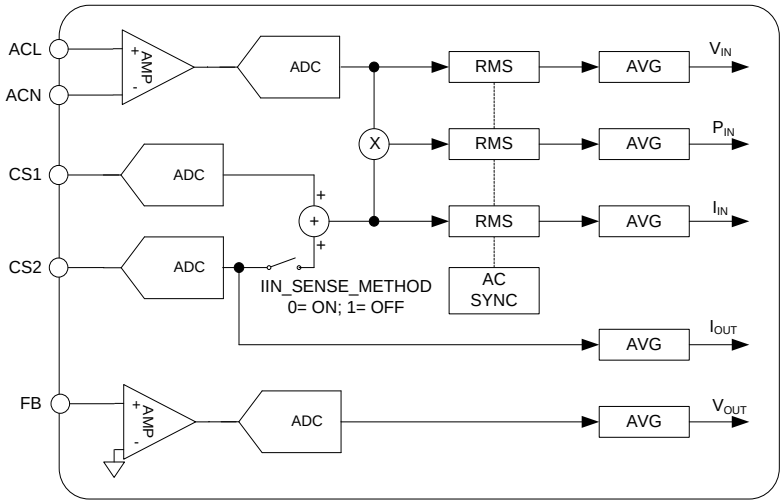


Figure 37 Power Monitoring Diagram

COMMICATION INTERFACES AND EEPROM

The HP1010 provides one I²C communication interface and one UART communication interface.

I²C INTERFACE

The I²C Bus (Interface wires) consists of just two wires and are named as Serial Clock Line (SCL) and Serial Data Line (SDA). The data to be transferred is sent through the SDA wire and is synchronized with the clock signal from SCL. All the devices/ICs on the I²C network are connected to the same SCL and SDA lines as shown below.

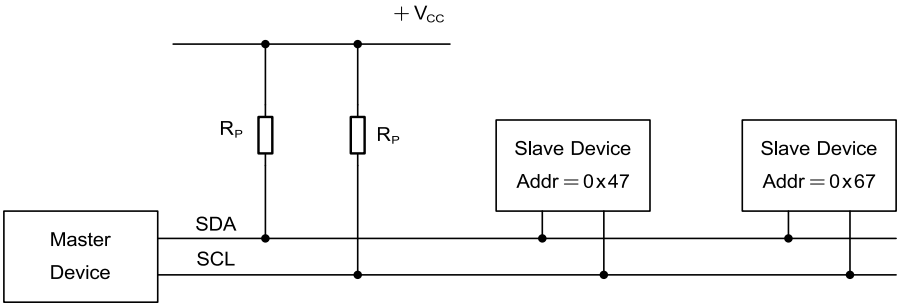


Figure 38. I²C Communication

The ALERT#/ADD is dual function pin. During the power-on reset, the state of this pin is sampled. Note: A 900 kΩ resistor should be used when connecting to the VDD pin or GND pin to reduce standby current, as shown in Figure 39.

- HIGH = I²C address is 0x67.
- LOW = I²C address is 0x47.

Figure 39 I²C Addressing

UART INTERFACE

Beside the I²C interface, the HP1010 also communicates with an external digital device with a standard UART protocol using two dedicated pins. The UART serial interface allows the user to:

- Write/read configuration registers:
  - ENABLE register bit to remote enable or disable PFC function.
  - VREF_LLINE register to set low line voltage regulation reference.
  - VREF_HLINE register to set high line voltage regulation reference.
- Read all STATUS and Telemetry register contents.

The HP1010 also supports low-cost, conventional opto-couplers for slow-speed communication.

When sleep mode is turned off, the HP1010 never goes into sleep mode. The UART feature is active as default. The TXD/RXD configuration determines how the HP1010 can connect to the host device.

The UART function is not available if sleep mode is enabled. After PFC has been off for five seconds, HP1010 automatically goes into sleep mode. The sleep state can be promptly woken up by a write or read to I²C. The HP1010 can also be promptly woken up from sleep mode by switching clearing PFC off state.

BAUD RATE

Both the transmitting UART and receiving UART must agree on the Baud Rate for a successful data transmission. Baud Rate is measured in bits per second. Some of the standard baud rates are 1200 bps, 9600 bps, 57600 bps, 115200 bps etc. Out of these 9600-bps baud rate is the most used. The baud rate is configurable through registers with I^2C interface:

Table 11. Baud Rate Options

Baud Rate (bps)	9600	1200	57600	115200
Options	0	1	2	3
Division from 25 MHz	2604	5208	434	217
Real Baud Rate (bps)	9600.6	4800.3	5760.4	11521

RULES OF UART

There is no clock signal in UART, and the transmitter and receiver must agree on the rules of serial communication for error free transfer of data. Such rules include:

- Synchronization Bits (Start and Stop bits)
- Parity Bit
- Data Bits
- Baud Rate

The HP1010 supports the most widely used UART rules.

- Synchronization Bits (1 bit Start and 1 bit Stop)
- Parity Bit (yes, 1 bit)
- Data Bits (8 bits)
- Baud Rate (programmable)

EEPROM

The HP1010 has a built-in EEPROM controller that is used to communicate with the embedded 128 × 8-byte EEPROM. When the digital core and EEPROM are powered-on, all the data from the EEPROM will be loaded to corresponding registers to configure the IC's parameters. Users can also read or write these registers to program the IC's parameters according to different applications. When these parameters are fully tested and working as expected, users can program to EEPROM through the I^2C interface. V_{DD} = 4.0 V is recommended during programming.

APPLICATION INFORMATION

TOTEM POLE POWER FACTOR CORRECTION

Typical totem-pole PFC (TPPFC) application circuit is shown in Figure 40.

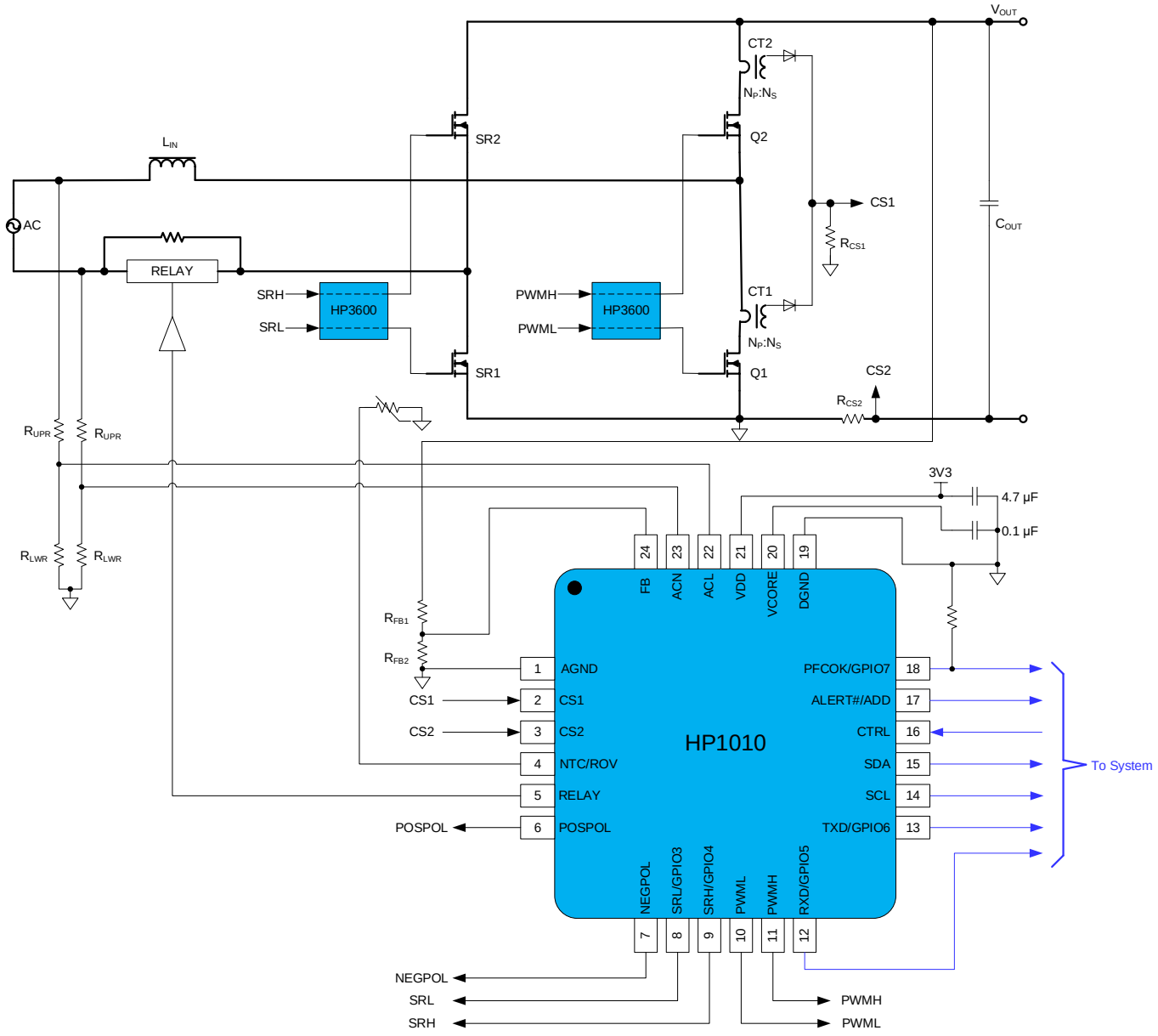
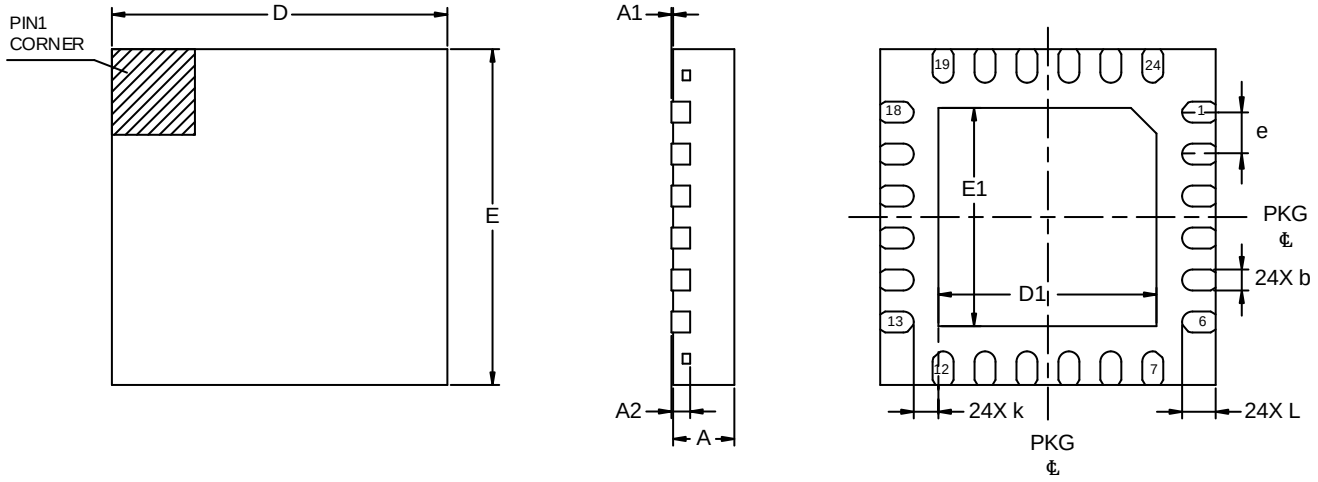


Figure 40 Totem Pole PFC Typical Application Circuit

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D1	2.40	2.70	2.80
E1	2.40	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN	

Figure 41 HP1010-BA000-QN24R Dimension

PACKAGE TOP MARKING

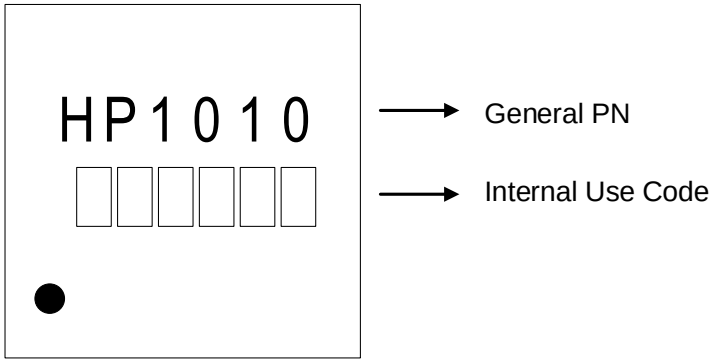


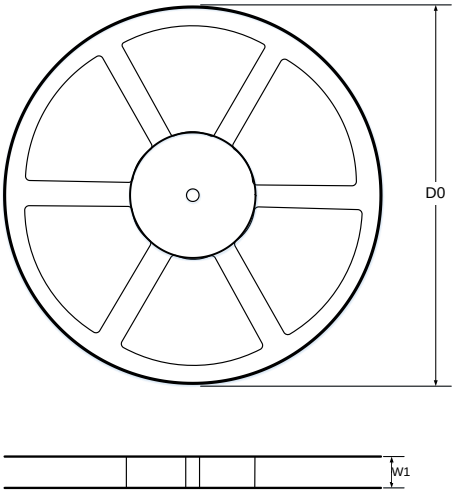
Figure 42 HP1010-BA000-QN24R Package Top Marking

ORDERING GUIDE

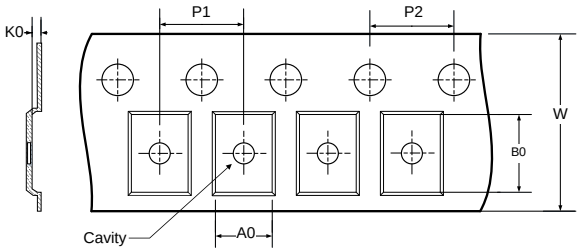
Model	Temperature Range	Package Type	MSL	Package Option	Quantity
HP1010-BA000-QN24R	-40°C to +125°C	QFN4x4-24L	3	T&R	5000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

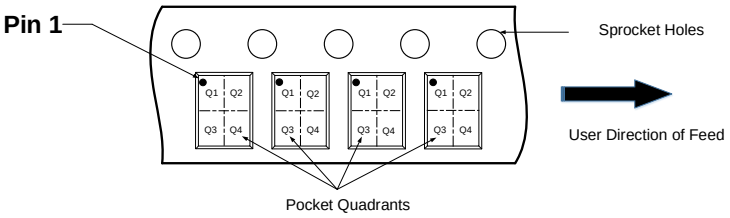


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP1010-BAXXX-QN24R	QFN4X4-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Figure 43 Tape and Reel Information

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