2-Bit Bidirectional Voltage-Level Translator

1 Features

- No direction-control
- Data rates
  24 Mbps (Push Pull)，2 Mbps (Open Drain)
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port($V_{CCA} \leq V_{CCB}$)
- V_{CC} isolation feature: if either V_{CC} input is at GND, both ports are in the high-impedance state
- No power-supply sequencing required:
  either V_{CCA} or V_{CCB} can be ramped first
- Ioff supports partial-power-down mode operation
- Operating temperature range:-40℃ to +85℃V

2 Application

- I2C/SMBus
- UART
- GPIO

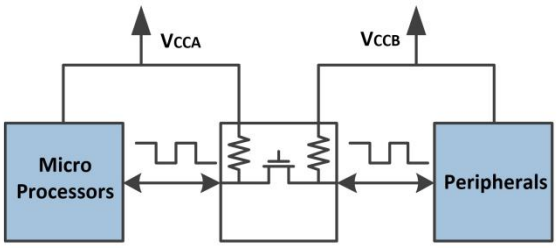
3 Description

This two-bit non-inverting translator which is a bidirectional voltage-level translator and can be used to build digital switching compatibility between multi voltage systems. This IC uses two separate configurable power supply tracks that including A ports supporting operating voltages from 1.65 V to 3.6 V with tracking V_{CCA} supply, and also including B ports supporting operating voltages from 2.3 V to 5.5 V with tracking V_{CCB} supply.

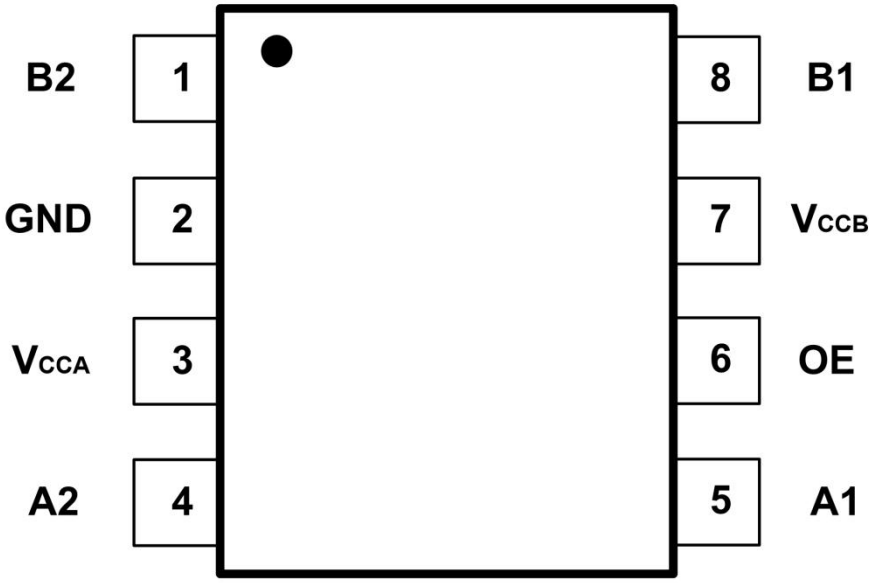
The advantage above provides the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8-V, 2.5-V, 3.3-V, and 5- V voltage circuit points.

Placing output-enable (OE) input to low level, all I/Os are forced to high-impedance state that significantly lower the quiescent current consumption. In order to ensure the high-impedance state during power up or power down, OE pin should be tied to GND via a pull down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

4 Circuit diagram



5 Device Pin and Packages



Name	Pin	I/O	Function
V_{CCB}	7	P	B Port Supply Voltage. 2.3V≤V_{CCB}≤5.5V
B1	8	I/O	Input/Output B1. Referenced to V_{CCB}.
B2	1	I/O	Input/Output B2. Referenced to V_{CCB}.
OE	6	I	Output Enable(Active High).Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	2	-	Ground
A2	4	I/O	Input/Output A2. Referenced to V_{CCA}.
A1	5	I/O	Input/Output A1. Referenced to V_{CCA}.
V_{CCA}	3	P	A Port Supply Voltage. 1.65V≤V_{CCA}≤3.6V and VCCA≤V_{CCB}

* It is suggested to leave the unconnected pins floating.

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings(1)(2)(3)

Parameters		Min	Max	Unit
Supply voltage, V_{CCA}		-0.3	6.0	V
Supply voltage, V_{CCB}		-0.3	6.0	V
Input voltage range,V_I	A port	-0.3	6.0	V
	B port	-0.3	6.0	
Voltage range applied to any output in the high-impedance or power-off state, V_O	A port	-0.3	6.0	V
	B port	-0.3	6.0	
Voltage range applied to any output in the high or low state, V_O	A port	-0.3	V_{CCA}+0.3	V
	B port	-0.3	V_{CCA}+0.3	
Input clamp current,I_{IK}	V_I＜0		-50	mA
Output clamp current,I_{OK}	V_O＜0		-50	mA
Continuous output current,I_O			±50	mA
Continuous current through V_{CCA},V_{CCB} or GND			±100	mA
Maximum junction temperature			150	°C
Storage temperature range		-65	150	°C

(1)Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2)The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3)The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-Body Model (HBM)(1)	±6K	V
		Charged-Device Model (CDM)(2)	±2K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port.V_{CCO} is the supply Voltage associated with the output port.

Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage (1)	V_{CCA}		1.65		3.6	V
	V_{CCB}		2.3		5.5	
High-level input voltage(V_{IH})	A-port I/Os	V_{CCA}=1.65V to 1.95V V_{CCB}=2.3 V to 5.5 V	V_{CCI}-0.2		V_{CCI}	V
		V_{CCA}=2.3 V to 3.6 V V_{CCB}=2.3 V to 5.5 V	V_{CCI}-0.4		V_{CCI}	
	B-port I/Os	V_{CCA}=1.65 V to 3.6V V_{CCB}=2.3 V to 5.5 V	V_{CCI}-0.4		V_{CCI}	
	OE input	V_{CCA}=1.65 V to 3.6 V V_{CCB}=2.3 V to 5.5 V	V_{CCI} ×0.8		5.5	
Low-level input voltage(V_{IL})(2)	A-port I/Os	V_{CCA}=1.65 V to 1.95 V V_{CCB}=2.3 V to 5.5 V	0		0.15	V
	B-port I/Os	V_{CCA}= 1.65 V to 3.6 V V_{CCB}=2.3 V to 5.5 V	0		0.15	
	OE input	V_{CCA}=1.65 V to 3.6 V V_{CCB}=2.3 V to 5.5 V	0		V_{CCA}×0.25	V
Input transition rise or fall rate(Δt/Δv)	A-port I/Os push-pull driving				10	ns/V
	B-port I/Os push-pull driving				10	
	Control input				10	
TA operating free-air temperature	-		-40		85	°C

(1) V_{CCA} must be less than or eqμal to V_{CCB}.

(2) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass gate transistor.

7 Electrical Specifications

7.1 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2)

Parameter		Conditions	V_{CCA}	V_{CCB}	Temp	Min	Typ	Max	Unit
V_{OHA}	Port A Output High Voltage	I_{OH}= –20 μA V_{IB} ≥ V_{CCB} – 0.4V	1.65V to 3.6V	2.3V to 5.5V	Full	V_{CCA}×0.7			V
V_{OLA}	Port A Output Low Voltage	I_{O}L=1mA V_{IB} ≤ 0.15 V	1.65V to 3.6V	2.3V to 5.5V	Full			0.3	V
V_{OHB}	Port B Output High Voltage	I_{OH}= –20 μA V_{IA} ≥ V_{CCA} – 0.4V	1.65V to 3.6V	2.3V to 5.5V	Full	V_{CCA} ×0.7			V
V_{OLB}	Port B Output Low Voltage	I_{OL}=1mA V_{IA} ≤ 0.15 V	1.65V to 3.6V	2.3V to 5.5V	Full			0.3	V
I_I	Input Leakage Current	OE	1.65V to 3.6V	2.3V to 5.5V	+25℃			±1	μA
					Full			±1.5	
I_{off}	Partial Power Down Current	A Ports	0V	0V to 5.5V	+25℃			±0.5	μA
					Full			±1	
		B Ports	0V to 3.6V	0V	+25℃			±0.5	
					Full			±1	
I_{OZ}	High-impedance State Output Current	A or B port OE=0V	1.65V to 3.6V	2.3V to 5.5V	+25℃			±0.5	μA
					Full			±1	
I_{CCA}	V_{CCA} Supply Current	V_I=VO=open I_O=0	1.65V to V_{CCB}	2.3v to 5.5V	Full			2.5	μA
			3.6v	0V	Full			2.5	
			0v	5.5V	Full			-1	
I_{CCB}	V_{CCB} Supply Current	V_I=V_O=open I_O=0	1.65V to V_{CCB}	2.3v to 5.5V	Full			10	μA
			3.6v	0V	Full			-1	
			0v	5.5V	Full			1	
I_{CCA} + I_{CCB}	Combined Supply Current	V_I=V_{CCI} or GND I_O=0	1.65V to V_{CCB}	2.3v to 5.5V	Full			13	μA
I_{CCZA}	V_{CCA} Supply Current	V_I=V_{CCI} or 0V I_O=0, OE=0V	1.65V to V_{CCB}	2.3v to 5.5V	Full			1	μA
I_{CCZB}	V_{CCB} Supply Current	VI=V_{CCI} or 0V I_O=0, OE=0V	2.3v to 3.6V	2.3v to 5.5V	Full			1	μA
C_i	Input Capacitance	OE	3.3V	3.3V	+25℃		2.5		pF
C_{io}	Input-to-output Internal Capacitance	A Port	3.3V	3.3V	+25℃		5		pF
		B Port	3.3V	3.3V	+25℃		5		

(1) V_{CCI} is the VCC associated with the input port.And V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCA} must be less than or equal to V_{CCB}.

7.2 Timing Requirements

V_{CCA}=1.8V ± 0.15V

		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Unit
		Typ	Typ	Typ	
Data Rate	Push-pull Driving	21	22	24	Mbps
	Open-drain Driving	2	2	2	
Pulse Duration(tw)	Push-pull Driving (Data Inputs)	47	45	41	ns
	Open-drain Driving (Data Inputs)	500	500	500	

V_{CCA}=2.5V ± 0.15V

		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Unit
		Typ	Typ	Typ	
Data Rate	Push-pull Driving	20	22	24	Mbps
	Open-drain Driving	2	2	2	
Pulse Duration(tw)	Push-pull Driving (Data Inputs)	50	45	41	ns
	Open-drain Driving (Data Inputs)	500	500	500	

V_{CCA}=3.3V ± 0.15V

		V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Unit
		Typ	Typ	
Data Rate	Push-pull Driving	23	24	Mbps
	Open-drain Driving	2	2	
Pulse Duration(tw)	Push-pull Driving (Data Inputs)	43	41	ns
	Open-drain Driving (Data Inputs)	500	500	

7.3 Switching Characteristics: V_{CCA}=1.8V±0.15V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Units
				Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	Push-pull Driving	5.6	5	5	ns
			Open-drain Driving	7.5	7.9	8.3	
t_{PLH}	Propagation Delay Time low-to-high Output	A to B	Push-pull Driving	10.0	9.5	9	ns
			Open-drain Driving	181	170	154	
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	Push-pull Driving	7	7.1	7.2	ns
			Open-drain Driving	7.6	8.1	9.2	
t_{PLH}	Propagation Delay Time low-to-high Output	B to A	Push-pull Driving	7.6	6.9	6	ns
			Open-drain Driving	163	145	118	
t_{en}	Enable Time	OE to A or B		135	159	182	ns
t_{dis}	Disable Time	OE to A or B		170	174	181	ns
t_{rA}	Input Rise Time	A port rise time	Push-pull Driving	13.4	11.9	10.6	ns
			Open-drain Driving	68	66	62	
t_{rB}	Input Rise Time	B port rise time	Push-pull Driving	13	12	11.6	ns
			Open-drain Driving	66	65	50	
t_{fA}	Input Fall Time	A port fall time	Push-pull Driving	5.6	4.7	4.0	ns
			Open-drain Driving	5.0	5.1	5.2	
t_{fB}	Input Fall Time	B port fall time	Push-pull Driving	3.0	3.0	2.9	ns
			Open-drain Driving	6.1	5.6	4.4	
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew		0.5	0.5	0.5	ns
Maximum Data Rate		Push-pull Driving		22	23	24	Mbps
		Open-drain Driving		2	2	2	

7.4 Switching Characteristics, V_{CCA}=2.5V±0.15V

over operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Units
				Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	Push-pull Driving	3.5	3.5	3.2	ns
			Open-drain Driving	6.3	6.5	6.7	
t_{PLH}	Propagation Delay Time low-to-high Output	A to B	Push-pull Driving	4.5	4.9	4.7	ns
			Open-drain Driving	158	152	142	
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	Push-pull Driving	3.7	3.9	4.6	ns
			Open-drain Driving	6	6.6	7.7	
t_{PLH}	Propagation Delay Time low-to-high Output	B to A	Push-pull Driving	4.8	4	2.5	ns
			Open-drain Driving	153	138	116	
t_{en}	Enable Time	OE to A or B		7.7	41.8	130	ns
t_{dis}	Disable Time	OE to A or B		175	181	182	ns
t_{rA}	Input Rise Time	A port Rise Time	Push-pull Driving	9.8	8.6	7.5	ns
			Open-drain Driving	79	77	65	
t_{rB}	Input Rise Time	B port Rise Time	Push-pull Driving	9.8	8.7	8.1	ns
			Open-drain Driving	93	68	53	
t_{fA}	Input Fall Time	A port Fall Time	Push-pull Driving	4.6	4.1	3.6	ns
			Open-drain Driving	5.1	5.1	5.2	
t_{fB}	Input Fall Time	B port Fall Time	Push-pull Driving	4.5	4.0	4.0	ns
			Open-drain Driving	6.9	7.4	7.8	
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew		0.5	0.5	0.5	ns
Maximum Data Rate		Push-pull Driving		22	24	24	Mbps
		Open-drain Driving		2	2	2	

7.5 Switching Characteristics, VCCA=3.3V±0.3V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Units
				TYP	TYP	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	Push-pull Driving	2.1	2.2	ns
			Open-drain Driving	5.9	6.1	
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	Push-pull Driving	1	3.3	ns
			Open-drain Driving	138	131	
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	Push-pull Driving	2.3	2.6	ns
			Open-drain Driving	5.4	6.6	
t_{PLH}	Propagation delay time low-to-high Output	B to A	Push-pull Driving	1.0	1.0	ns
			Open-drain Driving	133	115	
t_{en}	Enable Time	OE to A or B		4.7	5.2	ns
t_{dis}	Disable Time	OE to A or B		174	182	ns
t_{rA}	Input Rise Time	A port Rise Time	Push-pull Driving	7.4	6.6	ns
			Open-drain Driving	75	67	
t_{rB}	Input Rise Time	B port Rise Time	Push-pull Driving	7.7	7.1	ns
			Open-drain Driving	70	65	
t_{fA}	Input Fall Time	A port Fall Time	Push-pull Driving	3.4	3.0	ns
			Open-drain Driving	5.1	5.1	
t_{fB}	Input Fall Time	B port Fall Time	Push-pull Driving	3.5	3.2	ns
			Open-drain Driving	6.8	6.7	
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew		0.5	0.5	ns
Maximum Data Rate		Push-pull Driving		24	24	Mbps
		Open-drain Driving		2	2	

8 Typical Characteristics

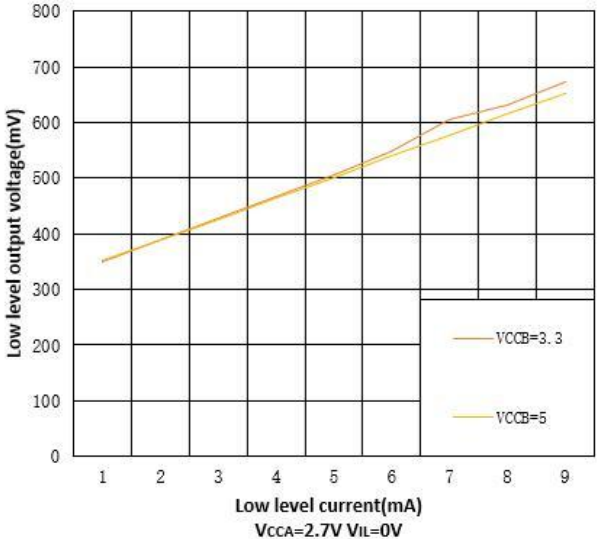


Fig.8-1. Low Level Output Voltage vs Low Level Current

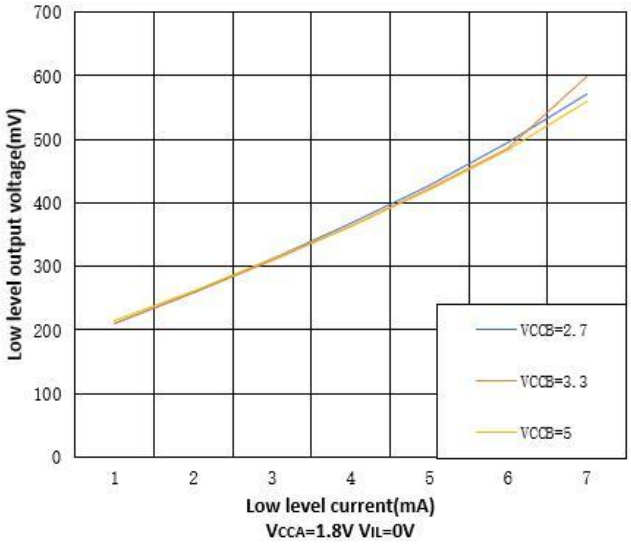


Fig.8-2. Low Level Output Voltage vs Low Level Current

9 Parameter Measurement Information

Unless otherwise noted, all input pulsed are supplied by generators having the following characteristics:

- PSRR 10MHz
- Zo=50 Ω
- dv/dt ≥1V/ns

Note: All input pulses are measured one at a time with one transition per measurement

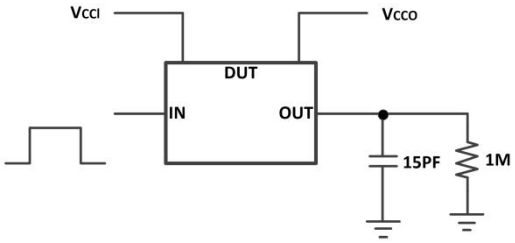


Fig.9-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise and Fall Time Measurement Using a Push-Pull Driver

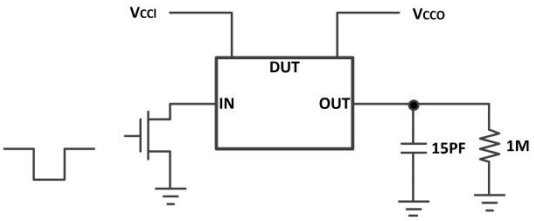


Fig.9-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise and Fall Time Measurement Using an Open-Drain Driver

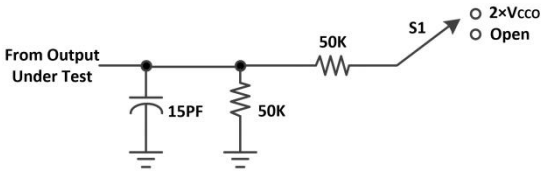


Fig.9-3. Load Circuit for Enable/Disable Time Measurement

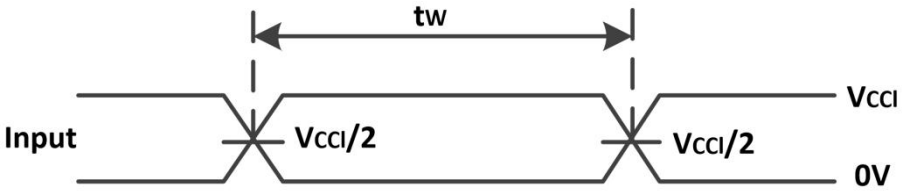
Table 9-1 Switch Configuration for Enable/Disable Timing

Test	S1
$t_{PZL}^{(1)}$, $t_{PLZ}^{(2)}$	$2\times V_{CCO}$
$t_{PZH}^{(1)}$, $t_{PHZ}^{(2)}$	Open

(1) t_{PZL} and t_{PZH} are the same as t_{en}.

(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

9 Parameter Measurement Information(Continued)



(1) All input pulses are measured one at a time, with one transition per measurement.

Fig.9-4. Voltage Waveforms Pulse Duration

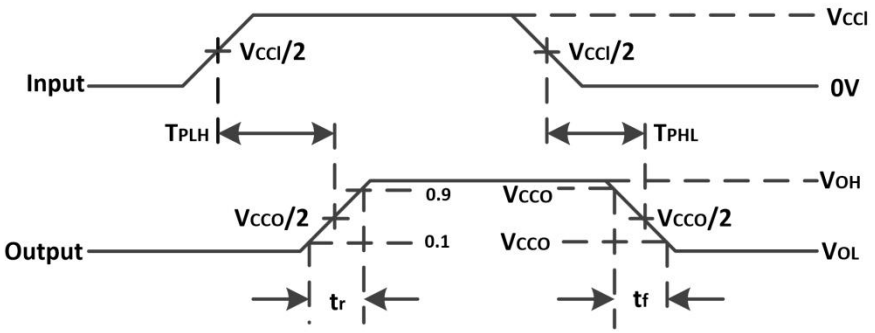


Fig.9-5. Voltage Waveforms Propagation Delay Times

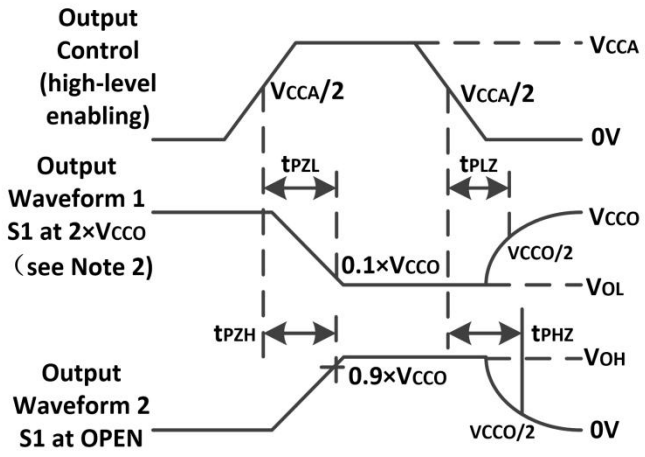


Fig.9-6. Voltage Waveforms Enable and Disable

10 Detailed Description

10.1 Overview

The WB0102 IC is a Bi-direction voltage-level translator specifically designed for translating logic voltage levels. The A port can accept I/O voltages that cover from 1.65 V to 3.6 V range; The B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10-kΩ pullup resistors that usually used in open-drain applications have been integrated inside IC with the advantage saving an external resistor. Not only the IC is designed for open-drain applications, but also this device can translate push-pull CMOS logic outputs.

10.2 Architecture

The WB0102 architecture (see Figure below) is a translator with Bi-direction-Sensing function that means a direction- control mechanism to control the direction of data flow from A to B or from B to A is not needed. These two bidirectional channels independently determine the direction of data flow without a direction-control signal. This auto- direction feature is realized by each I/O pin can be automatically reconfigured as either an input or an output.

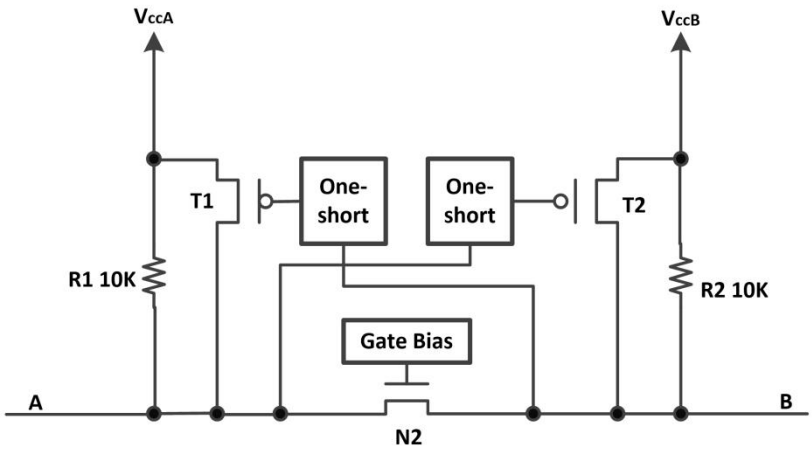


Fig.10-1. Architecture of WB0102

11 Application Information

The WB0102 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I2C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the WB0102 might be a better option for such push-pull applications.

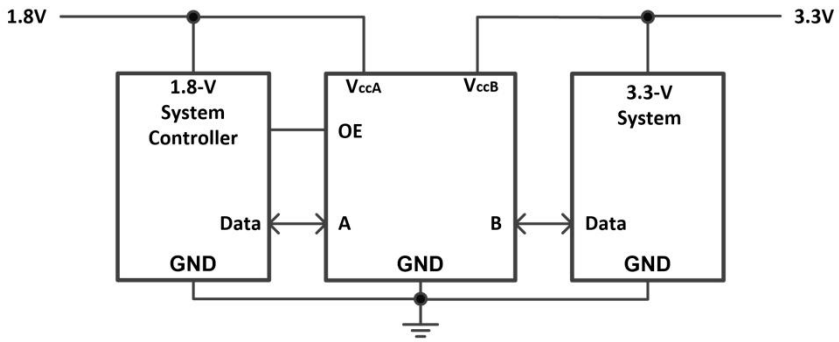
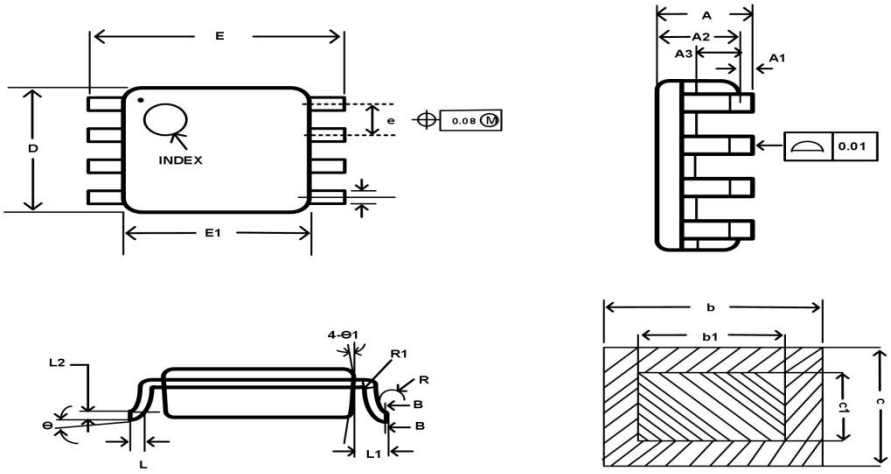


Fig.11-1. Typical Application Schematic

12 Package Outline Dimension

VSSOP8



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.90	-	-	0.035
A1	0	0.05	0.10	0.000	0.002	0.004
A2	0.65	0.75	0.80	0.026	0.030	0.031
A3	0.32	0.37	0.42	0.013	0.015	0.017
b	0.17	-	0.27	0.007	-	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	-	0.18	0.004	-	0.007
c1	0.10	0.13	0.14	0.004	0.005	0.006
D	1.90	2.00	2.10	0.075	0.079	0.083
E	3.00	3.10	3.20	0.118	0.122	0.126
E1	2.20	2.30	2.40	0.087	0.091	0.094
e	0.40	0.50	0.60	0.016	0.020	0.024
L	0.20	0.26	0.35	0.008	0.010	0.014
L1		0.40REF			0.016REF	
L2		0. 12BSC			0.005BSC	
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ	0°	-	6°	0°	-	6°
θ1	9°	12°	15°	9°	12°	15°

Notes For Attention

- When making the purchase, please ensure you recognize the company's trademark. If you have any questions, please contact the company's headquarters.
- When designing the circuit, please do not exceed the absolute maximum ratings of the components; otherwise, it will affect the reliability of the entire machine.
- This manual may be subject to changes in version without further notice.
- WaferBest assumes no obligation for application assistance or customer product design. The provided design solutions and materials are for reference only. Customers are responsible for the use of our products and applications by themselves. To minimize risks related to customer products and applications, customers should conduct thorough design verification, small-scale trial production, large-scale trial production, and operational safety measures.