Digital Dual-Phase Interleaved PFC Controller with I2C & UART Interfaces

Hynetek Semiconductor Co., Ltd.

HP1011

FEATURES

Digital dual-phase interleaved PFC controller with inherent current matching

High flexibility digital PWM

- PWM frequency ranges from 20 kHz to 200 kHz
- Switching frequency spread spectrum for improved EMI

High performance control loop

- 25 MHz sigma-delta ADC for line voltage and current sense, 12.5 MHz sigma-delta ADC for output voltage
- Enhanced dynamic loop response
- Input voltage feedforward
- Support HVDC input

Multi−mode operations

- Continuous Conduction Mode (CCM) in heavy load Conditions
- Discontinuous Conduction Mode (DCM) in light load conditions
- Burst mode in the zero load conditions

Advanced control functions

- True RMS power metering
- Inrush current control with programming relay delay
- Two channels X-cap discharge during shut down
- Dynamic current balancing between two phases

Extensive fault protections

- Fast over-voltage protection
- Bulk under-voltage protection and over-voltage protection
- External NTC thermal protection
- Cycle−by−cycle current limit
- Average switching current protection

Built-in 1 kBit MTP to store custom configurations

Low power consumption

I^2C and UART interfaces

Programming via easy-to-use Graphical User Interface (GUI)

Available in QFN-24L packages

-40°C to 125°C operating temperature

APPLICATIONS

Ultra−High Density Power Supplies

LED Lighting

Industrial Power Supplies

Server/Telecom

EV/E-Bike Charger

Supercomputing

Variable-Frequency Drivers (VFD)

GENERAL DESCRIPTION

The HP1011 is a highly flexible digital Power Factor Correction (PFC) controller designed to drive the dual phase interleaved PFC stage.

A rectified diode bridge and dual-phase interleaved boost converter each has a fast-switching leg driven at the PWM switching frequency and a fast-recovery diode make up the dual-phase interleaved PFC. HP1011 supports shut-down one PWM channel under light load condition which can achieve high efficiency at light load.

The HP1011 offers RMS value of input voltage, current, and power. Through the I^2C and UART interfaces, this information can be communicated to a microcontroller.

The HP1011 operates from a single 3.3 V supply. The device is available in 4 mm x 4 mm QFN-24L package specified over an ambient temperature range of −40°C to +125°C.

TYPICAL APPLICATION CIRCUIT

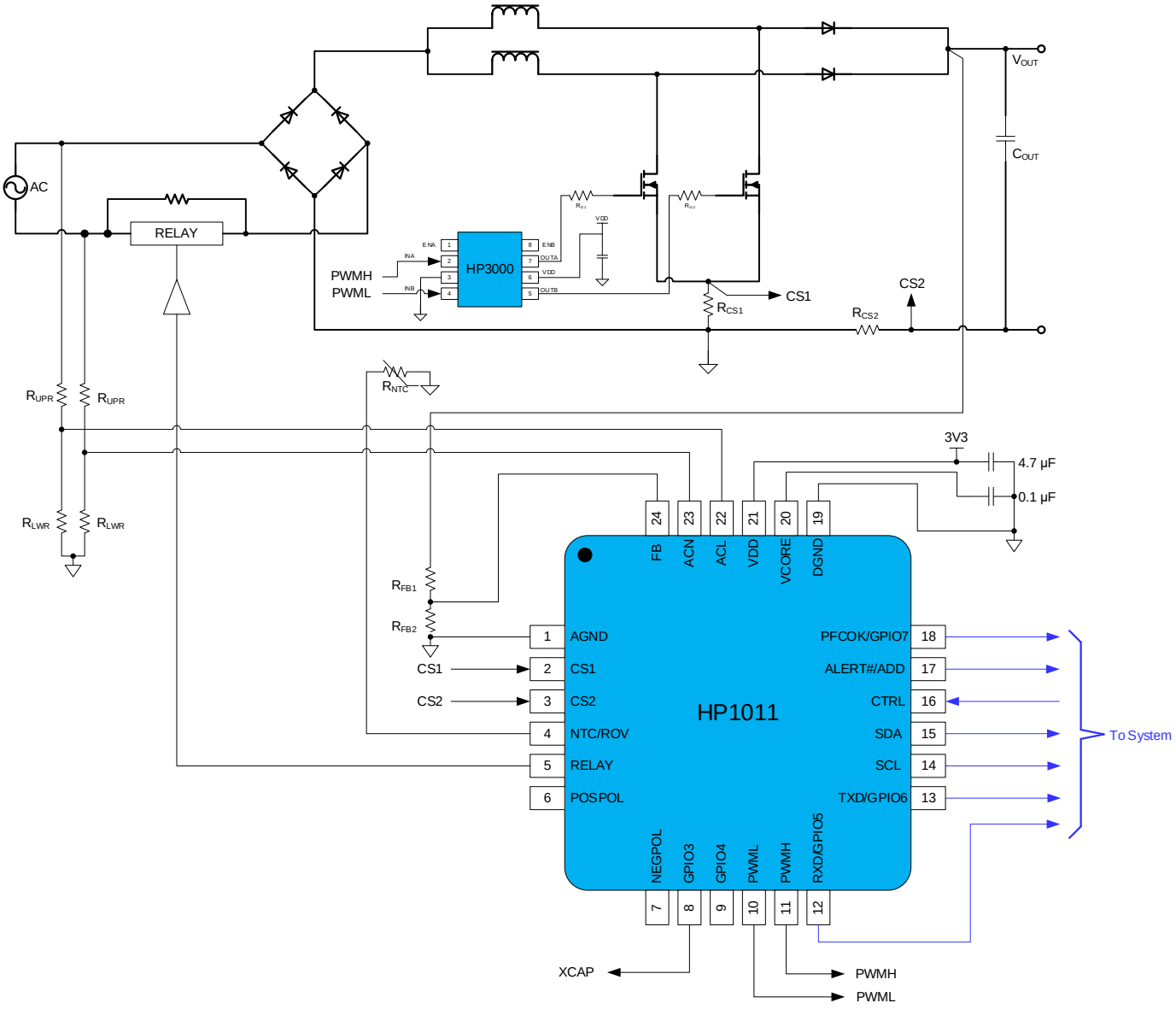


Figure 1 Typical Application Circuit

TABLE OF CONTENTS

REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	03/2024	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

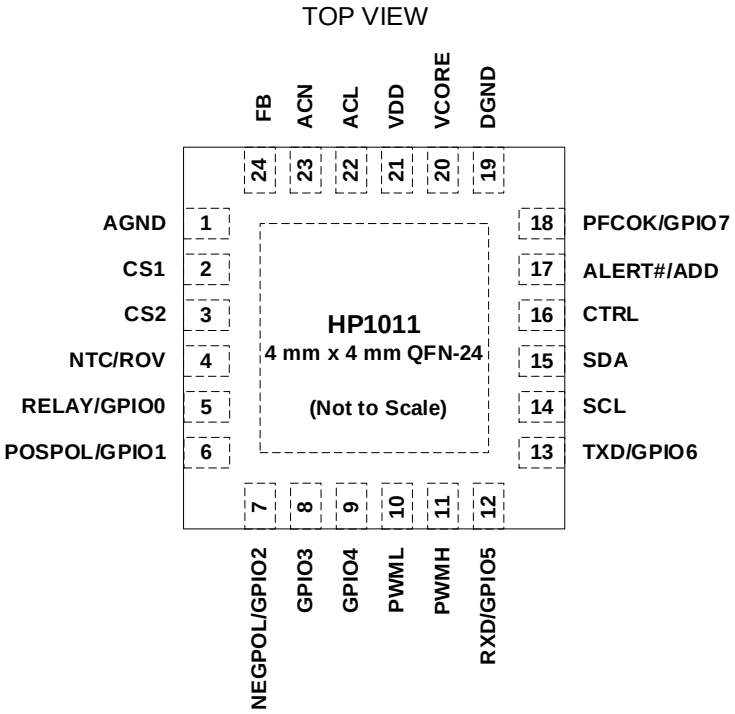


Figure 2 HP1011-BA000-QN24R Pin Configuration

Table 1. Pin Function Descriptions

Pin No.	Name	Type[1]	Primary Function	GPIO
1	AGND	P	Analog ground. AGND should be connected directly to DGND.	
2	CS1	AI	This pin senses the inductor current upslope through current sense transformers or sense resistor in the DIPFC topology. It is used to reconstruct the inductor current. It is also used for cycle−by−cycle current limiting. The signal is referred to AGND.	
3	CS2	AI	The pin optionally senses the inductor current downslope. The signal is referred to AGND.	
4	NTC/ROV	AI	Dual function for this pin. NTC: Temperature sense input, which is inverse proportional to the temperature, triggers the comparator when OTP happens. ROV: redundant OVP comparator with a programmable reference. The signal is referred to AGND.	
5	RELAY/GPIO0	DO	Relay control output. The response delay can be programmed. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
6	POSPOL	DO	Output of the internal AC polarity detection circuit. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
7	NEGPOL	DO	Inverted output of the internal AC polarity detection circuit. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
8	GPIO3	DO	General-purpose IO. The signal is referred to AGND.	Yes
9	GPIO4	DO	General-purpose IO. The signal is referred to AGND.	Yes
10	PWML	DO	PWM logic level output for control of channel 1 switch. The signal is referred to DGND.	
11	PWMH	DO	PWM logic level output for control of channel 2 switch. The signal is referred to DGND.	

Pin No.	Name	Type[1]	Primary Function	GPIO
12	RXD/GPIO5	DIO	UART_RX pin. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
13	TXD/GPIO6	DIO	UART_TX pin. The signal is referred to DGND. It can be re-used as GPIO pin.	Yes
14	SCL	AIO	I^2C serial clock line. The SCL signal is referred to DGND.	
15	SDA	AIO	I^2C serial data line. The SDA signal is referred to DGND.	
16	CTRL	DI	Remote control pin. The signal is referred to DGND.	
17	ALERT#/ADD	DIO	I^2C alert pin. The signal is referred to DGND. During the power on reset, the state of this pin is sampled as address select input for I^2C bus. Note: a 900 kΩ resistor should be used when connecting to VDD or DGND to reduce standby current. The signal is referred to DGND. HIGH = I^2C address is 0x67 LOW = I^2C address is 0x47	
18	PFCOK/GPIO7	DIO	The PFCOK/GPIO supports dual functions. The PFCOK function is held low when the PFC output voltage is out of regulation and during fault conditions. It is push−pull output. It can be re-used as GPIO pin.	Yes
19	DGND	P	Digital Ground. DGND should be connected directly to AGND.	
20	VCORE	P	1.8 V VDD for digital core. The VCORE signal is referred to DGND. Connect a 100 nF capacitor from VCORE to DGND.	
21	VDD	P	3.3 V main supply input. The VDD signal is referred to AGND. Connect a 4.7 μF capacitor from VDD to AGND.	
22	ACL	AI	AC line voltage sense. The signal is referred to AGND.	
23	ACN	AI	AC neutral voltage sense. The signal is referred to AGND.	
24	FB	AI	PFC output voltage sense for loop regulation. The signal is referred to AGND.	

[1] Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{DD} = 3.3 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2. Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Operating Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3	3.3	3.6	V
Supply Current	I_{DD}	Normal operation		10.0		mA
Peak Supply Current	I_{DD_PK}	While programming			7.5	mA
Shutdown Current	I_{DD_SD}	PFC off state		8.1		mA
Sleep Mode Current	I_{DD_SM}	Sleep mode enabled.		1.0		mA
POWER-ON RESET						
Power-on Reset	V_{DD_POR}	V_{DD} rising	2.7	2.8	2.9	V
UVLO	V_{DD_UVLO}	V_{DD} falling	2.6	2.7	2.8	V
VCORE PIN						
Output Voltage	V_{CORE}	100 nF capacitor connected to DGND	1.7	1.8	1.9	V
OSCILLATOR, CLOCK, PLL						
Oscillator Frequency	f_{OSC}		11.875	12.5	13.125	MHz
PLL Frequency	f_{PLL}		190	200	210	MHz
Digital PWM Resolution	t_{PWM_RES}	For PWML and PWMH pins		5		ns
PWMH, PWML, GPIO3, GPIO4, POSPOL, NEGPOL, RELAY PINS						
Output Low Voltage	V_{PWMOL}	Sink current = 10 mA			0.4	V
Output High Voltage	V_{PWMOH}	Source current = 10 mA	V_{DD}-0.4			V
Rise time	t_{RISE}	Cload= 50 pF		4.0		ns
Fall time	t_{FALL}	Cload= 50 pF		4.0		ns
Output Source Current	I_{OL}		-10			mA
Output Sink Current	I_{OH}				10	mA
SWITCHING FREQUENCY						
Frequency Range	f_{SW}	See Table 9	20		195	kHz
Accuracy			-3%		3%	
ACN AND ACL PINS						
External Divider Ratio	$K_{AC\_DIV\_EXT}$			1/200		
Input Voltage Range	V_{AC}		0		2.8	V
Input Impedance	R_{AC}		400	500		kΩ
Amplifier GBW	GBW_{AC}			2		MHz
Amplifier Gain	G_{AC_OP}			0.5		
ADC						
ADC range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Data updating frequency 25 kHz		10		Bits
Voltage Sense Accuracy		10% to 90% of usable range	-1.3		2.0	%FSR
Positive Comparator for VIN On						

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Threshold Range[1]	V_{AC_POS}		200	320	480	mV
Threshold Accuracy		Factory trimmed at 320 mV	280	320	355	mV
Resolution				3		Bits
LSB				40		mV
Hysteresis			30	45	70	mV
Propagation Delay					1.0	µs
Negative Comparator for VIN On						
Threshold Range[1]	V_{AC_NEG}		-0.2	-0.32	-0.48	V
Threshold Accuracy		Factory trimmed at -320 mV	-360	-318	-285	mV
Resolution				3		Bits
LSB				40		mV
Hysteresis Width				40		mV
Propagation Delay					1.0	µs
Positive Comparator for Surge						
Threshold Range[1]	V_{AC_PSUR}		1.6	1.9	2.2	V
Threshold Accuracy		Factory trimmed at 1.9 V	-2.32		1.16	%
Resolution				4		Bits
LSB				40		mV
Hysteresis			110	135	165	mV
Propagation Delay					1.0	µs
AC Line Frequency Monitor						
High Threshold	f_{5060_H}		68	70	72	Hz
Lower Threshold	f_{5060_L}		37	40	43	Hz
Detection Timer	N_{LINE_DET}			4		cycles
Exceed Timer	$N_{LINE\_FREQ\_EXC}$			4		cycles
Brown-out and SAG						
Vin On Threshold	V_{IN_ON}	Programmable, KAC_DIV_EXT=1/200	0	78	255	VAC
Vin Off Threshold	V_{IN_OFF}	Programmable, KAC_DIV_EXT=1/200	0	71	255	VAC
Brown-out Debounce	t_{BO_DEB}		-	0.5	-	cycles
Line Sag Timeout Range	t_{SAG_TO}	Programmable 4 to 32 AC cycles	4	12	32	cycles
High/Low Line Detection						
High Threshold	V_{HLINE}	Programmable, KAC_DIV_EXT=1/200	120	168	180	VAC
Low Threshold	V_{LLINE}	Programmable, KAC_DIV_EXT=1/200	120	156	180	VAC
High Line to Low Line Debounce Time	t_{H2L_DED}		20	25	30	ms
VAC ZERO CROSSING DETECTION						
VAC Zero Detection Comparator		Between ACL Pin to ACN pin				
Threshold	V_{POL_DET}		-0.01	0	0.01	V
Hysteresis Width	V_{POL_HYS}			10		mV
Propagation Delay	t_{POL_PD}				1.0	µs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Polarity Detection						
Propagation Delay				5		µs
VIN_POL Detection Debounce	t_{POL_DEB}		20	200	320	µs
VIN_POL Detection LSB				20		µs
FB PIN						
External Divider Ratio	$K_{FB\_DIV\_EXT}$			1/200		
Input Voltage			0		2.8	V
Input Impedance			500			kΩ
Amplifier GBW				2		MHz
Amplifier Gain				0.5		
ADC						
ADC Range			0		1.4	V
ADC Clock Frequency				12.5		MHz
Equivalent Resolution				11		Bits
Voltage Sense Accuracy		10% to 90% of usable range	-1.3		1.5	%FSR
Fast Over-Voltage Protection						
Threshold Range[1]	$V_{FB\_FOV\_LIM}$		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-0.86		1.64	%
Resolution				6		Bits
Hysteresis			110	135	160	mV
Propagation Delay	$t_{FB\_FOV\_PD}$				160	ns
Debounce Time	$t_{FB\_FOV\_DB}$	Programmable in 4 steps	40		100	µs
Blanking time	$t_{FB\_FOV\_BK}$			10		µs
Open Loop Protection						
Sink Current	I_{FB_SNK}			250		nA
Threshold	V_{FB_OL}		20		88	V
Hysteresis	V_{FB_OLHYS}			18		V
Debounce Time	t_{FB_OLDB}	Programmable in 4 steps	0		30	ms
Slow Over-Voltage Protection						
Threshold	$V_{FB\_SOV\_LIM}$		V_{REF}		V_{REF}+68	V
Resolution				5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SOV\_DB}$		0		30	ms
Slow Under-Voltage Protection						
Threshold			V_{REF}-68		V_{REF}	V
Resolution	$V_{FB\_SUV\_LIM}$			5		Bits
Accuracy			-2		+2	%
Debounce Time	$t_{FB\_SUV\_DB}$		0		30	ms
CS1 AND CS2 PINS						
Input Voltage			0		1.4	V
Input Impedance			1			MΩ
Amplifier						
GBW				2		MHz

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gain				1		
ADC						
High Input Voltage Range			0		1.4	V
ADC Clock Frequency				25		MHz
Equivalent Resolution		Updating frequency at 100 kHz		8		Bits
Current Sense Accuracy		10% to 90% of usable range	-1.5		2.0	%FSR
CS1 Fast Over Current Protection						
Threshold Range[1]	$V_{CS1\_OC\_LIM}$		1.0	1.25	1.5	V
Threshold Accuracy		Factory trimmed at 1.25 V	-1.2		0.48	%
Resolution				6		Bits
LSB				7.8		mV
Hysteresis			15	25	35	mV
Propagation Delay					100	ns
Blanking Time		Programmable in 4 steps	480		1920	ns
Debounce Time		Programmable in 4 steps	40		160	ns
CS2 Zero Crossing Detection						
Threshold Range[1]	V_{CS2_ZCD}		-100	22.4	48	mV
Threshold Accuracy		Factory trimmed at 22.4 mV	12.5	22.4	33.5	mV
Resolution				6		Bits
LSB				3.2		mV
Hysteresis			35	50	75	mV
Propagation Delay					100	ns
CTRL PIN						
Input High Voltage	V_{CTRL_IL}				0.8	V
Input Low Voltage	V_{CTRL_IH}		2.0			V
Debounce Time	t_{CTRL_DEB}			10		μs
Leakage Current	i_{CTRL_LK}				1.0	μA
PFCOK, ALERT#/ADD PINS						
Output Low Level					0.8	V
Output High Level			2.0			V
Debounce Time			0		600	ms
OVER AVERAGE SWITCHING CURRENT PROTECTION						
Average OCP Threshold		CS1 Sense ratio is 10:1	0		7	A
Resolution				7		Bits
Accuracy			-2		+2	%
Debounce				2		Switch cycle
NTC/ROV PIN						
Current Source	I_{NTC}		43	46	49	μA
Over-temperature Threshold	V_{NTC_OT}		0.36	0.4	0.41	V
OT Recover Threshold	V_{NTC_REC}		0.78	0.8	0.82	V
Debounce Time	t_{NTC_DEB}	Programmable in 2 steps		500	1000	ms

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Redundant Over-Voltage Protection						
Threshold Range[1]	V_{ROV_LIM}		1.9	2.2	2.5	V
Threshold Accuracy		Factory trimmed at 2.2 V	-2.00		1.64	%
Resolution				6		Bits
Hysteresis			115	135	160	mV
Propagation Delay					160	ns
Debouncing Time		Programmable in 4 steps	40		100	µs
Blanking Time		Blanking after threshold re-programming		10		µs
SDA/SCL PINS						
Input Voltage Low					0.8	V
Input Voltage High			2.2			V
Output Voltage Low					0.4	V
Pull-Up Current			100		350	µA
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						
Clock Frequency	f_{IIC}				400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			µs
Start Setup Time	t_{SU_STA}		4.7			µs
Start Hold Time	t_{HD_STA}		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_{R_I2C}				1000	ns
SCL, SDA Fall Time	t_{F_I2C}				300	ns
Data Setup Time	t_{SU_DAT}		250			ns
Data Hold Time	t_{HD_DAT}		300			ns
TXD/RXD PINS (UART)						
Baud Rate	f_{UART}	Programmable with (0:9600; 1: 1200; 2: 57600; 3: 115200)	1200	9600	115200	bps
Data Length				8		
Stop Bits				1		
Polarity Check Bit				1		
EEPROM RELIABILITY						
Endurance		T_A = 85°C	10,000			Cycles
		T_A = 125°C	1000			Cycles
Data Retention		T_A = 85°C	20			Years
		T_A = 125°C	15			Years

[1] The final range of thresholds will be determined by factor trimmed result.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum ratings

Parameter	Rating
VDD (Continuous)	4.2 V
ACL, ACN, FB, CS1, CS2, RELAY/GPIO0, NTC/ROV, POSPOL/GPIO1, NEGPOL/GPIO2, GPIO3, GPIO4, PWML, PWMH, RXD/GPIO5, TXD/GPIO6, SCL, SDA, CTRL, PFCOK/GPIO7, ALERT#/ADD	-0.3 V to VDD + 0.3 V
VCORE	2 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model	±6000 V
Charge Device Model	±2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN4x4-24L	46	23	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

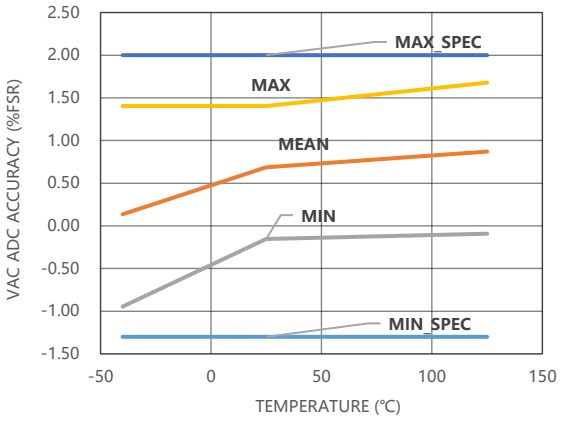


Figure 3 VAC ADC Accuracy vs. Temperature (from 10% to 90%)

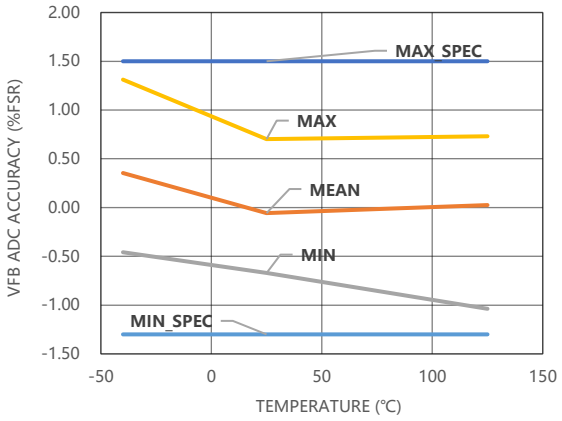


Figure 4 VFB ADC Accuracy vs. Temperature (from 10% to 90%)

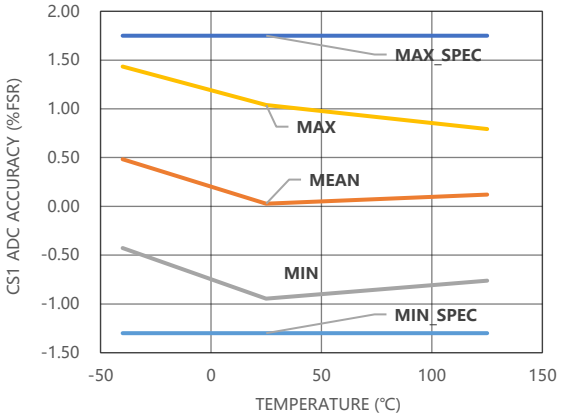


Figure 5 CS1 ADC Accuracy vs. Temperature (from 10% to 90%)

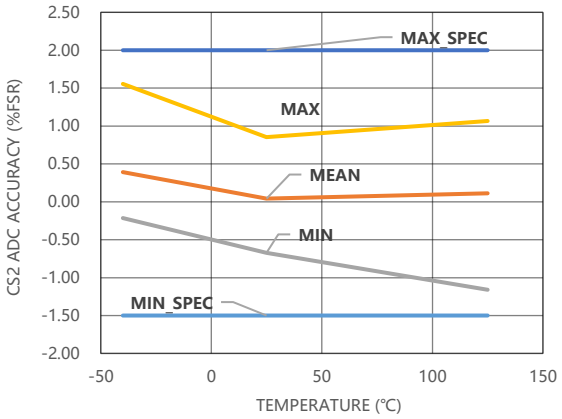


Figure 6 CS2 ADC Accuracy vs. Temperature (from 10% to 90%)

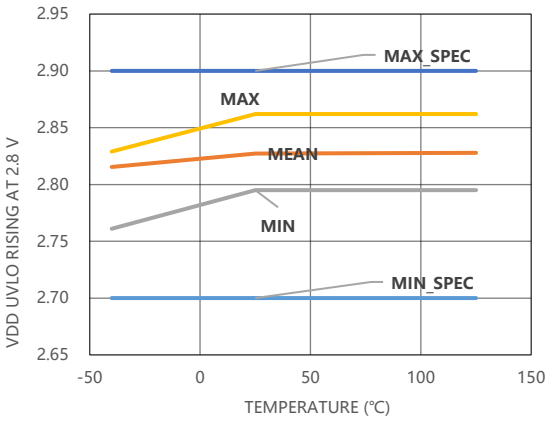


Figure 7 VDD UVLO Rising at 2.8 V vs. Temperature

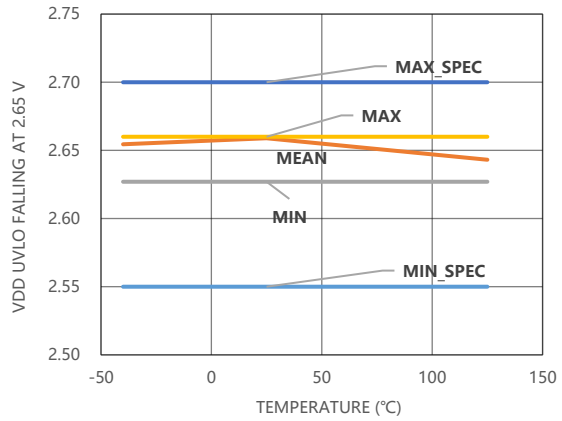


Figure 8 VDD UVLO Falling at 2.65 V vs. Temperature

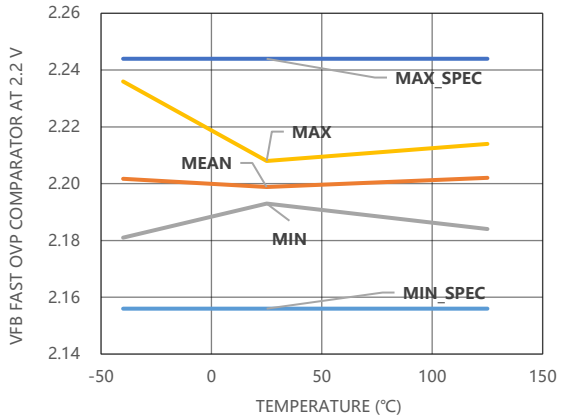


Figure 9 VFB Fast OVP Comparator at 2.2 V vs. Temperature

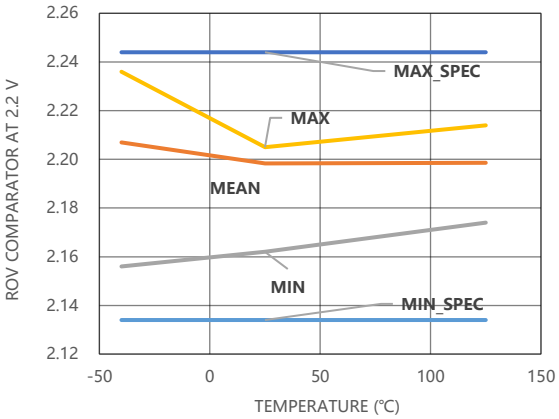


Figure 10 ROV Comparator at 2.2 V vs. Temperature

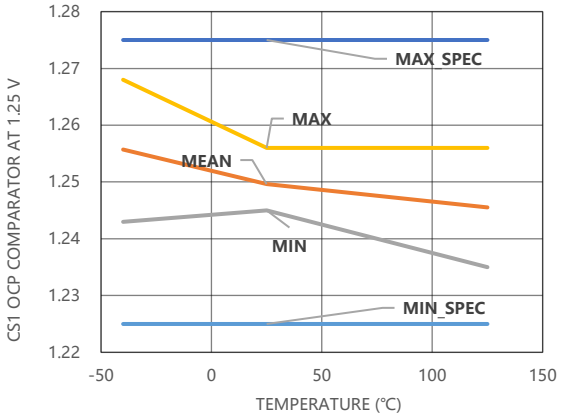


Figure 11 CS1 OCP Comparator at 1.25 V vs. Temperature

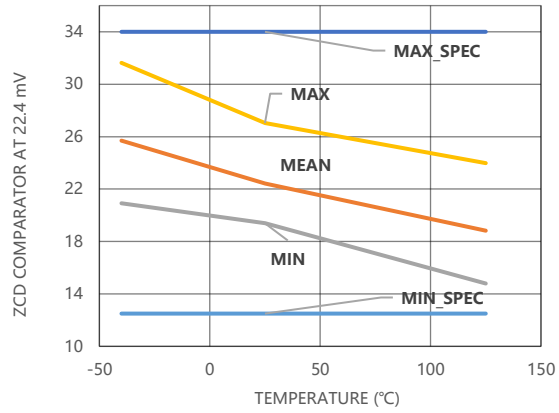


Figure 12 CS2 ZCD Comparator at 22.4 mV vs. Temperature

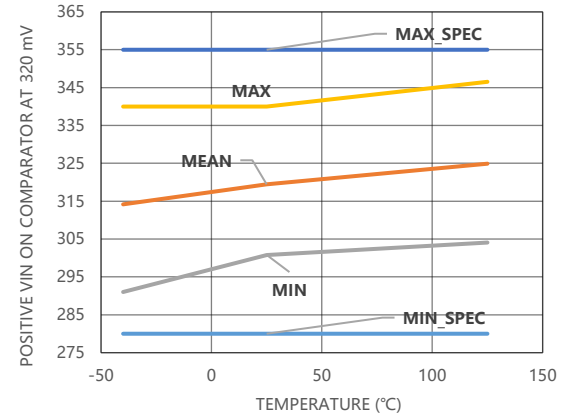


Figure 13 Positive VIN ON Comparator at 320 mV vs. Temperature

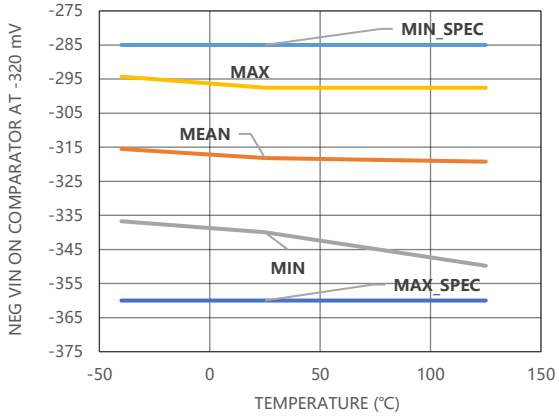


Figure 14 Negative VIN ON Comparator at -320 mV vs. Temperature

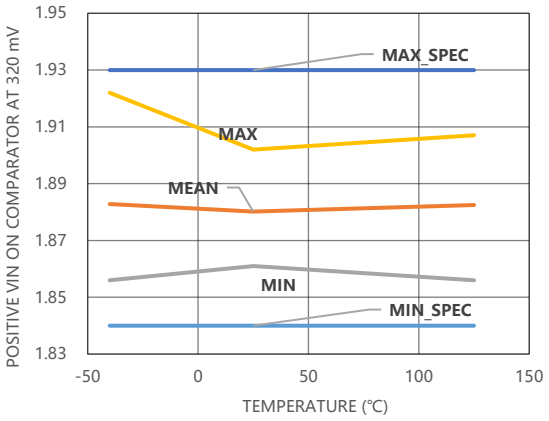


Figure 15 Positive Surge Comparator at 1.9 V vs. Temperature

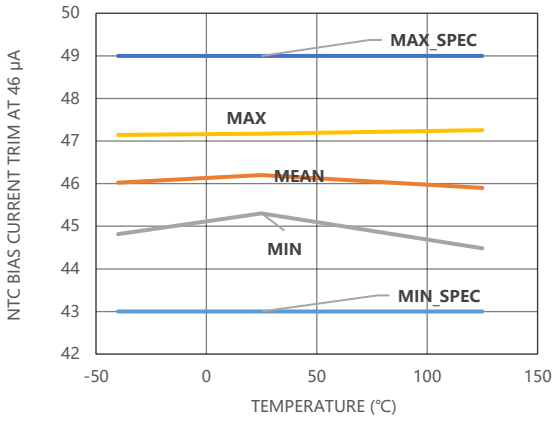


Figure 16 NTC Bias Current at 46 µA vs. Temperature

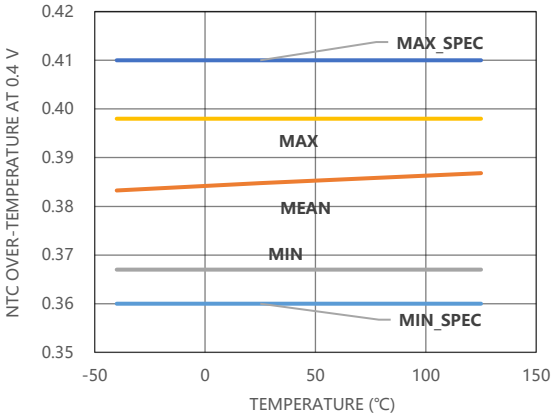


Figure 17 NTC Over-Temperature at 0.4 V vs. Temperature

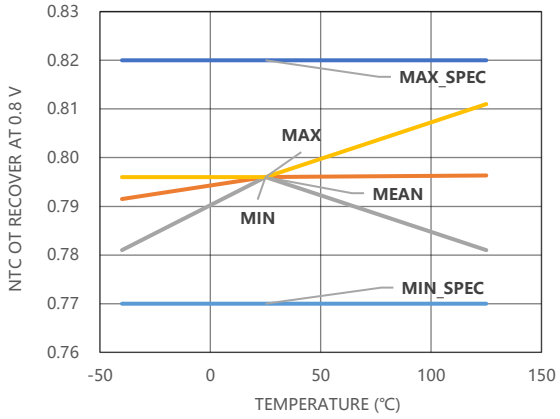


Figure 18 NTC Over-Temperature Recover at 0.8 V vs. Temperature

THEORY OF OPERATION

Figure 19 shows the overall control diagram for the dual-phase interleaved power factor correction. The voltage and current loop control are the same as conventional boost PFC converter. The feedback signals from the PFC power stage are the V_{FB}, V_{ACL}, V_{ACN}, I_{CS1} and I_{CS2}. The input voltage polarity and RMS value are determined from V_{ACL} and V_{ACN}. The outer voltage loop output multiplied by |VAC| gives sinusoidal current reference. Current loop gives the proper duty-ratio for boost circuit.

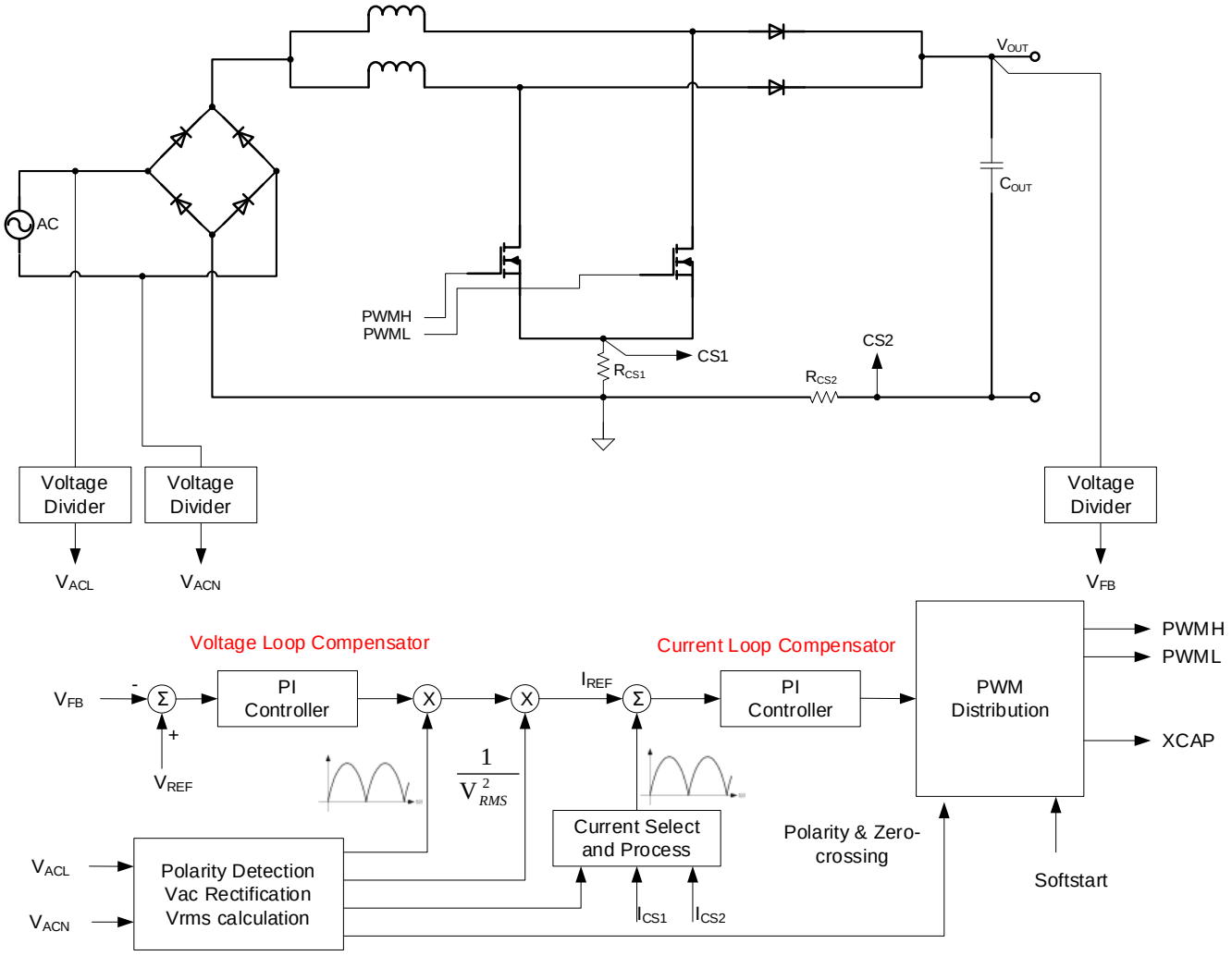


Figure 19 HP1011 Control Loop Scheme

VDD AND VCORE PINS

When the voltage of the VDD pin is applied (VDD), there is a delay before the part can regulate the power supply. When VDD voltage rises above the power-on reset and UVLO levels, it takes ~20 μs for the VCORE pin (Pin 23) to reach its operational point of 1.8 V. The EEPROM contents are then downloaded to the registers. After the EEPROM contents are downloaded, the HP1011 is ready for operation; however, it takes a maximum of 20 ms for the HP1011 to complete initialization of the address after a power-on reset. Therefore, it is recommended that the master device access the HP1011 at least 20 ms after power-on reset.

CTRL PIN AND SOFTWARE ENABLE

The HP1011 is in the PFC off state upon power-on reset. PFC_ON configuration can be enabled in one of four ways, depending on the setting:

- Always on whenever the input voltage is ready.

- Hardware CTRL only. Power on whenever the CTRL pin is pulled high, and the input voltage is ready.
- Software ENABLE only. Power on whenever the ENABLE bit in Register 0x00 is set and the input voltage is ready.
- Both hardware CTRL being pulled high, and software ENABLE bit being set to turn on the PFC when the input voltage is ready.

Once the PFC_ON flag is set, the HP1011 follows the state machine as shown in section Operation for details.

The CTRL pin has a control debounce of t_{CTRL_DEB}, which is 10 μs, for both the rising edge and falling edge. The CTRL pin is used to control the HP1011 from the second side controller via an optical coupler, as shown in Figure 20. The remote signal is generated from the second-side controller.

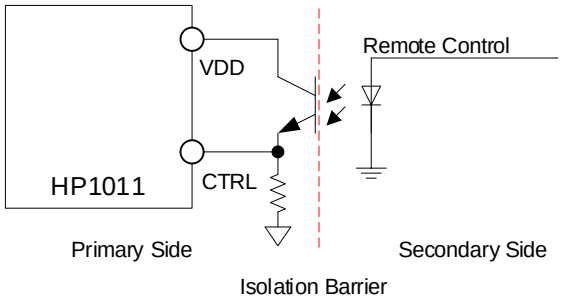


Figure 20 Remote Control Signal to Enable HP1011

INPUT AC VOLTAGE (ACL AND ACN PINS)

External resistor dividers are required to divide down two high voltage nodes to perform differential line sensing. The recommended divide down factor for universal input consumer applications is $K_{AC\_DIV\_EXT}$, typically 1/200.

$$K_{AC\_DIV\_EXT} = \frac{R_{LWR}}{R_{UPR}+R_{LWR}} \quad (1)$$

Such that the low-voltage signals that interface with the HP1011 are approximately 1% of the high-voltage signals that are being monitored. The ACL pin is intended to interface with the low-frequency node of the main boost inductor, L_{IN}, and the ACN pin is intended to interface with the bridge voltage of the slow-leg power switches. The internal line detector circuit is designed with substantially high input impedance, allowing for large external resistors to minimize the power dissipation in the dividers, enabling the application to achieve low no-load power consumption. Typical values for RUPR can be in the range of 993 kΩ, while R_{LWR} can be 4.99 kΩ. In practice, the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

Since there is an additional amplifier U2 with a gain of $K_{AC\_DIV\_INT}$ = 1/2. The total gain of line voltage sense to the ADC is:

$$K_{AC\_DIV} = K_{AC\_DIV\_EXT} \times K_{AC\_DIV\_INT} \quad (2)$$

Therefore K_{AC_DIV} = 1/400.

POLARITY DETECTION

The ACL and ACN pins sense signals are compared directly against each other to determine when they cross. The crossover of the two signals indicates that the AC line voltage has changed polarity. When the AC line is in a positive cycle, POSPOL is high and NEGPOL signal is low. When the AC line is in a negative cycle, POSPOL is low and NEGPOL signal is high.

External filter capacitance may be needed to improve the noise immunity of the polarity detection circuitry; the recommended time constant of the RC filter is about 20 to 200 μs, enough to provide noise immunity from the switching frequency of the power supply but not such a large time constant to introduce significant lag in the line sense signals.

The output of the polarity comparison circuit is passed through a digital debounce filter, which will provide additional immunity if the comparison circuit is toggling due to the noise. The debounce filter has a programmable debounce time, typical 200 μs.

AC LINE FREQUENCY MONITORING

The HP1011 supports different input line types, including 50 Hz/ 60 Hz AC input and DC input.

BROWN−OUT AND LINE SAG PROTECTION

The HP1011 features line voltage Brown−out (BO) and Line sag (SAG) detection. These detection circuits' function works as a line voltage UVLO, enabling drive pulses when the RMS voltage exceeds the V_{IN_ON} threshold, typically 78 VAC, and disabling drive pulses when the line voltage falls below the V_{IN_OFF} threshold, typically 71 VAC, for a given timer duration.

When the line voltage VAC voltage drops below VIN_OFF for a debounce of t_{BO_DEB}, which is half an AC cycle, the BROWN-OUT flag is trigged. The SAG timer, programmable from 4-cycle to 32-cycle from the BROWN-OUT flag being triggered, allows the application to sustain a line voltage dropout for a single or multiple AC line cycles while the controller continues to deliver drive pulses. Within the timer, if the output voltage drops below the output under-voltage limit, the VOUT_UV_FAULT will trigger protection action. If the input current exceeds the input peak current limit or the input average current limit, the IIN_PK_OC fault or the IIN_AV_OC fault will trigger protection actions. If the protection action is selected as fault recovery, since the BROWN_OUT flag is triggered, the HP1011 resets to Mode 0. If the SAG timer expires, the controller will reset to Mode 0 for a new start-up. Figure 21 shows the timing diagram for the Brown-out and SAG. The missing cycle between t_1 to t_0 is smaller than t_{BO_DEB}, the BROWN_OUT flag is not triggered.

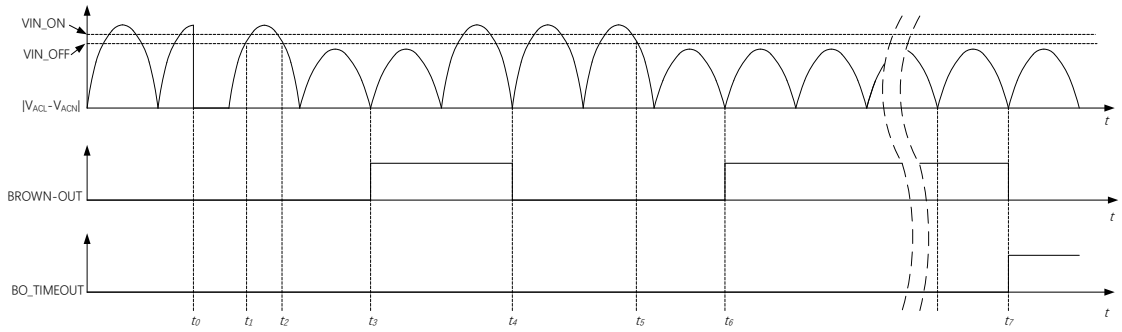


Figure 21 Brown-out and Sag Timing Diagram

LINE RANGE DETECTION

The HP1011 features input voltage range detection, which distinguishes between high line (nominally 230 VAC) and low line (nominally 115 VAC) input voltages. The input voltage range is detected based on the RMS value calculated with the VAC line signal. By default, the controller will power up into low line mode. If VAC exceeds the high line threshold, $V_{HLINE,}$ typically 168 V, for one half cycle, the controller transitions to high line mode. Once in high line mode the peak line voltage must fall below V_{LLINE}, typically 156 VAC, for a debounce longer than t_{H2L_DEB}, typically 25 ms, to enter back into the low line mode. The debounce duration, t_{H2L_DEB}, is set long enough to allow the controller to remain in high line mode in the event of a single line cycle dropout.

OUTPUT VOLTAGE (FB PIN)

REGULATION BLOCK

The bulk voltage is divided down via a resistor divider and input to an ADC, which converts the feedback voltage to a digital signal. This digital signal compares against a digital reference voltage. The recommended divide-down factor for universal output voltage sense is K_{FB_DIV}, typically 1/200.

$$K_{FB\_DIV\_EXT} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \quad (3)$$

Such that the low voltage signals which interface to the HP1011 are approximately 1% of the high voltage signals that are being monitored. Typical values for R_{FB1} can be in the range of 993 kΩ while R_{FB2} can be 4.99 kΩ. In practice the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

Since there is an additional amplifier with a gain of $K_{FB\_DIV\_INT}$ = 1/2. The total gain of output voltage sense to the ADC is:

$$K_{FB\_DIV} = K_{FB\_DIV\_EXT} \times K_{FB\_DIV\_INT} \quad (4)$$

Therefore K_{FB_DIV} = 1/400. During nominal condition, the output voltage is 400 V, resulting in FB pin sense voltage of 2 V and ADC input voltage of 1 V.

OUTPUT VOLTAGE REGULATION

In the HP1011, the output voltage can be regulated with a low line and a high line separately. As low-line and high-line reference, the regulation range is from 250 V to 505 V, with a nominal voltage of 400 V.

OUTPUT VOLTAGE PROTECTION FEATURES

The HP1011 features multiple protection and enhancement features for improved performance and robustness of the application. The slow OVP, fast OVP, slow UVP, and fast loop blocks monitor the sampled FB pin voltage.

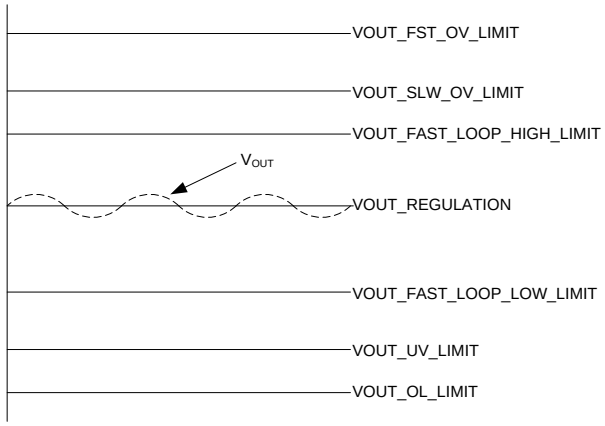


Figure 22 Output Voltage Protection Thresholds

CURRENT SENSE (CS1 AND CS2 PINS)

CURRENT SENSE METHODS

For the DIPFC topology, the HP1011 supports two current sense schemes:

1. Two current transformers + one sense resistor (2*CT+1*R_{sen})
2. Two sense resistors + one sense resistor (2*R_{sen}+1*R_{sen})

To achieve input and output current sense monitoring and protection, the CS1 and CS2 can be configured as Table 5 for correctly sense the input and output current.

Table 5. Input and Output Current Sense

Topology	Current Sense Scheme	Input Current Sense (via IIN_SENSE_METHOD)	Output Current Sense (via IOUT_SENSE_METHOD)
DIPFC	Scheme 1: 2*CT+1*R_{sen}	CS1+CS2	CS2
	Scheme 2: 2*R_{sen}+1*R_{sen}	CS1+CS2	CS2

Since different current sense components are used, the CS1 and CS2 current sense equivalent resistance can be selected as 6.25 mΩ, 12.5 mΩ, 25 mΩ, 50 mΩ, 100 mΩ, 200 mΩ and 400 mΩ. The goal to adopt different equivalent resistance is to optimize the usage of 1.4 V full range input ADC and achieve power saving. For example, in the current transformer method, if the turn ratio of CT1 and CT2 (N_P:N_S) is 1:100, and the R_{CS1} is 10 Ω, then the CS1 equivalent resistance is 1/100*10=100 mΩ.

CURRENT SENSE SCHEME 1: TWO CURRENT TRANSFORMERS + ONE SENSE RESISTOR FOR DIPFC TOPOLOGY

The current sense configuration used in this current scheme is illustrated in Figure 23.

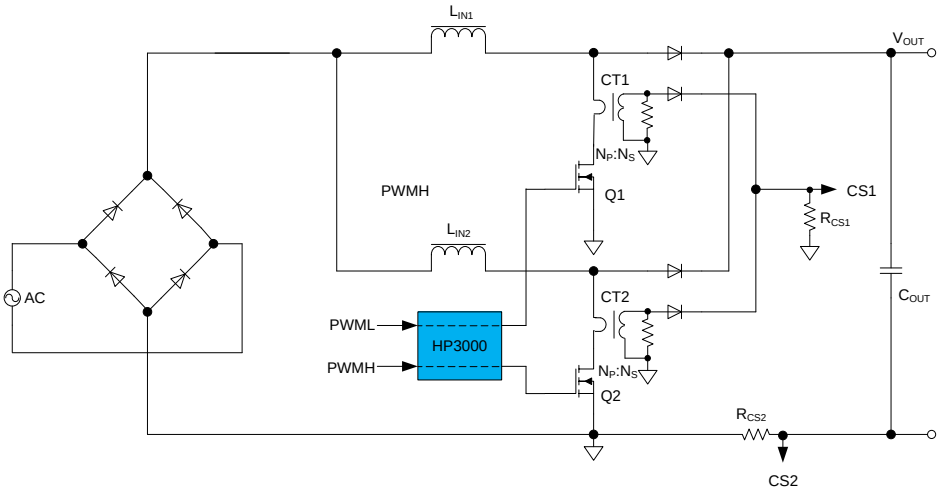


Figure 23 Current Transformer Current Sense in DIPFC Application

The equivalent resistance for the CT1 and CT2 is calculated based on the output power level.

Table 6. Recommended Equivalent Resistance Selection for Scheme 1

Output Power(W)	**400**	**800**	**1600**	**3200**	**6400**
Input current RMS value @ VAC = 85 VAC (A)	2.35	4.71	9.41	18.82	37.65
Input current Peak value @ VAC = 85 VAC (A)	3.33	6.65	13.31	26.62	53.23
CS1 equivalent resistance (NP/NS*RCS1) (mΩ)	400	200	100	50	25
CS1 peak voltage (V)	1.33	1.33	1.33	1.33	1.33
CS2 equivalent resistance (mΩ)	200	100	50	25	12.5
CS2 peak voltage (V)	0.67	0.67	0.67	0.67	0.67

In summary, this current sense method is a cost-effective solution that using two current transformers senses the up-slope of the inductor current. However, the input current and output current readings are not available. And the input power reading and output power readings are also not available.

CURRENT SENSE SCHEME 2: TWO SENSE RESISTORS FOR DIPFC TOPOLOGY

The current sense configuration used in this current scheme is illustrated in Figure 24.

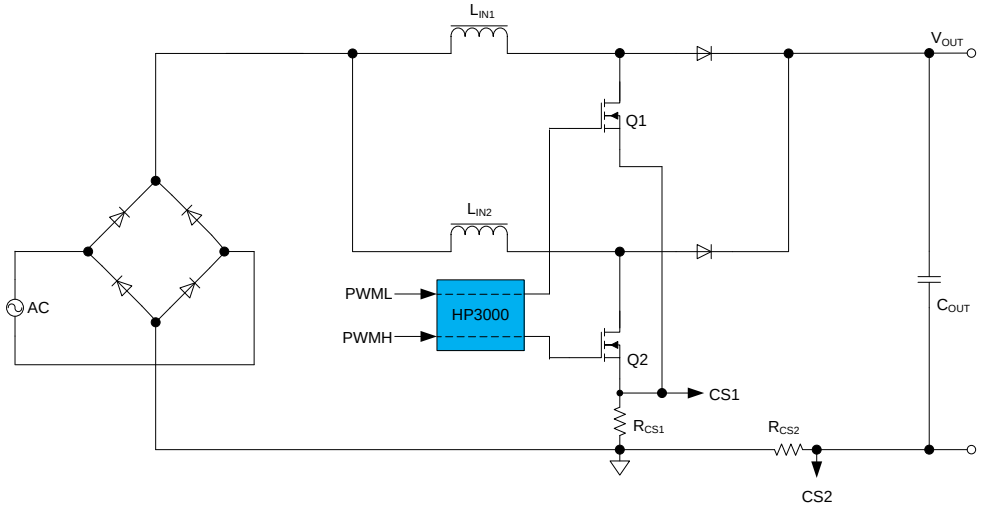


Figure 24 Sense Resistor Current Sense in DIPFC Application

The equivalent resistance for the R_{CS1} and R_{CS2} is calculated based on the output power level.

Table 7. Recommended Equivalent Resistance Selection for Scheme 2

Output Power(W)	400	800	1600	3200	6400
Input current RMS value @ VAC = 85 VAC (A)	2.35	4.71	9.41	18.82	37.65
Input current Peak value @ VAC = 85 VAC (A)	3.33	6.65	13.31	26.62	53.23
CS1 equivalent resistance (RCS1) (mΩ)	200	100	50	25	12.5
CS1 peak voltage (V)	0.67	0.67	0.67	0.67	0.67
CS2 equivalent resistance (RCS2) (mΩ)	200	100	50	25	12.5
CS2 peak voltage (V)	0.67	0.67	0.67	0.67	0.67

In summary, this current sense method is a cost-effective solution that using two sense resistor senses the up-slope of the inductor current. However, the input current and output current readings are not available. And the input power reading and output power readings are also not available, too.

CS1 AND CS2 COMPARATORS

For the DIPFC topology, the HP1011 has the programmable cycle-by-cycle current limit threshold V_{CS1_OC} for the CS1 pin and the same threshold and feature of V_{CS2_OC} for the CS2 pin.

The cycle-by-cycle current limit comparator also features programmable blanking and debounce times. See Table 8 for the debounce and blanking time option.

Table 8. Debounce and Blanking Time for CS1 and CS2 Cycle-by-cycle Limit

Parameter	Values or Options
Debounce Time	40 ns, 80 ns, 120 ns, 160 ns
Blanking Time	480 ns, 960 ns, 1440 ns, 1920 ns
Propagation Delay	100 ns maximum
Threshold Value	Programmable from 1.0 V to 1.5 V with 7.8 mV step for VCS1_OC and VCS2_OC (positive)
Actions for Protection	Terminate ‘d’ drive signal for 16 consecutively switching cycles, and then trigger IIN_PK_OC fault.

POWER FACTOR CORRECTION CONTROL LOOP

The HP1011 implement the average current mode power factor correction control loop. The implementation of the loop is digital, and all the signals are converted from analog to digital before they are processed by the control loop. Σ-Δ ADCs are used to achieve high performance, cost-effective implementation. The diagram of the current loop and voltage loop is shown in Figure 25.

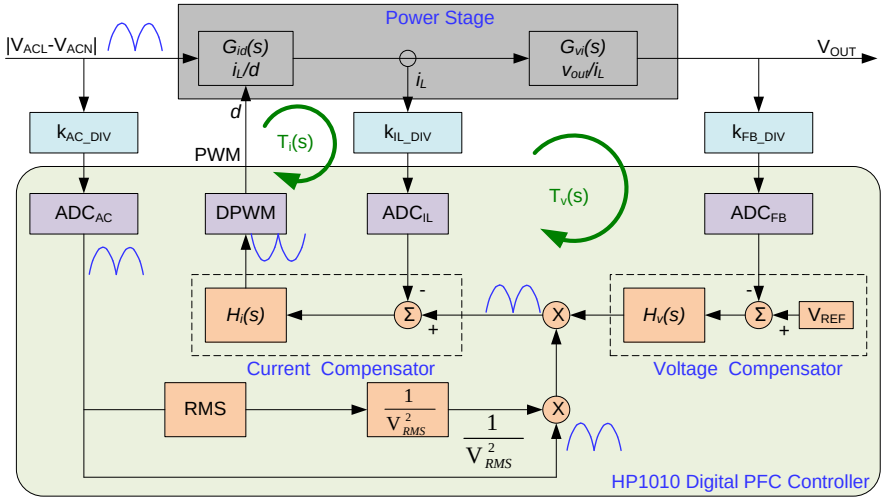


Figure 25 Current and Voltage Control Loops Diagram

FAST LOOP MODE

During transients, a fast loop mode is enabled in order to provide quicker loop responses. Typical timing can be seen in Figure 26. Fast loop mode has separate settings that can be programmed to respond quickly to load transients. The fast loop mode can be disabled by the user if it is not necessary by the application.

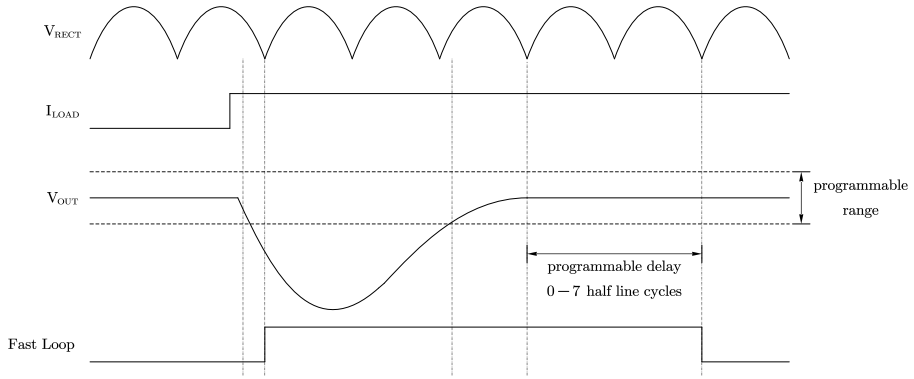


Figure 26 Fast Loop for Transient Response Improvement

DIGITAL PULSE MODULATION

The switching frequency is programmed in the SWTICHING_FREQ command. The switching frequency options are list in Table 9.

Table 9. Switching Frequency Options

Frequency setting #	Frequency setting (kHz)	Real Frequency (kHz)	Division of 25MHz
0	20	20.00	1250
1	30	30.05	832
2	45	44.96	556
3	65	65.10	384
4	90	89.93	278
5	120	120.19	208
6	160	160.26	156
7	195	195.31	128

PULSE-WIDTH MODULATION

Using the HP1011, only trailing edge modulation may be used. When utilized with downstream converter synchronization, trailing edge modulation can lower the rms ripple current in the bulk capacitors.

DUTY CYCLE MINIMUM/MAXIMUM LIMITS

The HP1011 allows the user to program the minimum off time and the minimum on time for the PWM outputs separately, thereby allowing the minimum and maximum duty cycles to be set. The minimum on-time is the smallest PWM pulse that the modulator generates on the PWM output. The minimum on-time of the main PWM and Sync PWM can be programmed from 40 ns to 320 ns in steps of 40 ns. The dead time T_{d1} between main PWM off and Sync PWM on is programmed from 40 ns to 320 ns, and the dead time T_{d2} between Sync PWM off and main PWM on is programmed from 40 ns to 320 ns. The maximum on-time of PWM is ($T_{sw}-T_{d1}-T_{d2}$).

FREQUENCY DITHERING (SPREAD SPECTRUM)

The PWM signal can be altered digitally to optimize for EMI reduction. For a wider but lower EMI spectrum, the switching frequency varies with the rectified line voltage. The switching cycle changes linearly with time from 87.5% to 112.5% of the nominal value, resulting in a frequency variation of 114% to 89% of the nominal value.

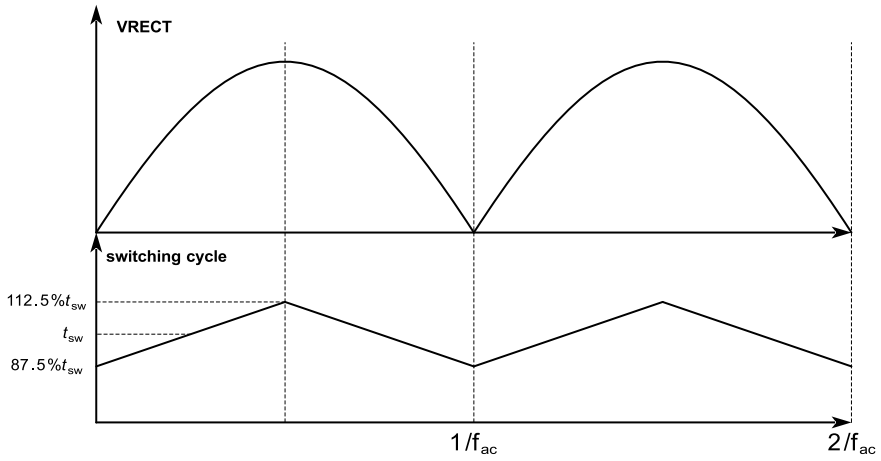


Figure 27 Frequency Dithering

OPERATION MODES

OPERATION MODE SUMMARY

The system can run in different modes. The mode transition is triggered by the events. These events may be from the ADC output, like OTP, OVP, etc. It can also be from the measurement (monitoring block), like light load detection or HVDC.

The HP1011 supports normal AC input (the frequency is between 40 and 70 Hz). With the AC input, they have the same operation. However, in HVDC mode, the system works as a boost converter; the main PWM switch is selected based on the input DC polarity.

START-UP SEQUENCE

When the user turns on the power factor correction, the following start-up procedure occurs, as shown in Figure 28.

1. Polarity detection. When the AC input voltage or the DC input voltage reach a threshold, the polarity detection starts and the POL_DET flag is triggered. The POSPOL and NEGPOL pins start to output signals indicating the input voltage polarity. Then the HP1011 enters the AC line frequency detection state.
2. AC line frequency detection It takes four consecutively half-AC cycles for line frequency detection. When the AC line frequency is within the range (50/60 Hz AC or HVDC), the HP1011 enters the brown-out detection state.
3. Brown-out detection. The HP1011 takes one AC cycle to complete the brown-out detection. If the AC line voltage is higher than the VIN_ON threshold, the brown-out flag is cleared. The HP1011 enters a turn-on delay state.
4. Turn-on delay. During this period, the relay is turned on, CS Short Detection is processed. The polarity detection comparator is then changed for surge detection.
5. Soft-start. The soft start PWM always begins at 0° of the AC cycle. During this period, the PWML and PWMH operate in duty-controlled mode (‘d’ drive) only. After the HP1011 finishes the soft start and enters the normal operation state, the PFCOK flag is triggered and the PFCOK pin is pulled high.
6. Normal operation. During normal operation, the PWML and PWMH operate in duty-controlled mode. The PFC may switch between CCM mode, DCM mode, and burst mode.

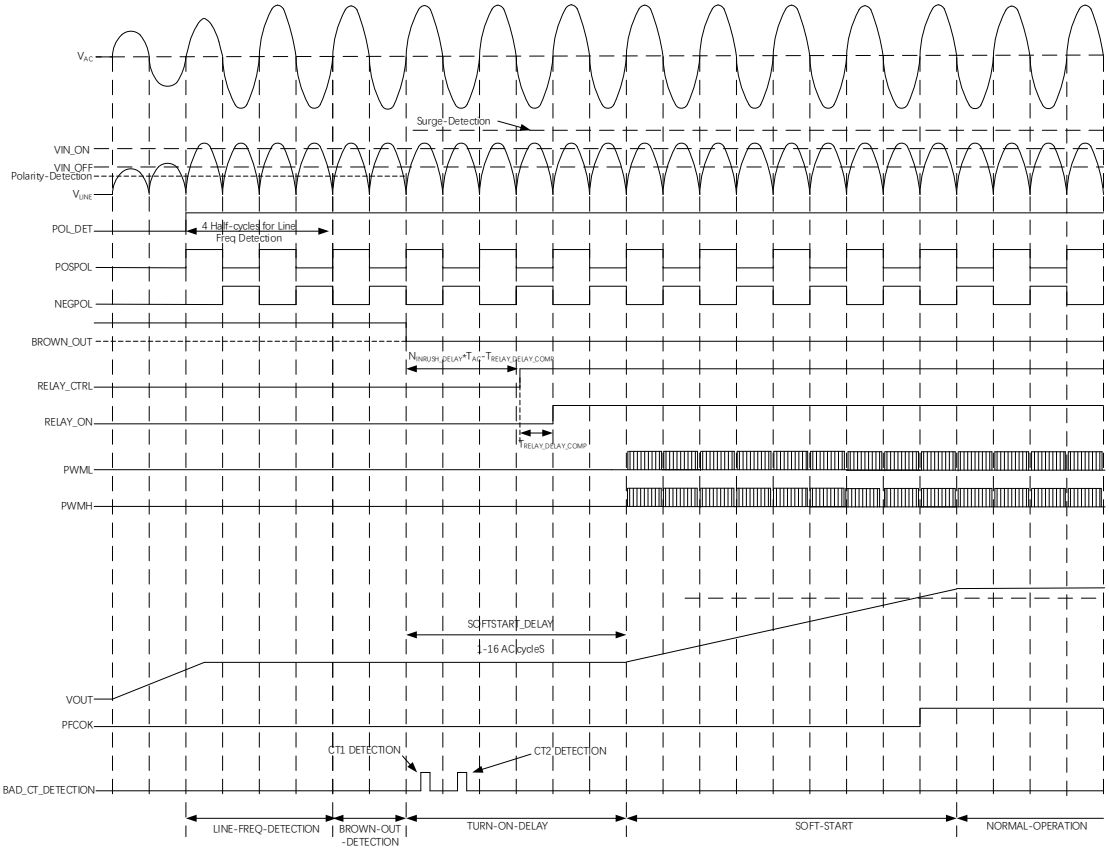


Figure 28 Start-up Sequence

PHASE SHEDDING

To achieve high efficiency at light load, the HP1011 can shut down one PWM channel under light load conditions, it is called phase shedding. The phase shedding function can be enabled or disabled and can be programmed to specify the PWM channel for phase shedding:

- no support
- PWMH works for phase shedding
- PWML works for phase shedding

When the input power drops below the input power, the specified phase shedding channel is disabled immediately. When the input power goes above the low power threshold plus power hysteresis, the PWM resumes operation during next AC zero-crossing.

The host device can manually force HP1011 to exist shedding. During this case, the PWM channel under phase shedding will exist to normal operation during next AC zero-crossing.

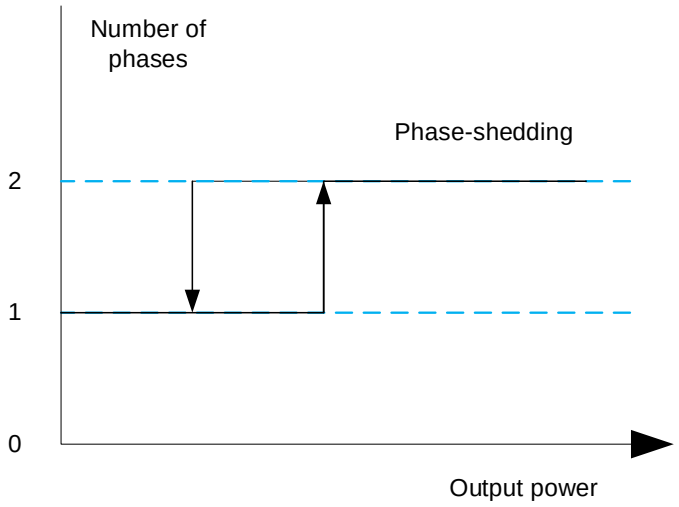


Figure 29 Phase Shedding Operation

CURRENT BALANCE

HP1011 support inherent inductor current balancing. When current balancing function enabled, the error of averaged switching period current between two phases will be compensated dynamically.

GPIO PINS & FUNCTIONS

The pins of RELAY/GPIO0, POSPOL/GPIO1, NEGPOL/GPIO2, GPIO3, GPIO4, RXD/GPIO5, TXD/GPIO6, and PFCOK/GPIO7 support the general-purpose digital IO function.

RELAY CONTROL

By controlling the power factor of the power drawn from the input, the PFC circuit generates a controlled, high voltage DC output while ensuring that the current is always proportional to the input voltage. High peak currents are drawn at the time of applying power to the input, though, as a result of the presence of a sizable "bulk" capacitor across the output. As "inrush" current, which is a PFC converter typically needs an inrush protection circuit to avoid circuitry damage.

Current protection techniques typically only work at initial power startup. Resistive current limiting is a widely used technique. It employs a resistor with the proper rating linked in series with the PFC circuit's primary power connection. This resistor is eliminated (i.e., shorted via a relay contact) following the charging of the output capacitor. Usually, once the initial inrush fades and the PFC converter turns to normal operation mode, the relay driving circuit needs a low power supply (typical 12V) to shut the relay contact. At this point, the PFC initiates its own current-limiting features, such as a "soft-start" or "peak-current detection".

Relays from various vendors exhibit varying delay times. To ensure proper operation, the relay should be closed at the beginning of the positive half cycle. Accounting for the relay delay time (t_{delay_relay}), the RELAY signal controlling the relay should be activated t_{delay_relay} time before the zero-crossing point of the positive half cycle (0° of the AC cycle).

Therefore, the actual delay time from the brown-out flag cleared to the DELAR pulling high is $N_{INRUSH\_DELAY}*T_{AC}-T_{REDELAY\_DELAY\_COMP}$. In the case of Figure 30, N = 2.

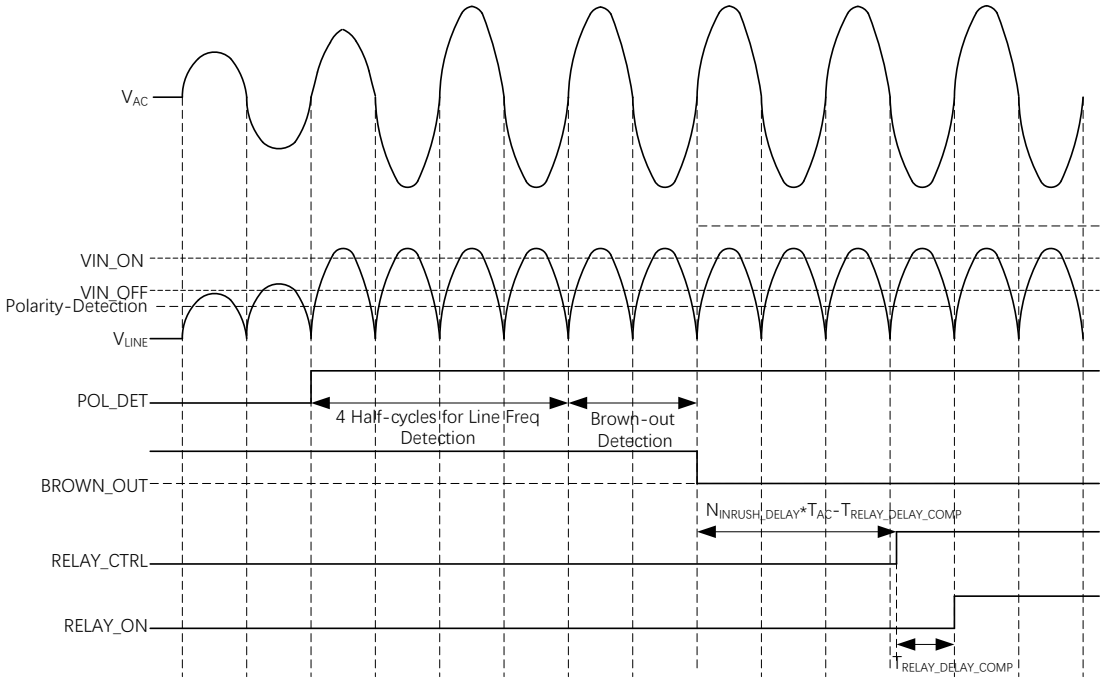


Figure 30 Relay Control Timing

During the normal operation of the PFC, the relay is closed to shorten the inrush resistor. It reduces the power loss on this resistor. But with a very light load or a zero load, the input current is almost zero. The power loss over the resistor can be ignored compared to the power consumption of the relay circuit. In this situation, disabling the relay can save more power. Thus, the RELAY signal for the relay control can be set to be low at this moment. The recovery hysteresis is 5 Watts.

X-CAPACITOR DISCHARGE

Consumer equipment must comply with safety regulations like IEC 61010-1, IEC 62368-1, and others. When the mains connector is disconnected, the EMI filter capacitors (X-capacitors) connected across the line between the phase and neutral must be discharged to a safe level. This prevents any risk of electrical shock to the user due to stored energy in the capacitors. This discharge is mandatory when the total capacitance before the input bridge exceeds 100 nF.

Typically, this function is performed by means of a resistor in parallel, but this method cannot be applied in cases where the converter requires very low power consumption during the light-load or no-load operation because the losses of the X-cap discharging resistor would be too high.

To overcome this issue, HP1011 offers a control signal to discharge the voltage across the X-cap without the traditional X-cap discharge resistor. The HP1011 internal circuits detect the AC mains plug disconnection by sensing the voltage on the ACL and ACN pins. After a detection time (typically 30 ms) from the mains disconnection, the X-cap discharge operation is triggered, and the external high voltage switches are turned on. A discharge current (a few mA) is drawn from the phase and the neutral wires, ensuring the X-capacitor discharge with a constant discharging time of 250 ms. Typically, GPIO0-GPIO7 pins can be configured to turn on the discharge circuit, as shown in Figure 31.

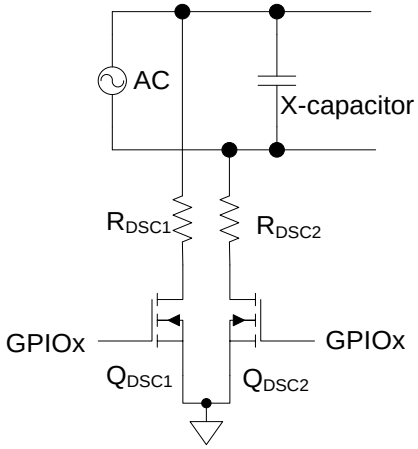


Figure 31 X-cap Discharge Circuit

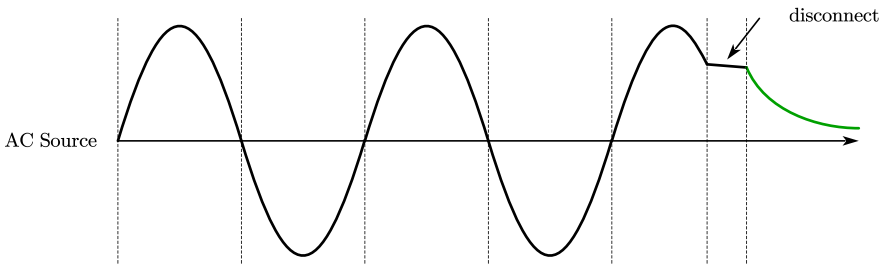


Figure 32 AC Disconnection (unplug) and X-cap Discharge Operation

As shown in Figure 32, normally the AC main voltage is applied to the X-cap. When the AC power is suddenly unplugged, the voltage crosses the X-cap keep the voltage at that moment. In HP1011, the ADC continuously measures the voltage between ACL and ACN, which is equal to the voltage across the X-cap. If it finds the voltage becomes a DC voltage from an AC voltage, one GPIO signal will be triggered to be active. This GPIO signal will be connected to the X-cap discharge circuit as shown in Figure 31, which includes the two resistors (R_{DSC1} and R_{DSC2}) and two power FETs (R_{DSC1} and R_{DSC2}) generally. In normal operation, these two power FETs are off. The equivalent resistance of the branch is extremely high; there is no current, essentially. When HP1011 detects the AC disconnection, the GPIO signal turns on the power switches, and the resistors R_{DSC1} and R_{DSC2} discharge the X-capacitor voltage.

When the input voltage is DC input, the X-capacitor discharge is not functional.

FAULT, PROTECTIONS AND MONITORINS

The HP1011 features advanced fault and system monitoring capabilities. Voltage, current, and power readings are all included in the system monitoring features. Out of limits for current, voltage, power, and temperature are among the fault conditions. The fault condition limitations are programmable. All these variables, flags, and thresholds are read through an I^2C interface. All the threshold settings can be stored in the on-chip EEPROM.

FAULT FLAGS AND PROTECTIONS

An extensive set of flags is set when certain thresholds or limits are exceeded. These flags are described in Table 10.

The NTC/ROV is a dual-function pin. Once the NTC function is selected by default, the over-temperature condition is able trigger the NTC_OT flag. While the redundant OVP function is disabled. On the contrary, if the redundant OVP is selected, the open loop condition can trigger the ROVP flag. Detail information is provided in Section OTP & Redundant OVP (NTC/ROV Pin) .

Table 10. Summary of Flags

Flag	Descriptions	Debounce	Protection Action
VIN_MODE	0: fault, 1: 40 Hz ~ 70 Hz, 3 = DC		None
BROWN_OUT	VIN exceed VIN_ON to clear flag	0.5 cycle	See Table 11
IIN_PK_OC	CS1 cycle-by-cycle current limit timeout	2, 4, 8, 16, 32,48,64	See Table 11
IIN_AV_OC	Input average over-current fault	2 switching cycle	See Table 11
SURGE	Surge detection		See Table 11
VIN_OV	Input over-voltage fault		See Table 11
INRUSH	RELAY signal is high	None	None
HIGH_LINE	0: low line; 1: high line	1 AC cycle	None
VOUT_SLW_UV	Output under-voltage fault	0~30 ms	See Table 11
VOUT_SLW_OV	Output slow over-voltage fault	0~30 ms	See Table 11
VOUT_FST_OV	Output Fast over-voltage fault	40~100 μs	See Table 11
FAST_LOOP	Fast loop operation	None	None
NTC_OT	NTC over-temperature fault	500, 1000 ms	See Table 11
PFCOK	Combination of eight fault flags	None	PFCOK pin is high
ALERT#	Combination of eight fault flags	None	ALERT# pin is low
CS_SHORT	CS Short fault	None	Wait for 1s and retry
FREQ_NOK	Line frequency not OK	4 cycles	See Table 11
VOUT_OL	Output open-loop fault	0~30 ms	See Table 11
3V3_UVLO	VDD Supply UVLO		HW reset and restart
ROV	Redundant OVP	40~100 μs	See Table 11
AUTO_PFC_OFF	Turn off PFC at low load		Turn-off PFC

Table 11 provide summary of fault protection actions.

Table 11. Summary of Fault Protection Actions

Flag	Type	Protection action
BROWN_OUT FAULT	3	Enter sag operation then go back to PFC off state
IIN_PK_OC	1	Ignore, latch, or fault recover
IIN_AV_OC	1	Ignore, latch, or fault recover
SURGE	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover
VIN_OV	1	Ignore, latch, or fault recover
VOUT_SLW_UV	1	Ignore, latch, or fault recover

VOUT_SLW_OV	1	Ignore, latch, or fault recover
VOUT_FST_OV	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover
VOUT_OL	1	Ignore, latch, or fault recover
NTC_OT	1	Ignore, latch, or fault recover
FREQ_NOK	3	Enter LINE_FREQ_EXCEED mode for 4 ac cycles, if fault still exist, goes to PFC off state
ROV	2	Ignore (disable all PWM and recover without soft start once fault cleared), latch, or fault recover

PFCOK AND ALEART# PINS

The HP1011 has two digital status pins: PFCOK and ALERT#. The PFCOK is intended to control the operation of a downstream DC−DC converter by acting as an enable or UVLO signal. The PFCOK output is high when the application is in nominal operation and low when the device detects a fault condition. The ALERT# is pulled low to notice the I²C master when the device detects a fault condition. When the I²C mater reads the fault flags to clear the corresponding fault flags, the ALERT# flag recovers.

Both signals represent an OR function for a programmable list of internal flags, as shown in Figure 33. Users can mask some of these flags to tailor the PFCOK and ALERT# signals to their needs. When the signals on the PFCOK and ALERT# pins are set, the corresponding internal flag is also set.

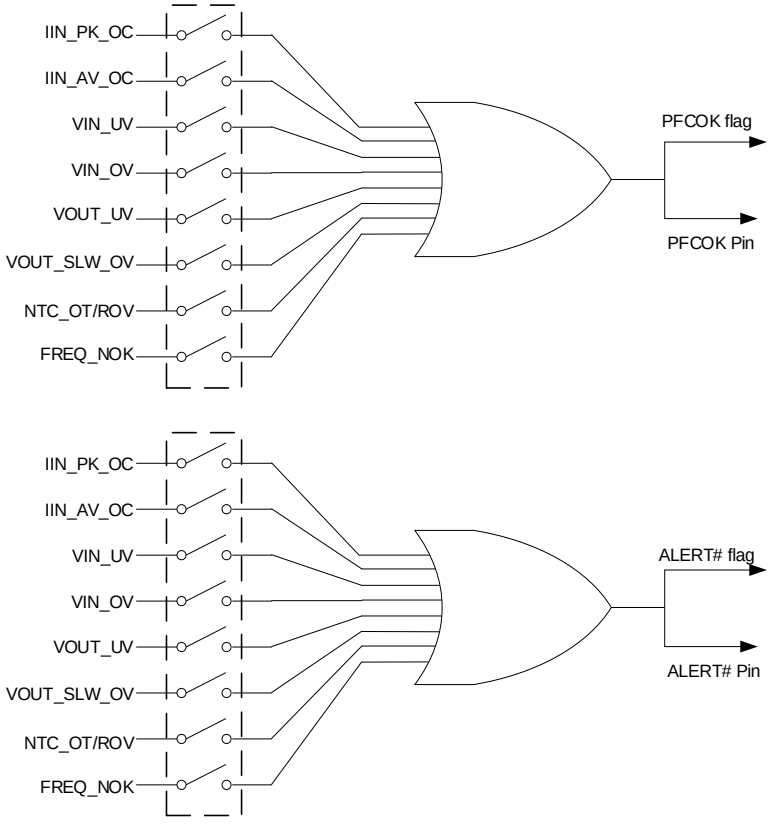


Figure 33 PFCOK and ALEART# Signals

OTP & REDUNDANT OVP (NTC/ROV PIN)

The NTC/ROV pin is a dual-functions pin for over-temperature protection (OTP) and redundant over-voltage protection (Redundant OVP). When the NTC/ROV pin is used as OTP, a source current I_{NTC_SRC} (typically 46 μA) is applied to the NTC/ROV pin. The HP1011 detects an NTC over-temperature fault if the NTC/ROV pin voltage is pulled below the lower fault threshold, V_{NTC_OT}, typically 0.4 V. The hysteresis is 0.4 V. The protection actions include a reset from brown-out cleared and latch mode. Once operating in latch mode, the line frequency detection and VAC detection continue. A PFC_ON signal by the CTRL pin and/or ENABLE bit will reset from the brown-out cleared state.

Alternatively, the NTC/ROV pin can be configured as a redundant OVP function. The redundant OVP comparator is analog and directly monitors the feedback pin voltage for immediate blanking of the drive pulses. The reference of the redundant OVP comparator is programmable from 1.9 V to 2.5 V with a 9.4 mV step. This represents that the actual redundant OVP limit is programmable from 380 V to 500 V with a 1.87 V step. Once the output voltage exceeds the redundant OVP limit, the ROV fault is triggered. During redundant OVP, the source current I_{NTC_SRC} is disabled. The protection actions include all ignore, latch mode, and going to fault recovery mode. Once operating in latch mode, line frequency detection and VAC detection continue. A PFC_ON reset will reset HP1011 to PFC off state.

POWER METERING

True RMS values are calculated at the end of each half AC line cycle by integrating the instantaneous values across each line cycle. The averaging window is programmable from 64, 128, 256, and 512 AC cycles. For the DC input, the averaging window is programmed for 1.28 seconds, 2.56 seconds, 5.12 seconds, and 10.24 seconds. At the end of each averaging period, the new average values are written to the registers and are available to be read back through the interface until they are overwritten by the next averaged value at the end of the next averaging period.

Figure 34 shows the block diagram of power monitoring. The IIN_SENSE_METHOD bits in Register 0x16 should be correctly selected.

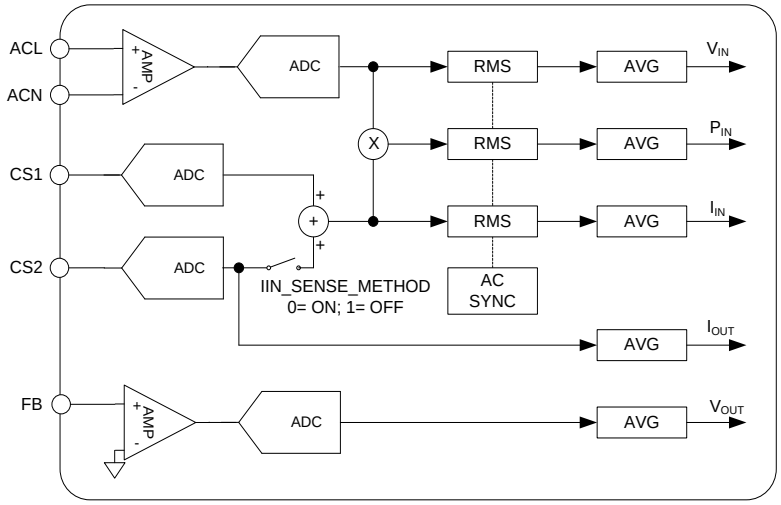


Figure 34 Power Monitoring Diagram

COMMICATION INTERFACES AND EEPROM

The HP1011 provides one I²C communication interface and one UART communication interface.

I²C INTERFACE

The I²C Bus (Interface wires) consists of just two wires and are named as Serial Clock Line (SCL) and Serial Data Line (SDA). The data to be transferred is sent through the SDA wire and is synchronized with the clock signal from SCL. All the devices/ICs on the I²C network are connected to the same SCL and SDA lines as shown below.

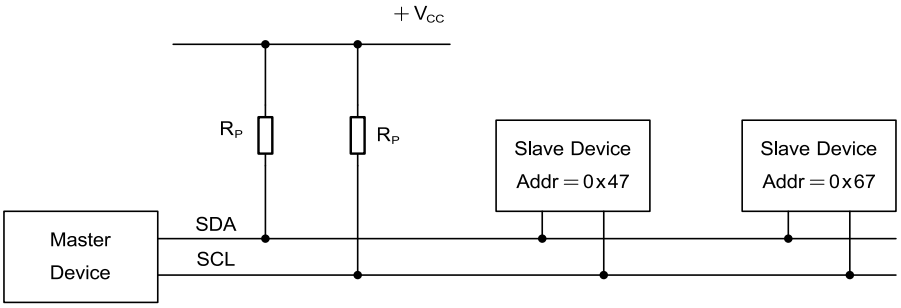


Figure 35 I²C Communication

The ALERT#/ADD is dual function pin. During the power-on reset, the state of this pin is sampled. Note: A 900 kΩ resistor should be used when connecting to the VDD pin or GND pin to reduce standby current, as shown in Figure 36.

- HIGH = I²C address is 0x67.
- LOW = I²C address is 0x47.

Figure 36 I²C Addressing

UART INTERFACE

Beside the I²C interface, the HP1011 also communicates with an external digital device with a standard UART protocol using two dedicated pins.

The UART serial interface allows the user to:

- Write/read configuration registers:
  - ENABLE register bit to remote enable or disable PFC function.
  - VREF_LLINE register to set low line voltage regulation reference.
  - VREF_HLINE register to set high line voltage regulation reference.
- Read all STATUS and Telemetry register contents.

The HP1011 is designed to support low-cost, conventional opto-couplers for slow-speed communication.

When sleep mode is turned off, the HP1011 never goes into sleep mode. The UART feature is active as default. The TXD/RXD configuration determines whether the HP1011 can connect to the host device using the UART bus.

The UART function is not available if sleep mode is enabled. After PFC has been off for five seconds, HP1011 automatically goes into sleep mode. The sleep state can be promptly woken up by a write or read to I²C. The HP1011 can be promptly woken up from sleep mode by switching from PFC off state.

BAUD RATE

The speed at which the data is transmitted is mentioned using the Baud Rate. Both the transmitting UART and receiving UART must agree on the Baud Rate for a successful data transmission. Baud Rate is measured in bits per second. Some of the standard baud rates are 1200 bps, 9600 bps, 57600 bps, 115200 bps etc. Out of these 9600-bps baud rate is the most used.

The baud rate is configurable through registers with I²C interface:

Table 12. Baud Rate Options

Baud Rate (bps)	9600	1200	57600	115200
Options	0	1	2	3
Division from 25 MHz	2604	5208	434	217
Real Baud Rate (bps)	9600.6	4800.3	5760.4	11521

RULES OF UART

There is no clock signal in UART, and the transmitter and receiver must agree on some rules of serial communication for error free transfer of data. The rules include:

- Synchronization Bits (Start and Stop bits)
- Parity Bit
- Data Bits
- Baud Rate

In the HP1011 the most popular UART rule is selected.

- Synchronization Bits (1 bit Start and 1 bit Stop)
- Parity Bit (yes, 1 bit)
- Data Bits (8 bits)
- Baud Rate (programmable)

EEPROM

The HP1011 has a built-in EEPROM controller that is used to communicate with the embedded 128 × 8-byte EEPROM. When the digital core and EEPROM are power-on, all the data from the EEPROM will be loaded to corresponding registers to configure the IC's parameters. Users can also read or write these registers to program the IC's parameters according to different applications. When these parameters are fully tested and working as expected, users can program to EEPROM through the I²C interface.

APPLICATION INFORMATION

DUAL-PHASE INTERLEAVED PFC

Dual-phase interleaved PFC typical application circuit is shown in Figure 37.

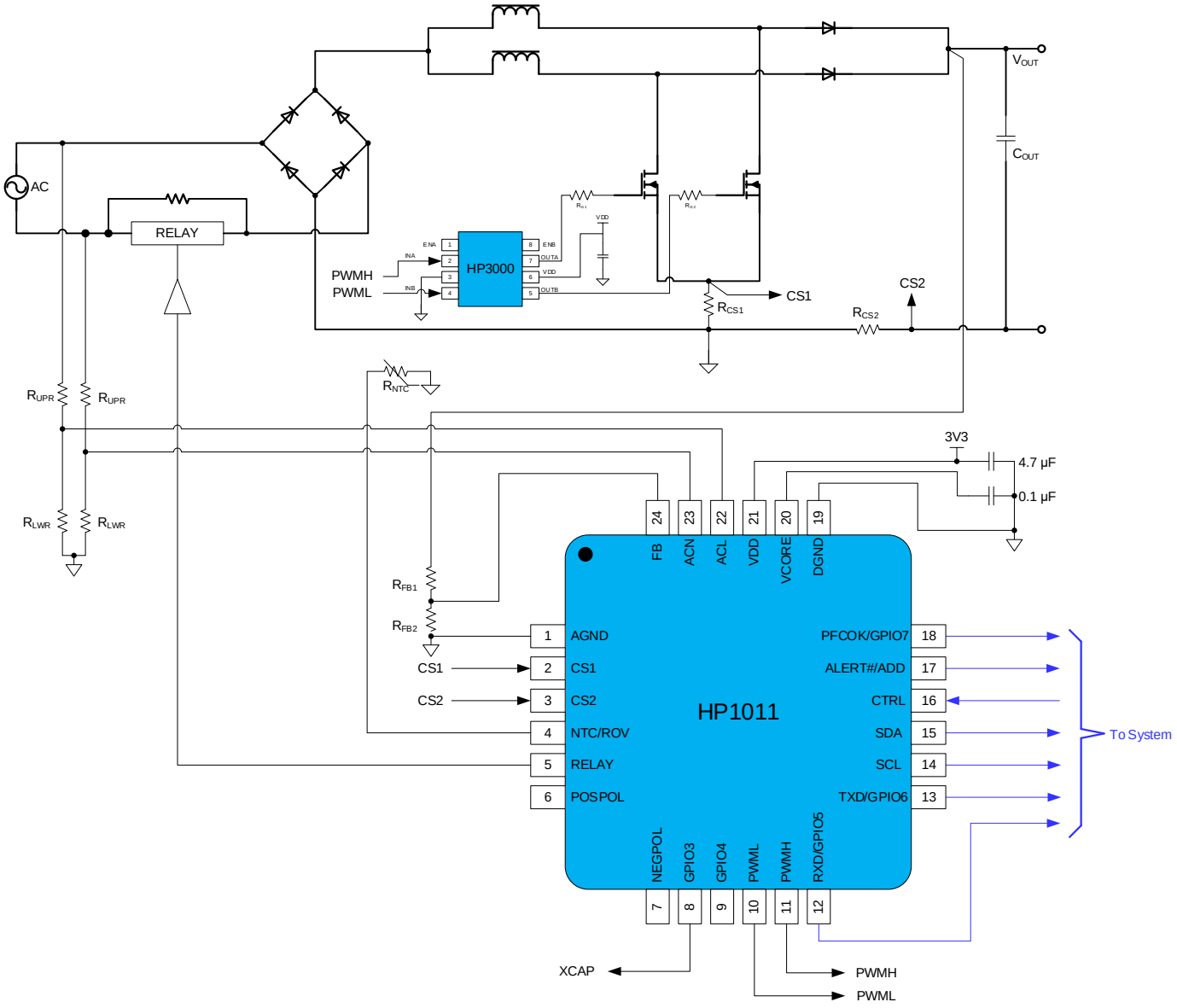
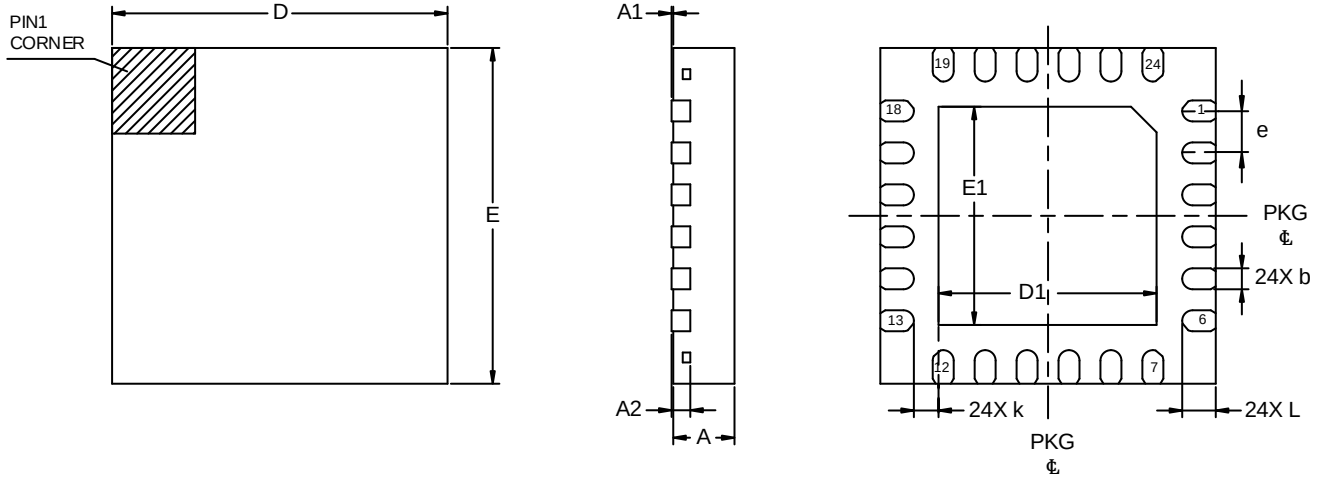


Figure 37 Dual-phase Interleaved PFC Typical Application Circuit

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.000	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D1	2.40	2.70	2.80
E1	2.40	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN	

Figure 38 HP1011-QN24 Package

PACKAGE TOP MARKING

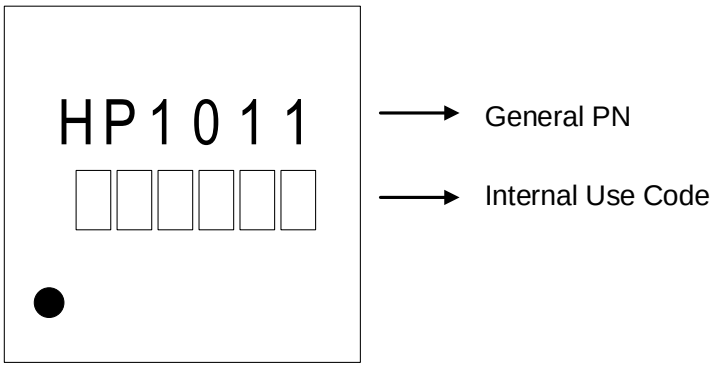


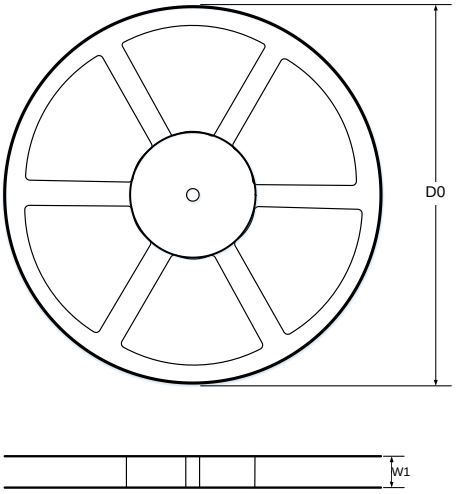
Figure 39 HP1011-BA000-QN24R Package Top Marking

ORDERING GUIDE

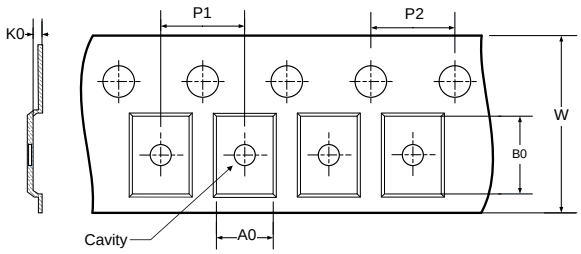
Model	Temperature Range	Package Type	MSL	Package Option	Quantity
HP1011-BA000-QN24R	-40°C to +125°C	QFN4x4-24L	3	T&R	5000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

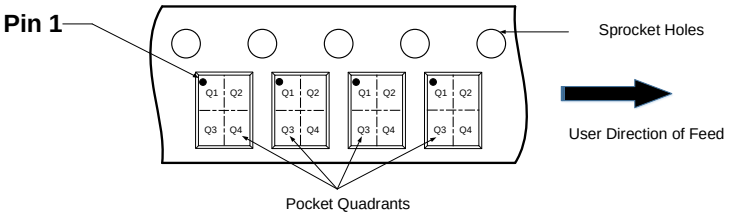


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HP1011-BAXXX-QN24R	QFN4X4-24L	330.00	12.40	4.30	4.30	1.10	8.00	4.00	12.00	Q1	5000

All dimensions are nominal

Figure 40 Tape and Reel Information

IMPORTANT NOTICE

Hynetek Semiconductor Co., Ltd. and its subsidiaries (Hynetek) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to Hynetek’s terms and conditions of sale supplied at the time of order acknowledgment.

Hynetek warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in Hynetek’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent Hynetek deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

Hynetek assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using Hynetek components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Hynetek does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Hynetek components or services are used. Information published by Hynetek regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Hynetek under the patents or other intellectual property of Hynetek.

Reproduction of significant portions of Hynetek information in Hynetek data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Hynetek is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of Hynetek components or services with statements different from or beyond the parameters stated by Hynetek for that component or service voids all express and any implied warranties for the associated Hynetek component or service and is an unfair and deceptive business practice.

Hynetek is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Hynetek components in its applications, notwithstanding any applications-related information or support that may be provided by Hynetek. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify Hynetek and its representatives against any damages arising out of the use of any Hynetek components in safety-critical applications.

In some cases, Hynetek components may be promoted specifically to facilitate safety-related applications. With such components, Hynetek’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No Hynetek components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those Hynetek components which Hynetek has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of Hynetek components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Hynetek has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, Hynetek will not be responsible for any failure to meet ISO/TS16949.

Please refer to below URL for other products and solutions of Hynetek Semiconductor Co., Ltd.