General Description

The LTP7792 is a CMOS low dropout regulator that operates from 2.3 V to 6.5 V and provides up to 2 A of output current. This high output current LDO is ideal for regulation of high performance analog and mixed-signal circuits operating from 6 V down to 1.2 V rails. Using an advanced proprietary architecture, the device provides high power supply rejection and low noise, and achieves excellent line and load transient response with just a small 4.7 uF ceramic output capacitor. Load transient response is typically 1.5 us for a 1 mA to 1.5 A load step.

The LTP7792 is available in 17 fixed output voltage options. The following voltages are available from stock: 1.3 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V, 4.2 V, and 5.0 V. Additional voltages that are available by special order are: 1.5 V, 1.85 V, 2.0 V, 2.2 V, 2.7 V, 2.75 V, 2.8 V, 2.85 V, 3.8 V, and 4.6 V. An adjustable version is also available that allows output voltages that range from 1.2 V to $V_{IN} - V_{DO}$ with an external feedback divider.

Features

- Operating Input Voltage Range: 2.3 V to 6.5 V
- Maximum Output Current: 2 A
- Low noise: 5 µV rms independent of output voltage at 100 Hz to 100 kHz
- Fast transient response: 1.5 µs for 1 mA to 1.5 A load step
- High Power Supply Ripple Rejection: 60 dB PSRR at 100 kHz
- Low dropout voltage: 135 mV at 2 A load, V_{OUT} = 3 V
- Initial accuracy: −0.8% (minimum), +0.7% (maximum)
- Accuracy over line, load, and temperature: ±1.5%
- Quiescent current, I_{GND} = 0.7 mA with no load
- Low shutdown current: 0.25 µA at V_{IN} = 5 V
- Stable with small 4.7 µF ceramic output capacitor
- Adjustable and fixed output voltage options: 1.2 V to 5.0 V
- Adjustable output from 1.2 V to $V_{IN} - V_{DO}$
- Precision enable
- Adjustable soft start
- Package: DFN3×3-8

Applications

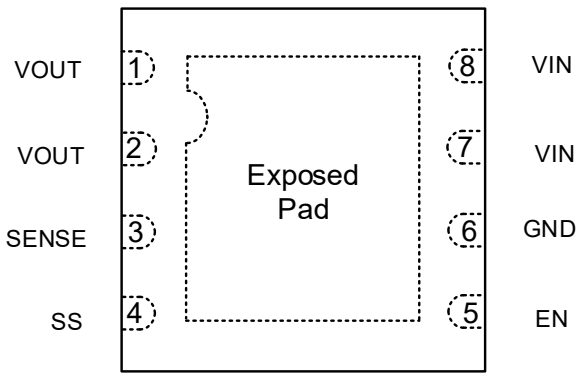
- Regulation to noise sensitive applications: ADC and DAC circuits, precision amplifiers, PLLs/VCOs, and clocking ICs
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation

Ordering Information

Model	Package	Output Current	Ordering Number[Note1]	Packing Option
LTP779X	LTP7790	500 mA	LTP7790-xxXF8/R10	Tape and Reel, 5000
	LTP7791	1 A	LTP7791-xxXF8/R10	Tape and Reel, 5000
	LTP7792	2 A	LTP7792-xxXF8/R10	Tape and Reel, 5000

Note1: xx stands for output voltages, e.g. if xx = 18, the output voltage is 1.8 V; if xx = A, the output voltage is adjustable version.

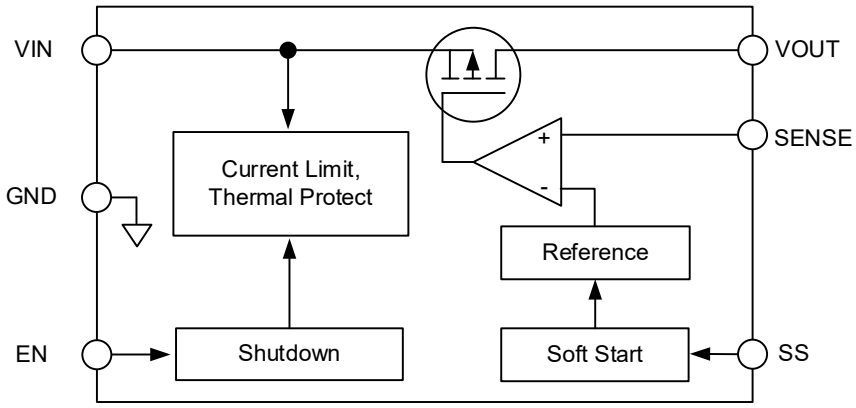
Pin Configurations (Top View)



Pin Function

Pin No.	Symbol	Function
1	VOUT	Regulated Output Voltage. Bypass this pin to GND with a 4.7 µF or greater capacitor.
2	VOUT	Regulated Output Voltage. This pin is internally connected to Pin 1.
3	SENSE	Sense Input. Connect this pin as close as possible to the load for best load regulation. Use an external resistor divider to set the output voltage higher than the fixed output voltage.
4	SS	Soft Start. A 1 nF external capacitor connected to SS results in a 1.0 ms start-up time.
5	EN	Regulator Enable. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN (Pin 7 or Pin 8).
6	GND	Ground.
7	VIN	Regulator Input Supply. Bypass this pin to GND with a 4.7 µF or greater capacitor.
8	VIN	Regulator Input Supply. This pin is internally connected to Pin 7.
	EP	Exposed Pad. The exposed pad is on the bottom of the package. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. Connect the exposed pad to the ground plane on the board to ensure proper operation.

Block Diagram



Applications Information

General

The LTP7792 is a low quiescent current, low dropout linear regulator that operates from 2.3 V to 6.5 v and provides up to 2 A of load current. Drawing a low 3.5 mA of quiescent current(typical) at full load makes the LTP7792 ideal for portable equipment.

Input Bypass Capacitor

Connecting a 4.7 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or a high source impedance is encountered. If greater than 4.7 µF of output capacitance is required, increase the input capacitor to match it.

Output Capacitor

The LTP7792 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 4.7 µF capacitance with an ESR of 0.05 Ω or less is recommended to ensure the stability of the LTP7792. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the LTP7792 to large changes in load current.

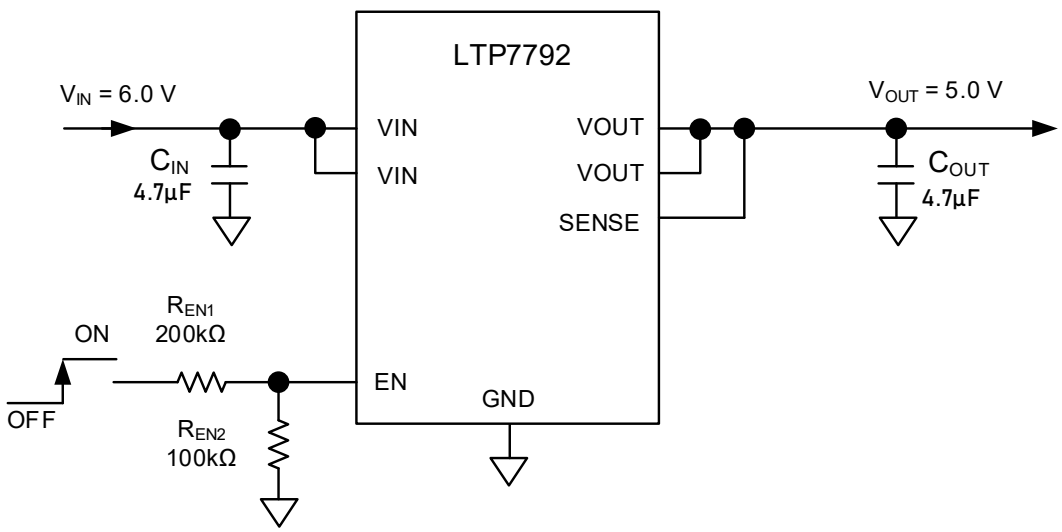
Programmable Precision Enable

The LTP7792 has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0.1 µA typical. The EN pin may be directly tied to VIN to keep the part on. The Enable input is CMOS logic and cannot be left floating.

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.2 V threshold by using two resistors. The resistance values, R_{EN1} and R_{EN2}, can be determined from

$R_{EN1} = R_{EN2} * (V_{IN} - 1.2\ V)/1.2\ V$

where:
R_{EN2} is nominally 10 kΩ to 100 kΩ.
V_{IN} is the desired turn-on voltage.
The hysteresis voltage increases by the factor $(R_{EN1} + R_{EN2})/R_{EN1}$



Applications Information

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 3.3 A to prevent over-current and to protect the regulator from damage due to overheating.

Soft Start

The LTP7792 incorporates a Soft-Start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown point (T_{SD} =150°C typically) the device goes to disabled state and the output voltage is not delivered until the die temperature decreases to 135°C. The Thermal Shutdown feature provides a protection from a catastrophic device failure at accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the LTP7792 device can handle is given by:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed TJ(MAX) and thermal resistance, θ_{JA}.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	-0.3 to 7	V
Output Voltage	V_{OUT}	−0.3 to V_{IN}	V
Enable Voltage	V_{EN}	−0.3 to 7	V
Soft-start Voltage	V_{SS}	−0.3 to V_{IN}	V
Sense Voltage	VSENSE	−0.3 to 7	V
Operating Junction Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	36.4	°C /W
Human Body Model	ESD	±6000	V
ESD Capability		±2000	V

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}	2.3		6.5	V
Output Current	I_{OUT}		2		A
Effective Input Ceramic Capacitor Value	C_{IN}	3.3	4.7		μF
Effective Output Ceramic Capacitor Value	C_{OUT}		4.7		μF

Caution

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. LINEARIN recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

LINEARIN reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact LINEARIN sales office to get the latest datasheet.

Electrical Characteristics

(V_{IN}= $V_{OUT-NOM}$ + 0.5 V or 2.3 V, EN = V_{IN}, I_{OUT}=10 mA, T_a= 25 °C, C_{IN}= C_{OUT} = 4.7 µF, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Operation Range	V_{IN}		2.3		6.5	V
Fixed Output Voltage Accuracy	V_{OUT}	I_{LOAD} = 10 mA, T_J= 25°C	-0.8		0.7	%
		I_{LOAD} = 100 µA to 2A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	-1.5		1.5	
Adjustable Output Voltage Accuracy	V_{SENSE}	I_{LOAD} = 10 mA	1.194	1.2	1.212	V
		I_{LOAD} = 100 µA to 2A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	1.182		1.218	
Line Regulation	$\Delta V_{O(\Delta VI)}$	V_{IN} = $V_{OUT-NOM}$+0.5 V to 6.5 V	-0.1		0.1	%/V
Load Regulation	$\Delta V_{O(\Delta IO)}$	I_{OUT} = 100 µA to 2 A		0.1	0.3	%/A
Load Current	I_{LOAD}				2	A
Ground Current	I_{GND}	I_{OUT} = 0 µA		0.7	2	mA
		I_{OUT} = 2 A		3.5	5	
Shutdown Current	I_{SHDN}	V_{EN} = 0 V, I_{OUT} = 0 mA, V_{IN} = 5 V		5	10	µA
Output Current Limit	I_{OLIM}		2.4	3.2	3.9	A
Soft Start Current	I_{SS}	V_{IN} = 5 V	0.5	1	1.5	µA
Dropout Voltage	V_{DO}	I_{OUT} = 500 mA, V_{OUT} = 3 V		35	70	mV
		I_{OUT} = 1 A, V_{OUT} = 3 V		70	135	
		I_{OUT} = 2 A, V_{OUT} = 3 V		135	270	
Power Supply Rejection Ratio	PSRR	100 kHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A		60		dB
		100 kHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A,		53		
		100 kHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A		42		
		1 MHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A		31		
		1 MHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A,		30		
		1 MHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1.5A		20		
Output Voltage Noise	V_N	10 Hz to 100 kHz, all fixed output voltages		6		μV_{RMS}
		100 Hz to 100 kHz, all fixed output voltages		5		
		100 Hz, all fixed output voltages		110		nV/√Hz
		1 kHz, all fixed output voltages		40		
		10 kHz, all fixed output voltages		20		
		100 kHz, all fixed output voltages		12		
Start-up time	t_{START}	V_{OUT} = 5 V, C_{SS} = 0 nF		380		µS
		V_{OUT} = 5 V, C_{SS} = 1 nF		1		mS

Electrical Characteristics

(V_{IN}= $V_{OUT-NOM}$ + 0.5 V or 2.3 V, EN = V_{IN}, I_{OUT}=10 mA, T_a= 25 °C, C_{IN}= C_{OUT} = 4.7 µF, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Rising	$UVLO_{RISE}$	V_{IN} = 2.3 V to 6.5 V			2.28	V
Input Voltage Falling	$UVLO_{FALL}$		1.94			V
Internal UVLO Hysteresis	$UVLO_{HYS}$			200		mV
Transient Load Response	t_{TR_REC}	Time for output voltage to settle within ±V_{SETTLE} from V_{DEV} for a 1 mA to 1.5 A load step, load step rise time = 400 ns	1.5			µS
	V_{DEV}	Output voltage deviation due to 1 mA to 1.5 A load step	35			mV
	V_{SETTLE}	Output voltage deviation after transient load response time (t_{TR_REC} has passed, V_{OUT} = 5 V, C_{OUT} = 4.7 µF	0.1			%
EN Input Logic High	$V_{EN-HIGH}$	V_{IN} = 2.3 V to 6.5 V	1.27			V
EN Input Logic Low	V_{EN-LOW}				0.4	V
EN Input Logic Hysteresis	V_{EN-HY}			90		mV
EN Input Logic High	$V_{EN-HIGH}$	V_{IN} = 2.3 V to 6.5 V, EN = V_{IN} or GND, From EN rising from 0 V to V_{IN} to 0.1 V × V_{OUT}	1.11	1.2	1.27	V
EN Input Logic Low	V_{EN-LOW}		1.01	1.1	1.16	V
EN Input Logic Hysteresis	V_{EN-HY}			100		mV
EN Input Leakage Current	I_{EN-LK}			0.1		µA
EN Input Delay Time	T_{EN-DLY}			100		µs
VOUT Pull-down Resistance	$V_{OUT-PULL}$	EN = 0 V, V_{OUT} = 1 V		4		kΩ
Thermal Shutdown Temperature	T_{SD}	Temperature rising from T_J=+25°C		150		°C
Thermal Shutdown Hysteresis	T_{SDH}	Temperature falling from T_{SD}		15		°C

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

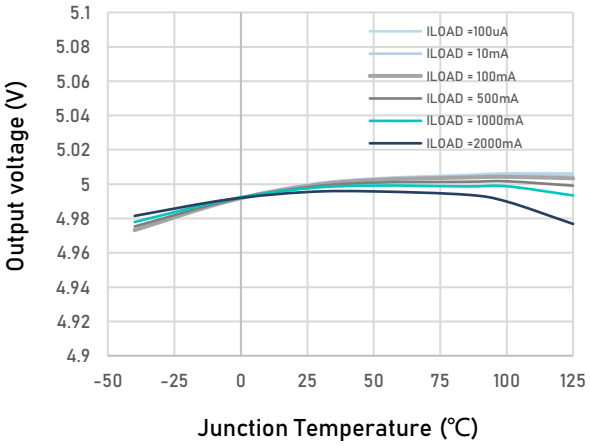


Figure 1. Output voltage vs Junction Temperature

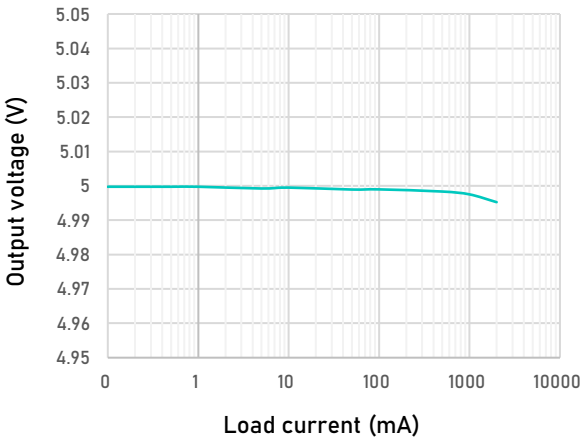


Figure 2. Output voltage vs Load current

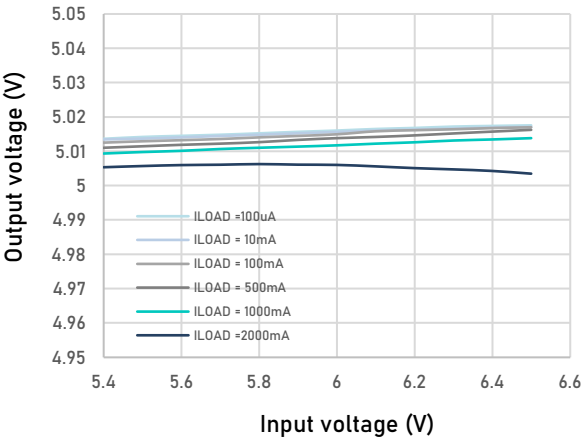


Figure 3. Output voltage vs Input voltage

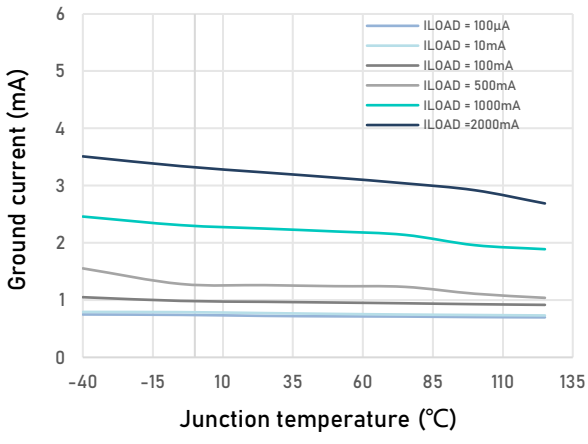


Figure 4. Ground current vs Junction temperature

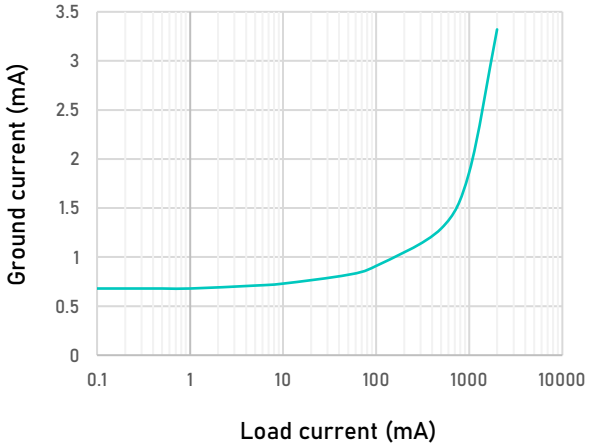


Figure 5. Ground current vs Load current

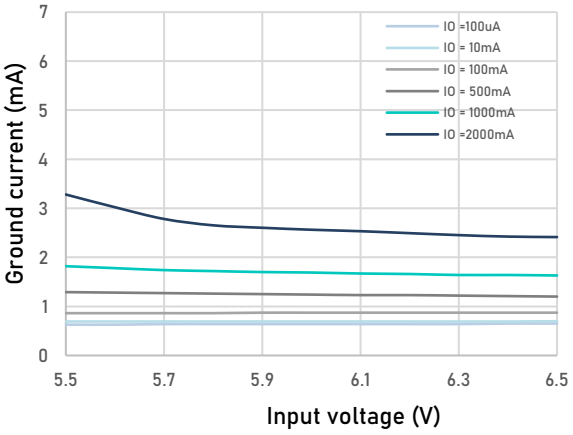


Figure 6. Ground current vs Input voltage

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

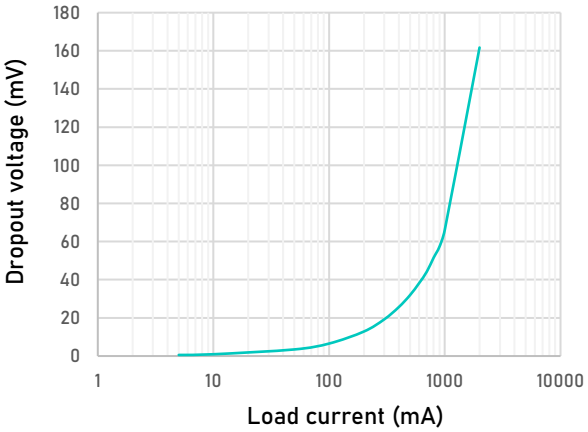


Figure 7. Dropout voltage vs Load current
(1.2 V Adjustable version & Vout = 5 V)

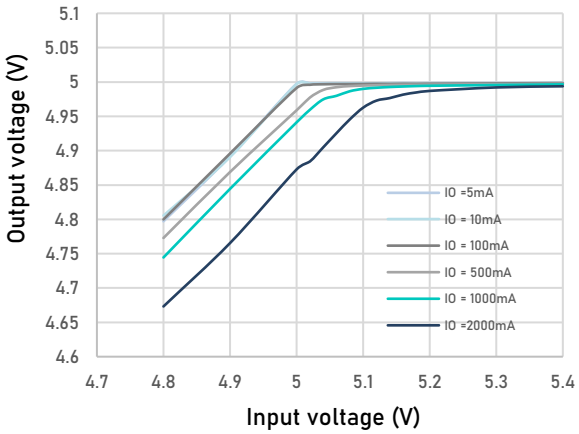


Figure 8. Output voltage vs Input voltage in dropout
(1.2 V Adjustable version & Vout = 5 V)

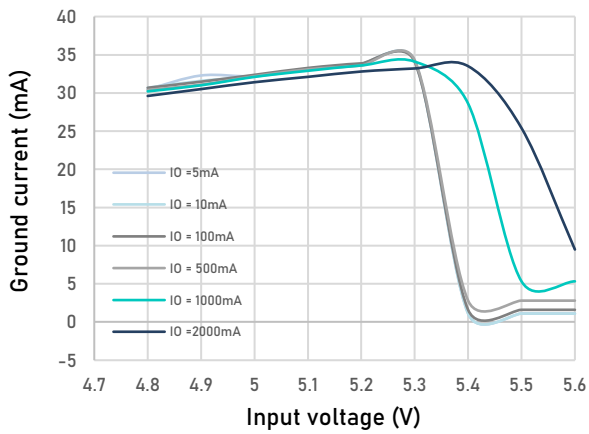


Figure 9. Ground current vs Input voltage in dropout
(1.2 V Adjustable version & Vout = 5 V)

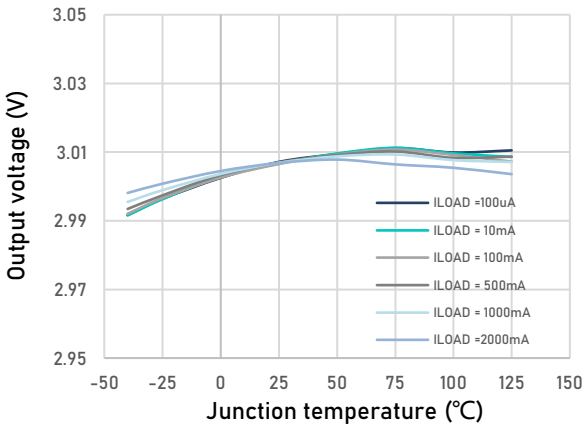


Figure 10. Output voltage vs Junction temperature
(Vout = 3 V)

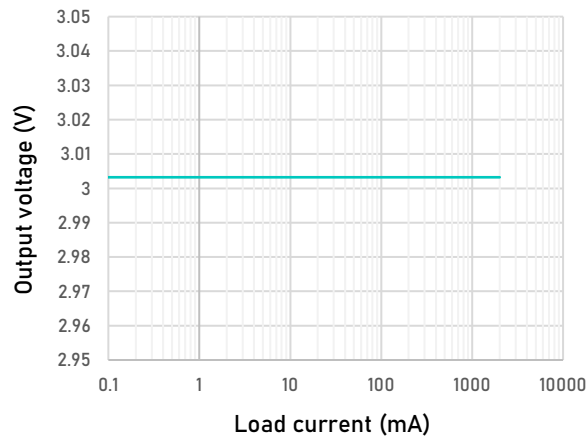


Figure 11. Output voltage vs Load current
(Vout = 3 V)

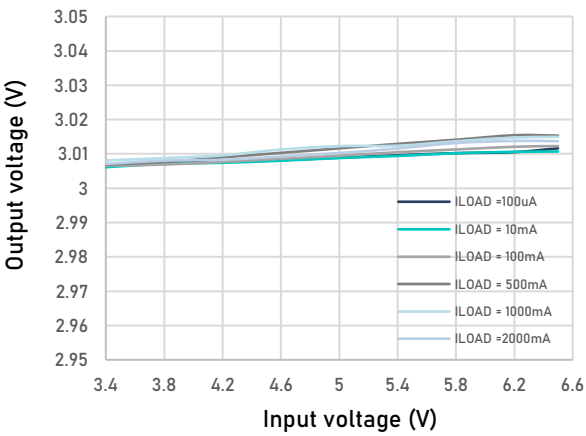


Figure 12. Output voltage vs Input voltage
(Vout = 3 V)

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

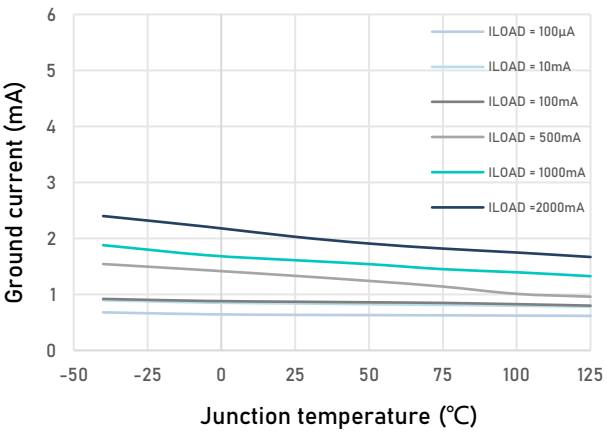


Figure 13. Ground current vs Junction temperature (Vout = 3 V)

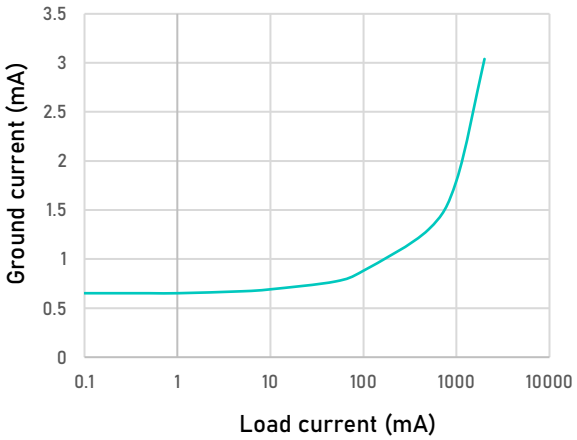


Figure 14. Ground current vs Load current (Vout = 3 V)

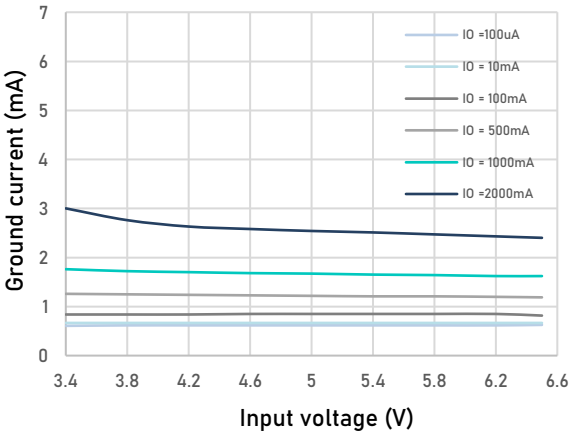


Figure 15. Ground current vs Input voltage (Vout = 3 V)

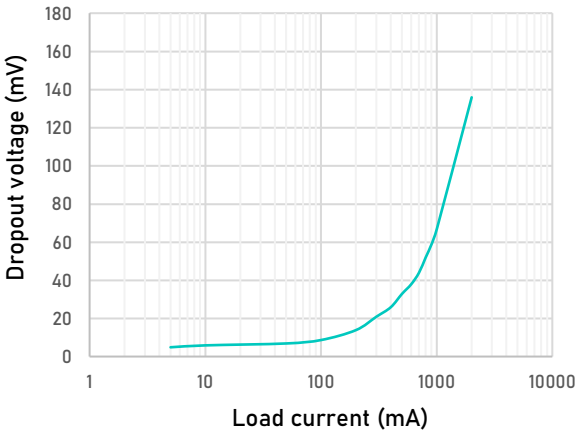


Figure 16. Dropout voltage vs Load current (Vout = 3 V)

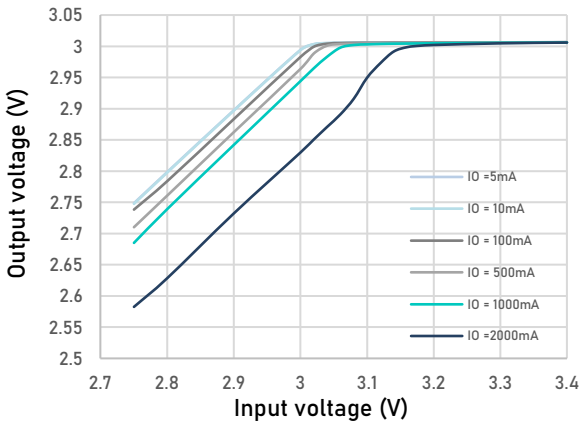


Figure 17. Output voltage vs Input voltage in dropout (Vout = 3 V)

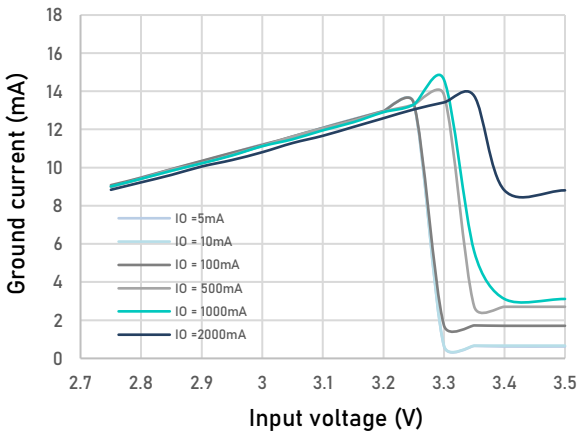


Figure 18. Ground current vs Input voltage in dropout (Vout = 3 V)

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

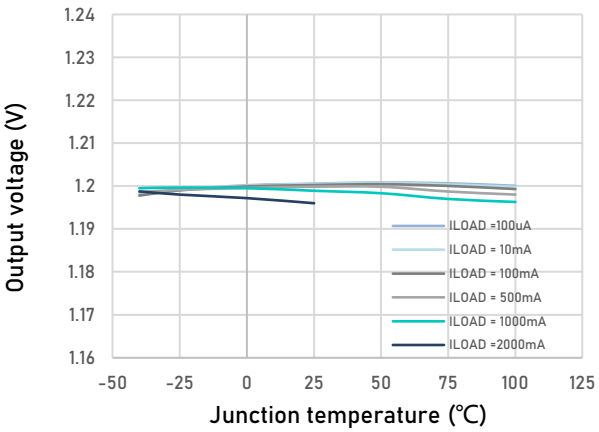


Figure 19. Output voltage vs Junction temperature
Adjustable version (Vout = 1.2 V)

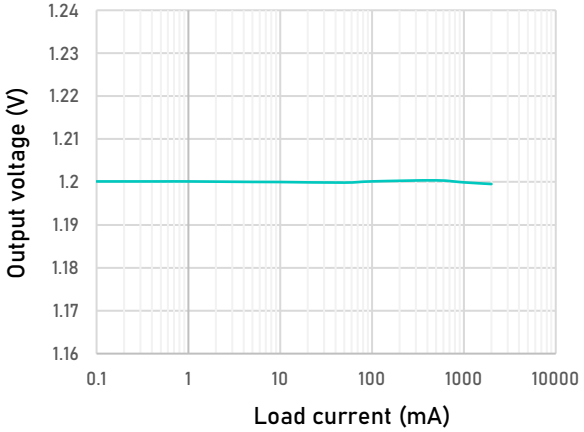


Figure 20. Output voltage vs Load current
Adjustable version (Vout = 1.2 V)

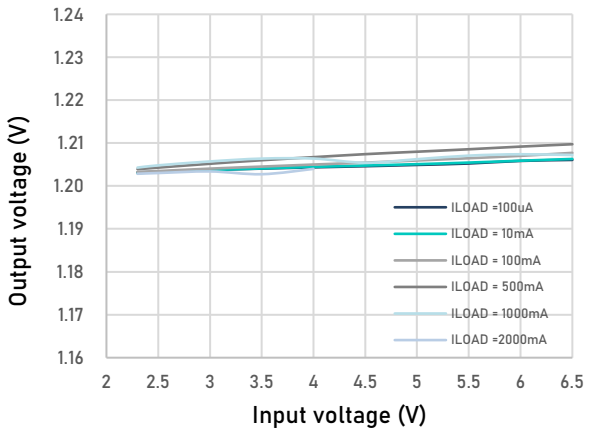


Figure 21. Output voltage vs Input voltage
Adjustable version (Vout = 1.2 V)

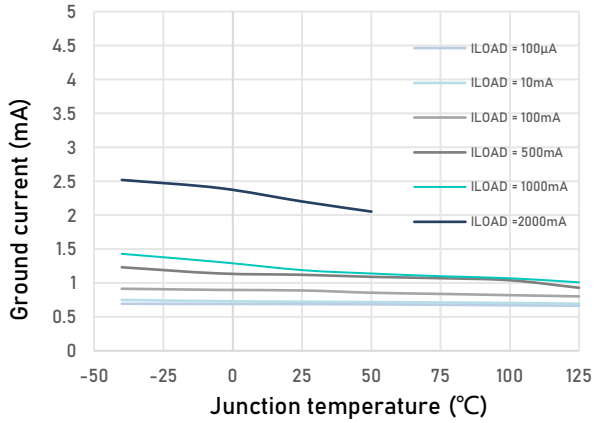


Figure 22. Ground current vs Junction temperature
Adjustable version (Vout = 1.2 V)

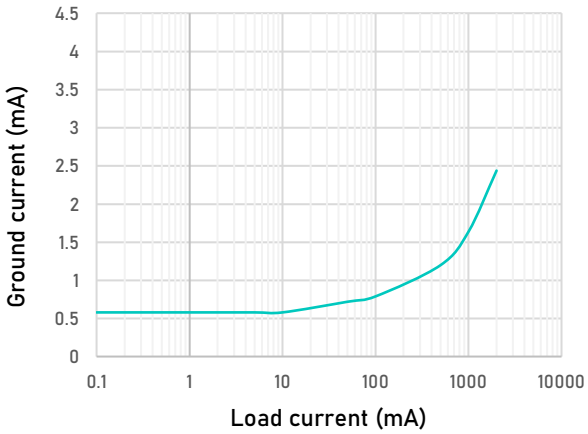


Figure 23. Ground current vs Load current
Adjustable version (Vout = 1.2 V)

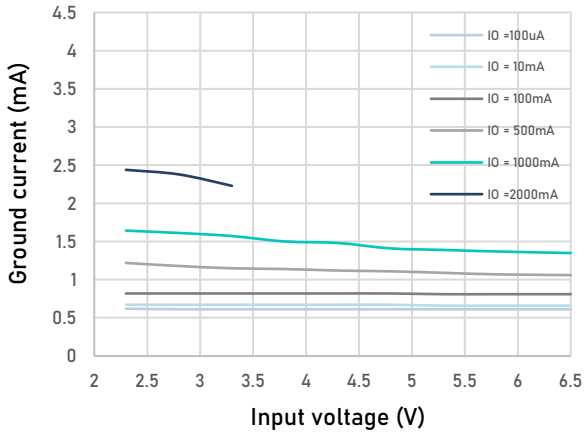


Figure 24. Ground current vs Input voltage
Adjustable version (Vout = 1.2 V)

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

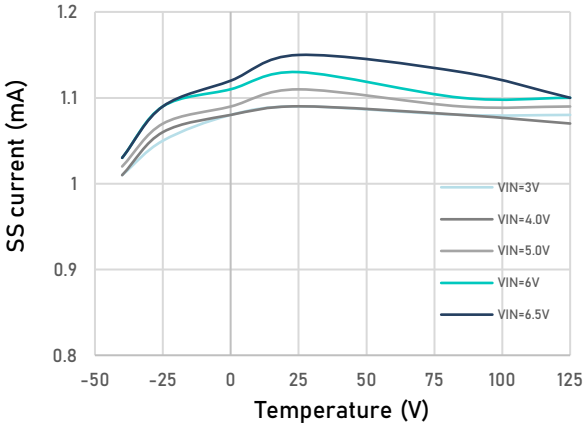


Figure 25. Soft start current vs Temperature, Input voltage (1.2 V Adjustable version & Vout = 5 V)

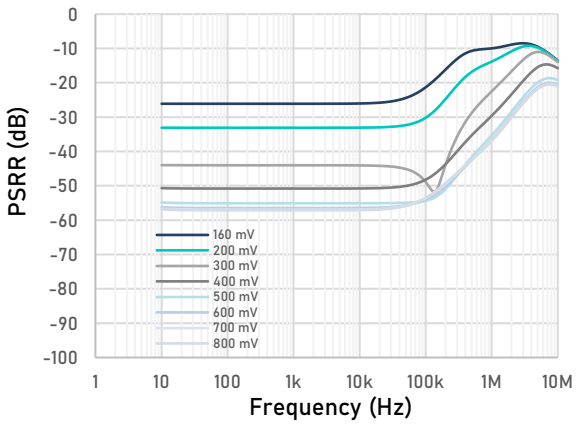


Figure 26. Power supply rejection ratio vs Frequency (Vout = 3 V, 2A load current, Various headroom voltages)

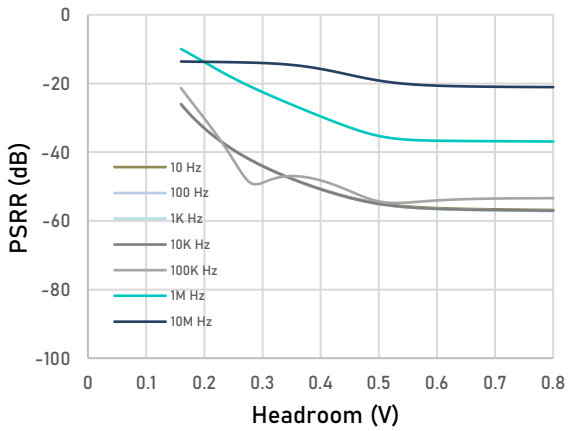


Figure 27. Power supply rejection ratio vs Headroom (Vout = 3 V, 2A load current, Different Frequencies)

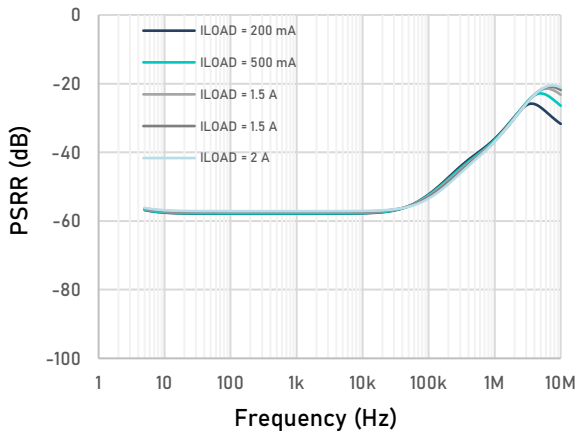


Figure 28. Power supply rejection ratio vs Frequency (Vout = 3 V, 800mV headroom)

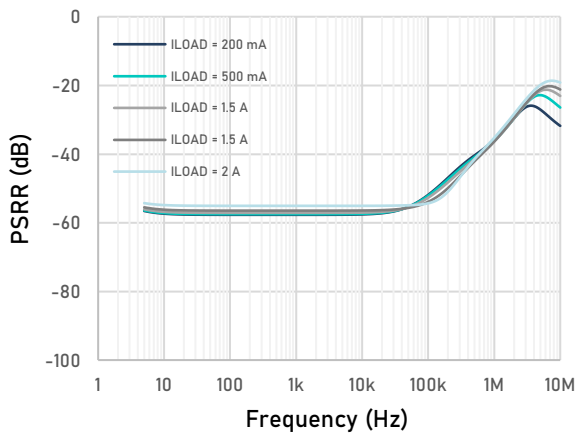


Figure 29. Power supply rejection ratio vs Frequency (Vout = 3 V, 500mV headroom)

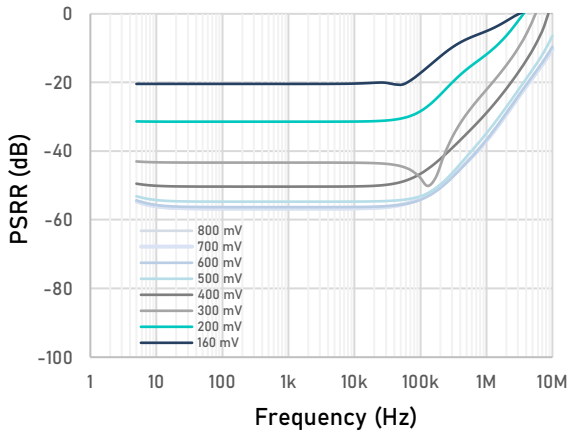


Figure 30. Power supply rejection ratio vs Frequency (1.2 V Adjustable version & Vout = 5 V, 2A load current, Various headroom voltages)

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

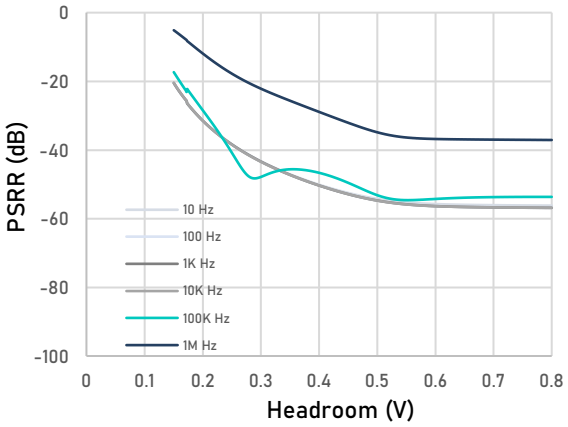


Figure 31. Power supply rejection ratio vs Headroom (1.2 V Adjustable version & Vout = 5 V, 2A load current, Different Frequencies)

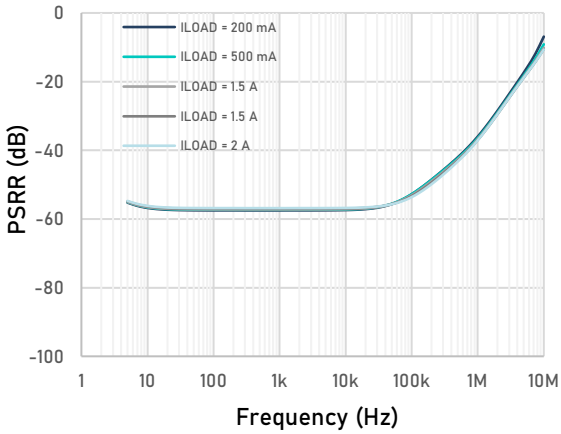


Figure 32. Power supply rejection ratio vs Frequency (1.2 V Adjustable version & Vout = 5 V, 800mV headroom)

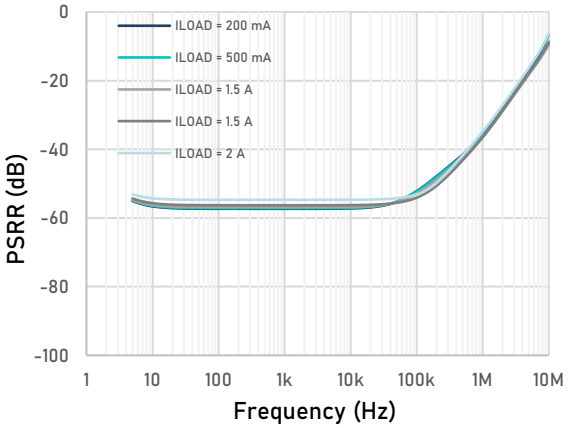


Figure 33. Power supply rejection ratio vs Frequency (1.2 V Adjustable version & Vout = 5 V, 500mV headroom)

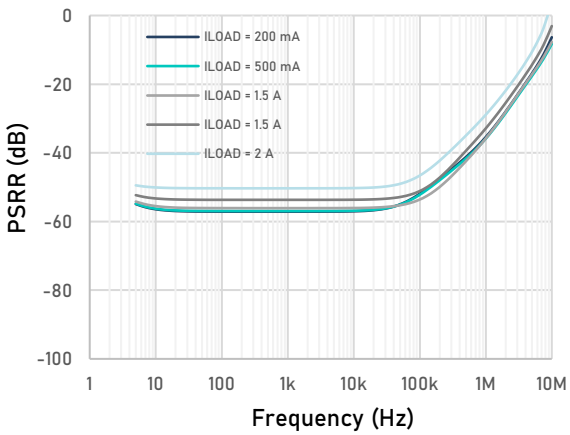


Figure 34. Power supply rejection ratio vs Frequency (1.2 V Adjustable version & Vout = 5 V, 400mV headroom)

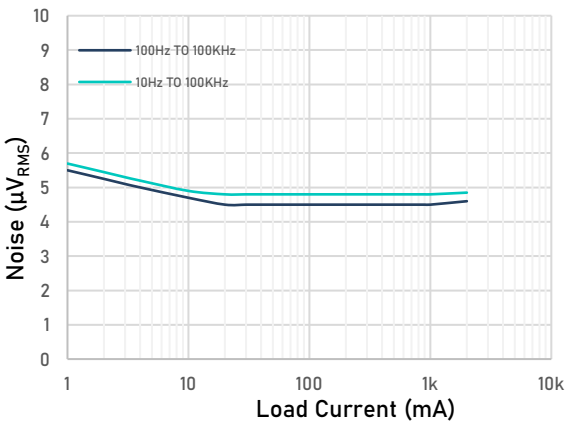


Figure 35. RMS Output Noise vs Load Current (Adjustable version Vout = 1.2 V)

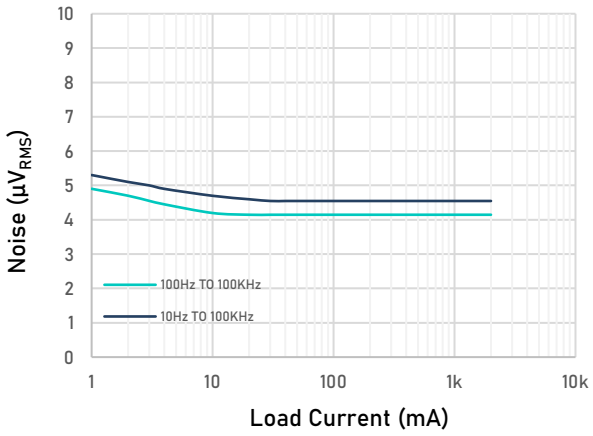


Figure 36. RMS Output Noise vs Load Current (Vout = 3 V)

Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

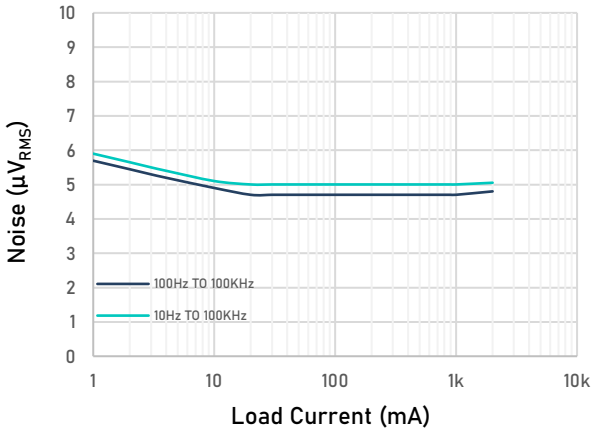


Figure 37. RMS Output Noise vs Load Current (1.2 V Adjustable version & Vout = 5 V)

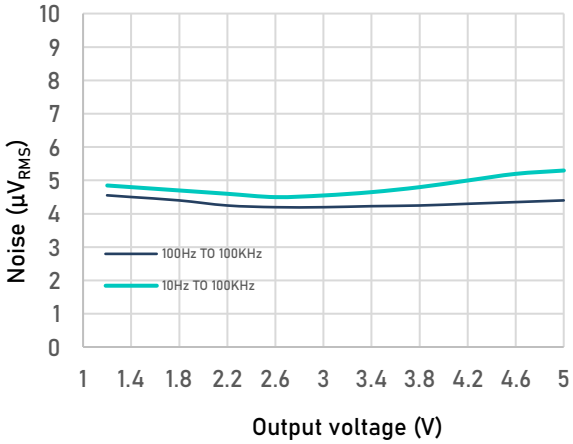


Figure 38. RMS Output Noise vs Output voltage (Load current = 100 mA)

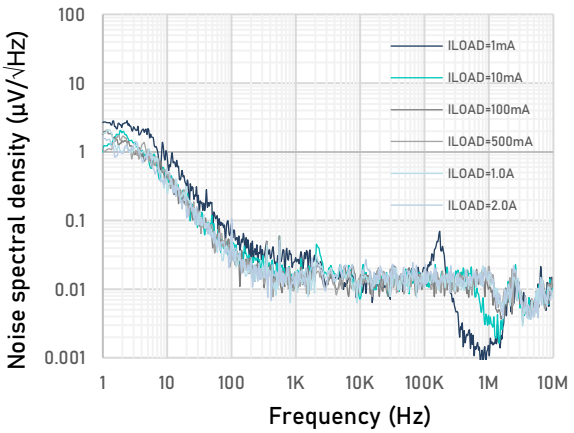


Figure 39. Output noise spectral density vs Frequency (Adjustable version Vout = 1.2 V)

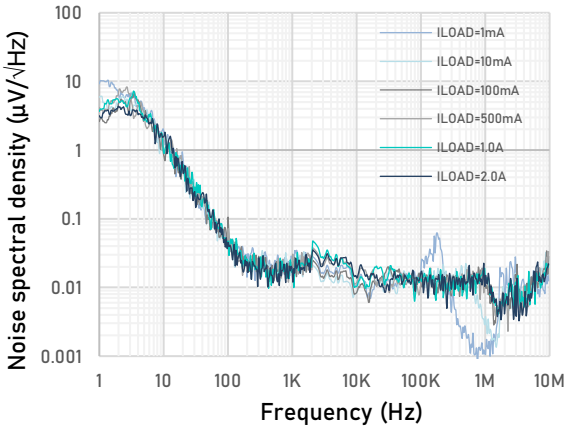


Figure 40. Output noise spectral density vs Frequency (Vout = 3 V)

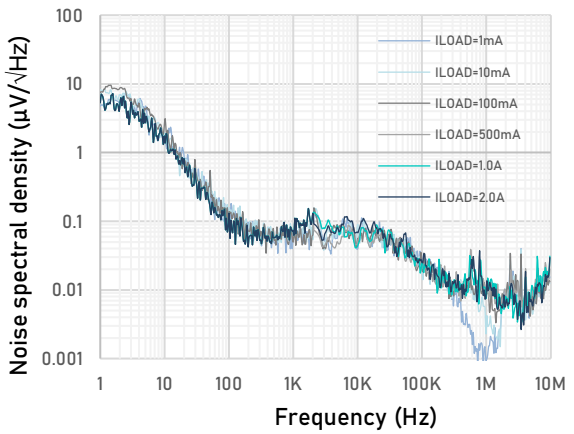


Figure 41. Output noise spectral density vs Frequency (1.2 V Adjustable version & Vout = 5 V)

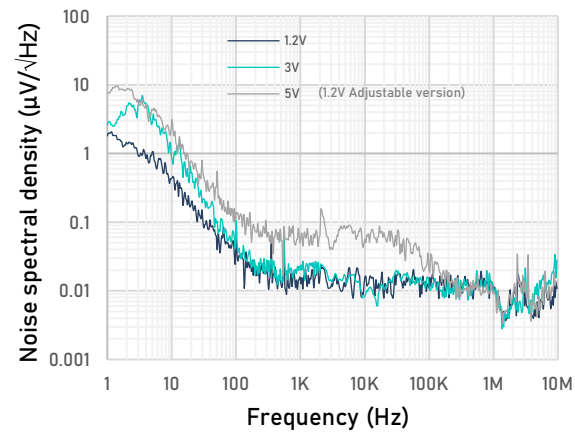
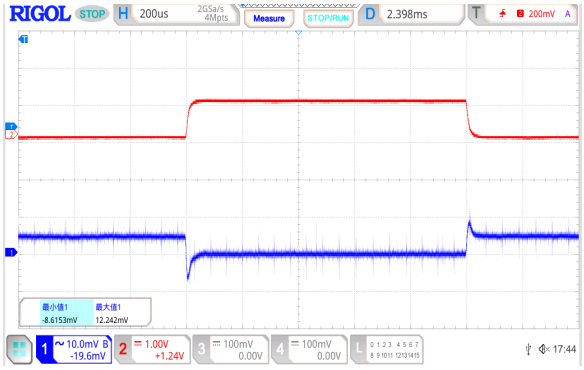


Figure 42. Output noise spectral density vs Frequency (Different output voltages, I_{LOAD} = 100 mA)

Note:

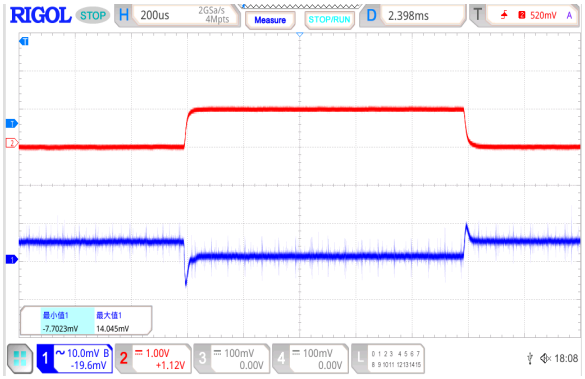
Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.



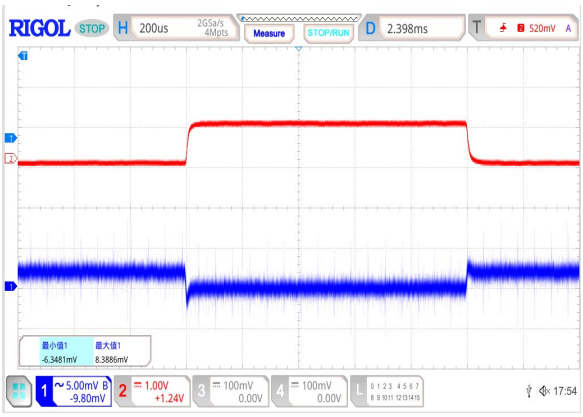
Time (200µs/div)

Figure 43. Load Transient Response, I_{LOAD} = 10 mA to 1 A, 1.2 V Adjustable version & Vout = 5 V, V_{IN} = 5.5 V, CH1 = V_{OUT}, CH2 = I_{LOAD}



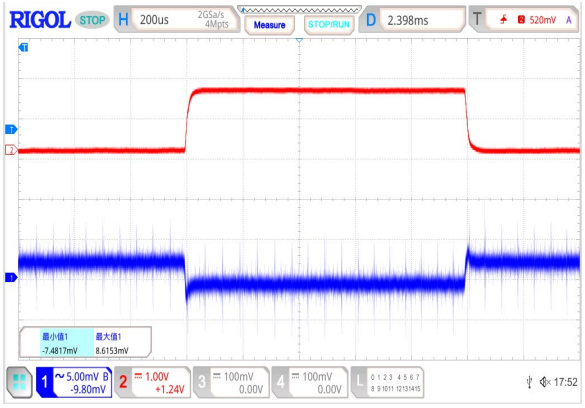
Time (200µs/div)

Figure 44. Load Transient Response, I_{LOAD} = 100 mA to 1.6 A, 1.2 V Adjustable version & Vout = 5 V, V_{IN} = 5.5 V, CH1 = V_{OUT}, CH2 = I_{LOAD}



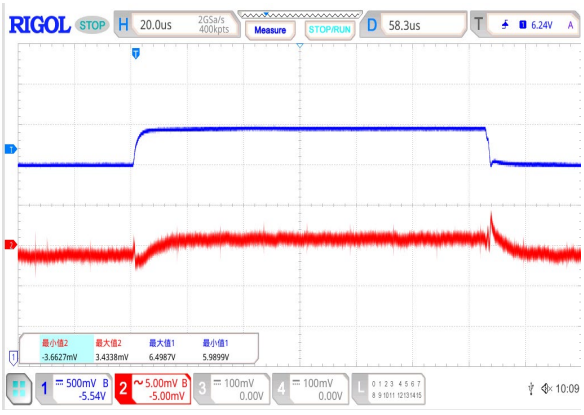
Time (200µs/div)

Figure 45. Load Transient Response, I_{LOAD} = 10 mA to 1 A, Adjustable Version , V_{OUT} = 1.2 V, V_{IN} = 2.5 V, CH1 = V_{OUT}, CH2 = I_{LOAD}



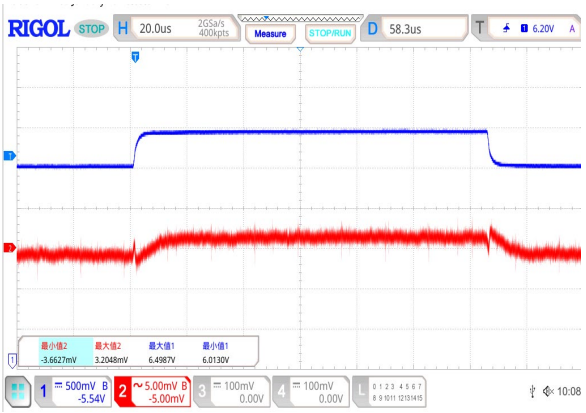
Time (200µs/div)

Figure 46. Load Transient Response, I_{LOAD} = 100 mA to 1.6 A, Adjustable Version , V_{OUT} = 1.2 V, V_{IN} = 2.5 V, CH1 = V_{OUT}, CH2 = I_{LOAD}



Time (20µs/div)

Figure 47. Line Transient Response, 6 V to 6.5 V, I_{LOAD} = 500 mA, 1.2 V Adjustable version & Vout = 5 V, CH1 = V_{IN}, CH2 = V_{OUT}

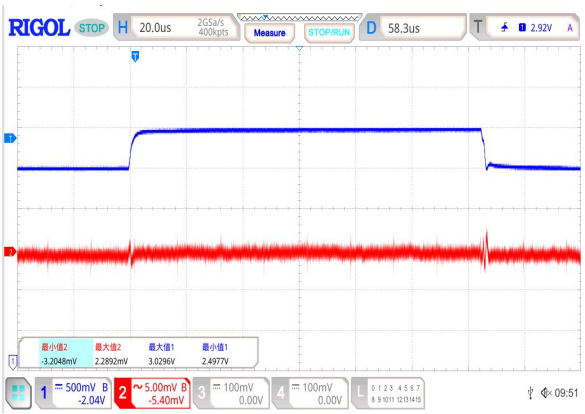


Time (20µs/div)

Figure 48. Line Transient Response, 6 V to 6.5 V, I_{LOAD} = 2 A, 1.2 V Adjustable version & Vout = 5 V, CH1 = V_{IN}, CH2 = V_{OUT}

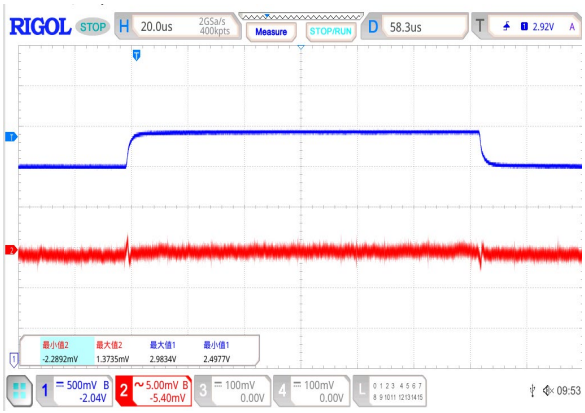
Typical Performance Characteristics

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.



Time (20µs/div)

Figure 49. Line Transient Response, 2.5 V to 3 V, I_{LOAD} = 500 mA, Adjustable Version , V_{OUT} = 1.2V, CH1 = V_{IN}, CH2 = V_{OUT}



Time (20µs/div)

Figure 50. Line Transient Response, 2.5 V to 3 V, I_{LOAD} = 2 A, Adjustable Version , V_{OUT} = 1.2V, CH1 = V_{IN}, CH2 = V_{OUT}

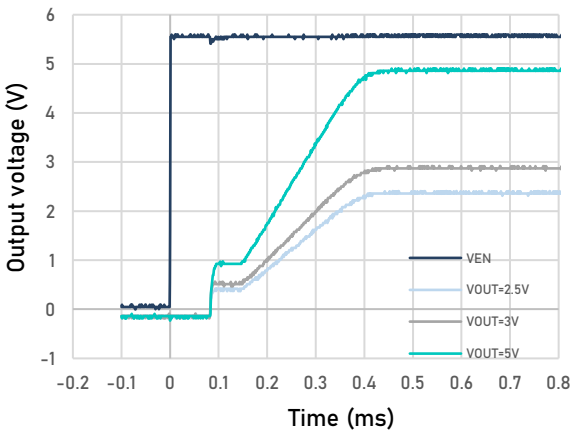


Figure 51. Typical start-up behavior

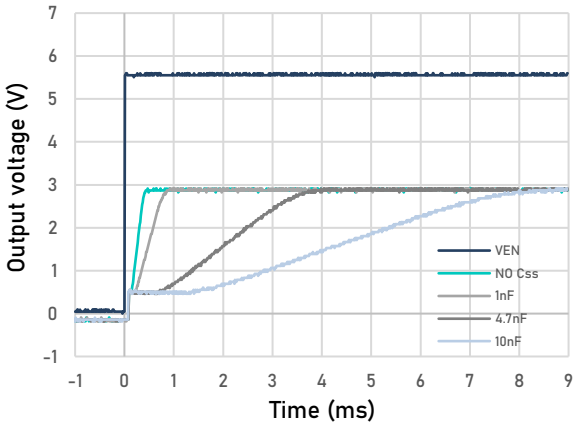
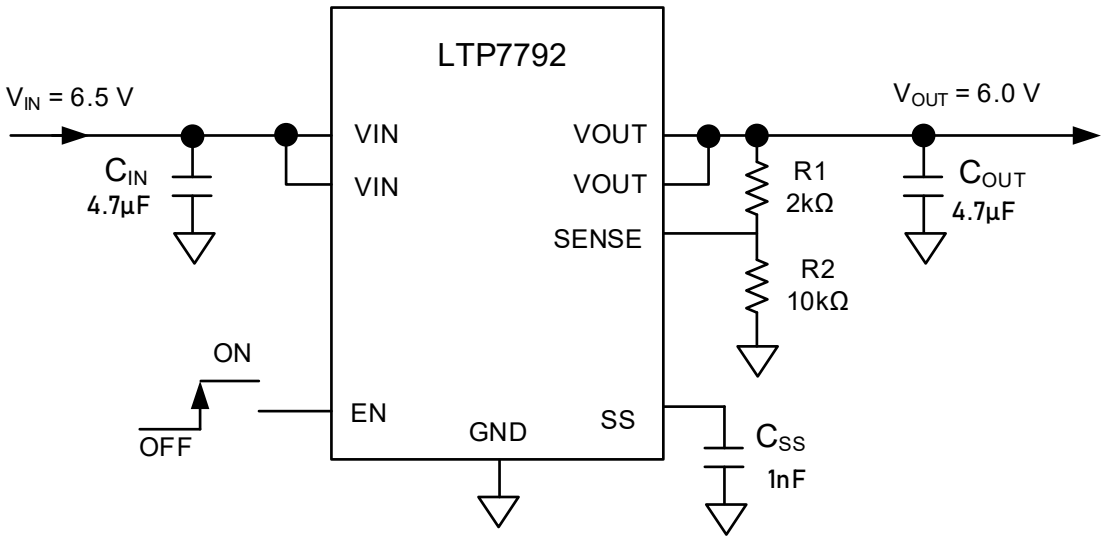
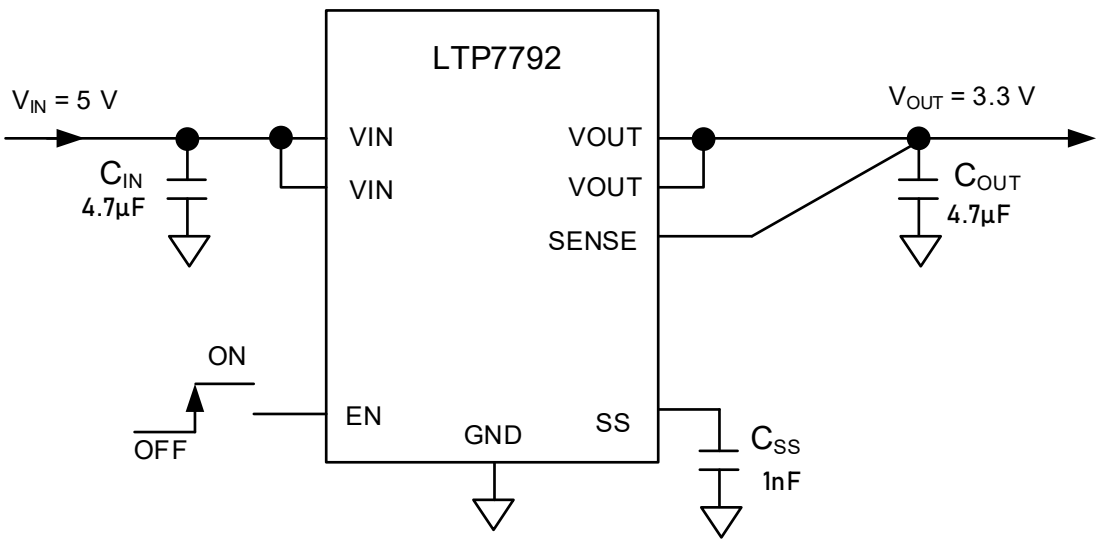


Figure 52. Typical soft start behavior, Different Css values

Application Circuits



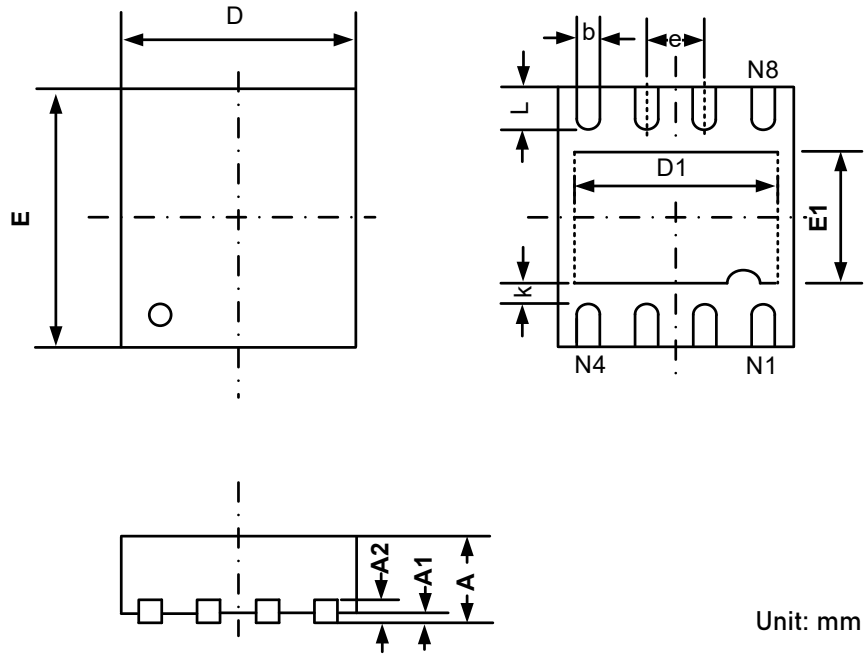
Typical Adjustable Output Voltage Application Schematic



Fixed Output Voltage, 3.3 V

Package Dimension

DFN3×3-8



Unit: mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	0.700	0.800
A1	0.000	0.050
A2	0.203REF	
b	0.180	0.300
D	2.900	3.100
D1	2.200	2.400
E	2.900	3.100
E1	1.400	1.600
e	0.650BSC	
L	0.375	0.575
k	0.200	