1. General Description

The LTP8036 is a series of multifunctional microprocessor supervisory circuit that monitors supply voltage rails from 0.4 V to 5 V. When the voltage on SENSE pin drops below the factory-preset threshold, or the manual reset pin ($\overline{MR}$) switches to logic low, the device asserts an open-drain $\overline{RESET}$ output signal. Only when the both trigger conditions are removed, the output $\overline{RESET}$ recovers after a user-defined delay time.

The LTP8036 employs a high-precision internal bandgap voltage reference to provide 1% threshold accuracy for all threshold voltage versions. The reset delay time is adjustable by changing the setup of the connection of C_T pin. The delay time can be set to 20 ms by floating the C_T, or 300 ms by connecting C_T to V_{DD} through a resistor, or vary from 1.25 ms to 10 s by adjusting the external capacitor connected to C_T. The device features an ultra-low-power consumption. A quiescent current as low as 0.6 μA makes the device suitable for any power sensitive applications, for example battery-powered devices. It is available in SOT23-6L and DFN2×2-6L packages and is fully specified over a temperature range of -40℃ to 125℃.

2. Features and Benefits

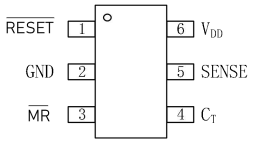
- Adjustable delay time: 1.25 ms to 10 s.
- Ultra-low quiescent current: 0.6 μA typical
- High threshold accuracy: 1%
- Fixed threshold voltages for standard voltage rails from 0.9 V to 5 V or adjustable voltage down to 0.4V
- Manual reset input: $\overline{MR}$
- Open-drain output: $\overline{RESET}$
- Small packages: available in SOT23-6L and DFN2×2-6L
- Temperature range: -40℃ to 125℃

3. Applications

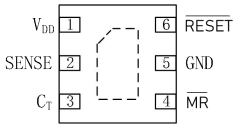
- Microprocessor or micro-controller applications
- Personal computers
- Battery-powered products
- Portable and hand-held products
- FPGA and ASIC applications

4. Pin Configuration (Top View)

SOT23-6L



DFN2×2-6L



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5. Device Versions and Thresholds

Version	Nominal Supply Voltage	Threshold voltage
LTP8036-01	Adjustable by external resistor divider	0.405 V
LTP8036-09	0.9 V	0.84 V
LTP8036-12	1.2 V	1.12 V
LTP8036-125	1.25 V	1.16 V
LTP8036-15	1.5 V	1.40 V
LTP8036-18	1.8 V	1.67 V
LTP8036-19	1.9 V	1.77 V
LTP8036-25	2.5 V	2.33 V
LTP8036-30	3 V	2.79 V
LTP8036-33	3.3 V	3.07 V
LTP8036-50	5 V	4.65 V

6. Pin Description

Symbol	Pin Number		Description
	SOT23-6L	DNF2×2-6L	
C_T	4	3	Delay time programming pin. Detailed information is given in section 13.2.2.
GND	2	5	Ground pin.
$\overline{MR}$	3	4	Manual reset pin. By driving $\overline{MR}$ low, $\overline{RESET}$ is asserted. $\overline{MR}$ is internally tied to V_{DD} through a pull-up resistor.
$\overline{RESET}$	1	6	Open-drain output pin. $\overline{RESET}$ remains to be logic low for user defined delay period after SENSE voltage recovers to be above V_{IT} and $\overline{MR}$ is set to logic high. $\overline{RESET}$ pin requires an external 10 kΩ to 1 MΩ pull-up resistor to supply voltage which is allowed to be higher than V_{DD}
SENSE	5	2	Input pin connected to the voltage expected to be monitored. Once the voltage drops below the preset threshold voltage V_{IT}, the $\overline{RESET}$ is asserted.
V_{DD}	6	1	Supply voltage pin. It is recommended to place a 0.1 μF ceramic capacitor as close as possible to this pin.
Thermal Pad	NA	Thermal Pad	Thermal pad. Connect to ground plane for enhanced thermal performance.

7. Typical Applications Diagram

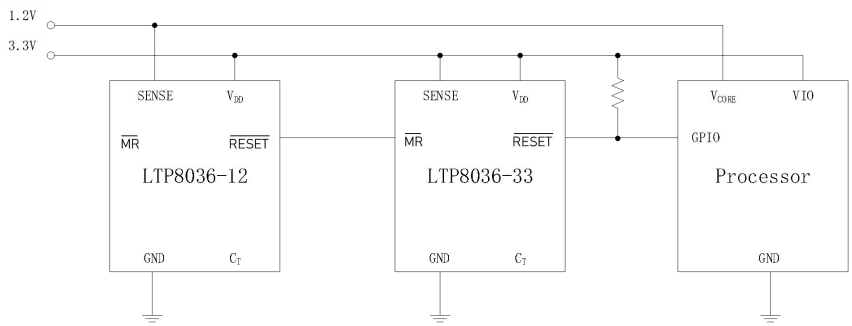


Fig.1 Dual supply rails simultaneously monitoring

8. Ordering Information

Part Number	Package Type	Quantity	Mark Code
LTP8036-01XT6/R6	SOT23-6L	Tape and Reel, 3000	3601
LTP8036-01XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3601
LTP8036-09XT6/R6	SOT23-6L	Tape and Reel, 3000	3609
LTP8036-09XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3609
LTP8036-12XT6/R6	SOT23-6L	Tape and Reel, 3000	3612
LTP8036-12XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3612
LTP8036-125XT6/R6	SOT23-6L	Tape and Reel, 3000	3613
LTP8036-125XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3613
LTP8036-15XT6/R6	SOT23-6L	Tape and Reel, 3000	3615
LTP8036-15XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3615
LTP8036-18XT6/R6	SOT23-6L	Tape and Reel, 3000	3618
LTP8036-18XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3618
LTP8036-19XT6/R6	SOT23-6L	Tape and Reel, 3000	3619
LTP8036-19XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3619
LTP8036-25XT6/R6	SOT23-6L	Tape and Reel, 3000	3625

LTP8036-25XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3625
LTP8036-30XT6/R6	SOT23-6L	Tape and Reel, 3000	3630
LTP8036-30XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3630
LTP8036-33XT6/R6	SOT23-6L	Tape and Reel, 3000	3633
LTP8036-33XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3633
LTP8036-50XT6/R6	SOT23-6L	Tape and Reel, 3000	3650
LTP8036-50XF6/R6	QFN2×2-6L	Tape and Reel, 3000	3650

9. Limiting Value

Parameter	MIN	MAX	UNIT
V_{DD}, $V_{\overline{RESET}}$, $V_{\overline{MR}}$, V_{SENSE}	-0.3	7	V
V_{CT}	-0.3	V_{DD}+0.3	V
$I_{\overline{RESET}}$	-5	5	mA
T_J	-40	150	℃
T_{STG}	-65	150	℃

10. ESD Ratings

Parameter	Level	UNIT
Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±4000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1000	V

11. Electrical Characteristics

1.65 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = −40°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

Parameter		Conditions	Min	Typ	Max	Unit
V_{DD},	Input supply range	-40 ℃ ≤ T_J ≤ 125 ℃	1.65		6.5	V
I_{DD}	Supply current	V_{DD} = 3.3 V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, and CT open		0.6	1.2	µA
		V_{DD} = 6.5 V $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, and C_T open		0.95	1.9	
V_{OL}	Low-level output voltage	1.3 V ≤ V_{DD} ≤ 1.8 V, I_{OL} = 0.4 mA			0.15	V
		1.8 V ≤ V_{DD} ≤ 6.5 V, I_{OL} = 1 mA			0.2	
V_{POR}	Power-up reset voltage	V_{OL}(max) = 0.2 V, $I_{\overline{RESET}}$ = 15 µA			0.8	V
V_{IT}	Negative-going input threshold accuracy	All version, T_A = 25 ℃	-1		1	%
		V_{IT} ≤ 3.3 V	-1.5		1.5	
		3.3 V ≤ V_{IT} ≤ 5 V	-1.8		1.8	
V_{HYS}	Hysteresis on V_{IT}	All versions			3	%
$R_{\overline{MR}}$	$\overline{MR}$ internal pull-up resistance		80	100		kΩ
I_{SENSE}	Input current at SENSE pin	LTP8036-01, V_{SENSE} = V_{IT}	-10		10	nA
		The other versions, V_{SENSE} = 6.5 V		235		nA
I_{OH}	$\overline{RESET}$ leakage current	$V_{\overline{RESET}}$ = 6.5V, $\overline{RESET}$ not asserted			0.1	µA
C_{IN}	Input capacitance, any pin	C_T pin, V_{IN} = 0 V to 6.5 V		5		pF
		The other pins, V_{IN} = 0 V to 6.5 V		5		
V_{IL}	$\overline{MR}$ input logic low		0		0.3V_{DD}	V
V_{IH}	$\overline{MR}$ input logic high		0.7V_{DD}		V_{DD}	V
t_{SENSE}	Input pulse width to $\overline{RESET}$	V_{IH} = 1.05V_{IT}, V_{IL} = 0.95V_{IT}		65		µs
$t_{\overline{MR}}$	Input pulse width to $\overline{RESET}$	V_{IH} = 0.7V_{IT}, V_{IL} = 0.3V_{IT}		85		ns
$V_{TH-RAMP}$	C_T source threshold voltage			1.22		V
t_D	$\overline{RESET}$ delay time	C_T floating		20		ms

		C_T = V_{DD}	300	ms
		C_T = 100 pF	1.1	ms
t_{MR}	Propagation delay	$\overline{MR}$ to $\overline{RESET}$	70	ns
t_{PRO}	High-to-low level $\overline{RESET}$ delay	SENSE to $\overline{RESET}$	55	µs

12. Typical Characteristics

T_J = +25 ℃, V_{DD} = 3.3 V and R_{LRESET} = 100 kΩ, unless otherwise noted.

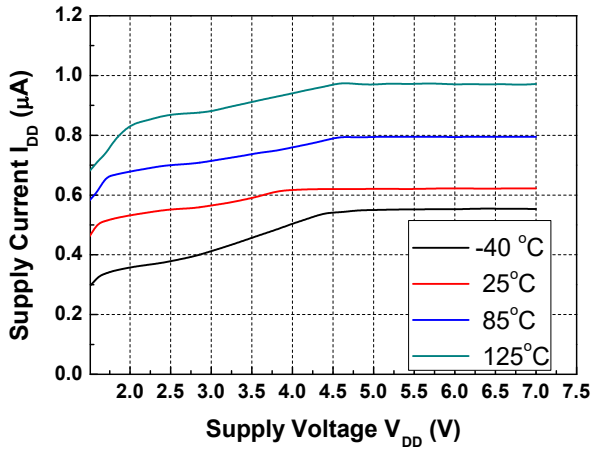


Fig.2 Supply Current I_{DD} vs. Supply Voltage V_{DD}

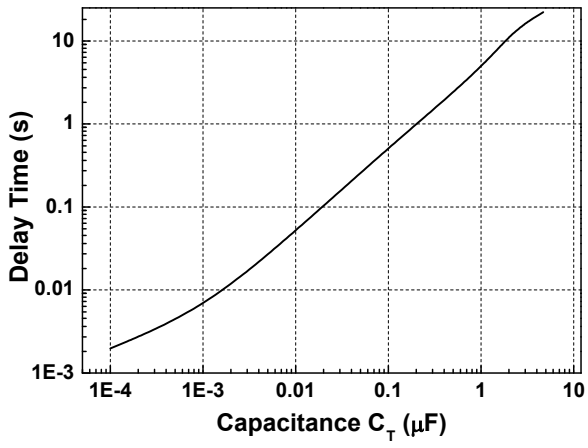


Fig.3 External Capacitance C_T vs. Recovery Delay Time

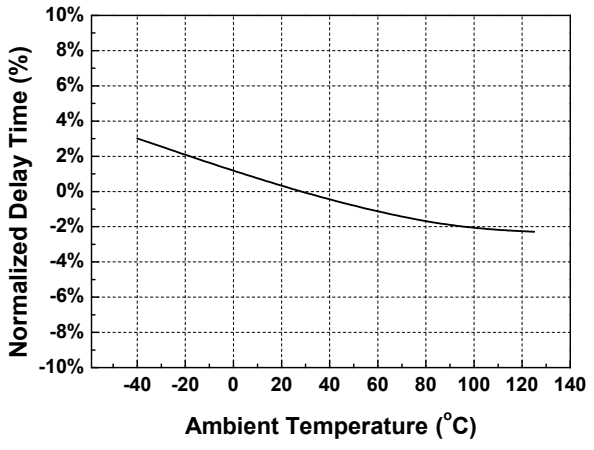


Fig.4 Normalized Delay Time vs. Ambient Temperature

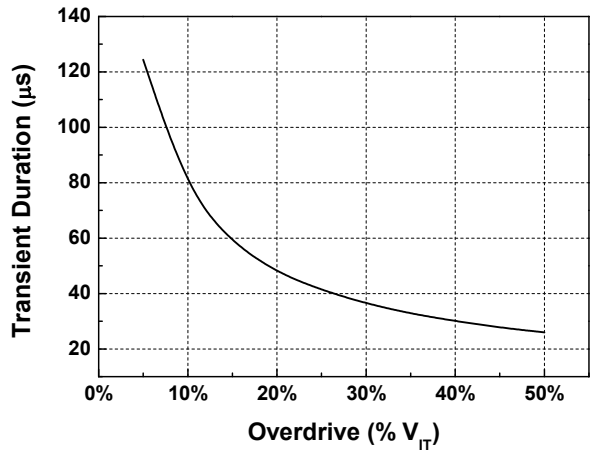


Fig.5 Transient Duration vs. Overdrive

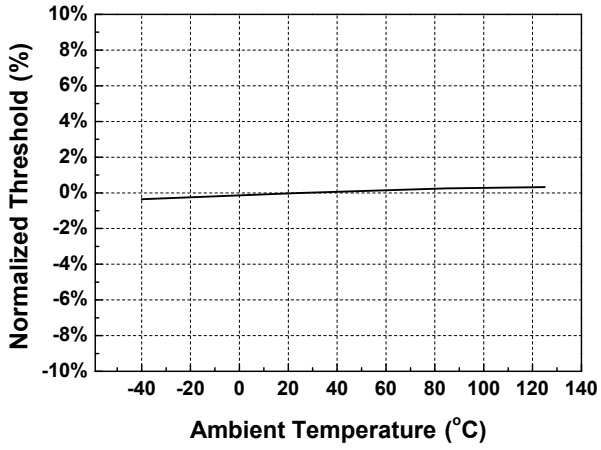


Fig.6 Normalized Threshold vs. Ambient Temperature

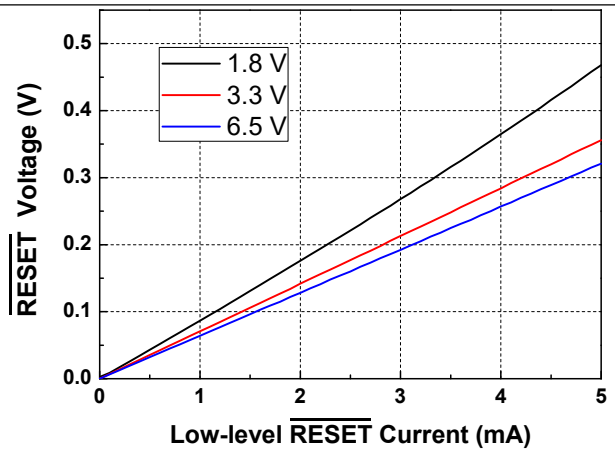


Fig.7 Low-level $\overline{RESET}$ Voltage vs. $\overline{RESET}$ Current under Different Supply Voltage

13. Detailed Description

13.1. Functional Block Diagram

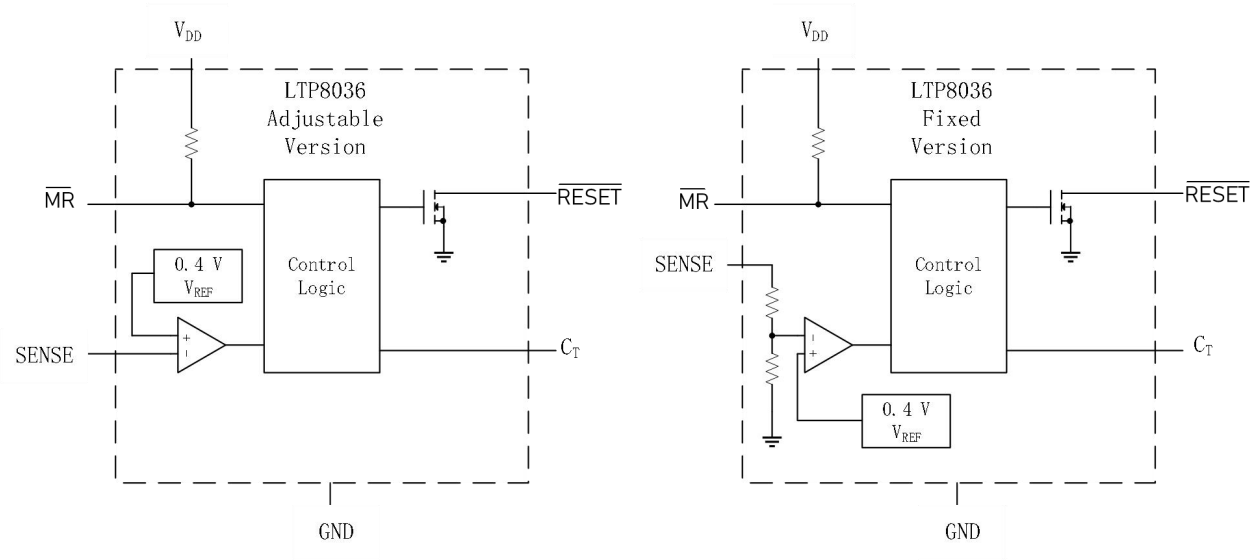


Fig.8 Functional block diagram

13.2. Feature Description

The LTP8036 series provide options of a wide range of monitoring voltage threshold and reset delay time. Such property makes it suitable for various applications. Fixed threshold voltage versions could cover from 0.9 V up to 5 V as the supply voltage being monitored. The threshold voltage of adjustable version can be set to any voltage above 0.405V by external resistor divider. Users can select from two preset reset delay time: 20 ms by floating C_T pin and 300 ms by connecting C_T pin to V_{DD} through resistor, or users can choose any delay time between 1.25 ms to 10 s by varying the capacitance of external capacitor between C_T and ground

13.2.1. Sense Input

SENSE pin senses the input voltage to be monitored, and will assert $\overline{\text{RESET}}$ if the voltage being sensed drops below the threshold. A built-in hysteresis of the comparator avoids uncertainty near the threshold value. It is recommended to place a 1 nF to 10 nF bypass capacitor on the SENSE pin to reduce transients and layout parasitics. The SENSE pin can endure short negative transients, and the endurable time is related to the threshold overdrive as shown in Fig.5. The adjustable version LTP8301 can set the threshold voltage to any value above 0.405 V using circuit shown below.

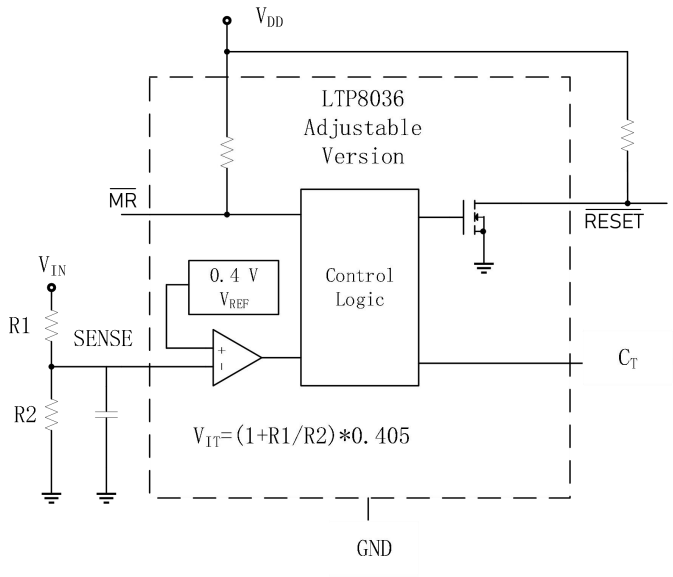


Fig.9 Adjustable threshold set by external resistor divider using LTP8036-01

13.2.2. Reset Delay Time

The reset delay time of the device can be selected from two fixed values or configured by varying the capacitance value connected to C_T pin. By floating C_T, a fixed 20 ms delay time is set. By connecting the C_T to V_{DD} through a resistor, from 40 kΩ to 200 kΩ, a fixed 300 ms delay time is set. User defined delay time between 1.25 ms to 10 s can be programmed by an external ground-referenced capacitor.

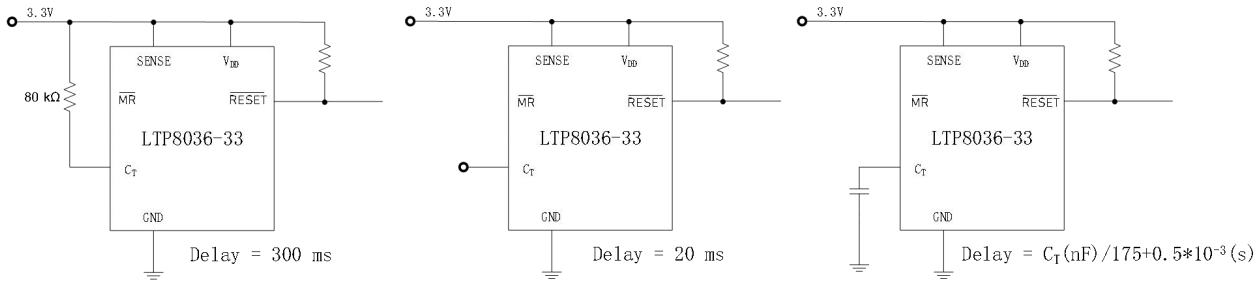


Fig.10 Delay time configuration

The reset delay time is determined by the charging time of a precise internal 220 nA current source to charge the external capacitor to 1.23 V. It follows the relations shown as below:

$$T_D = C_T(nF)/175+0.5*10^{-3}(s)$$

When reset condition is triggered either by SENSE pin or manual reset pin, the capacitor discharges. When the conditions are removed, the current source starts to charge the capacitor until its voltage reaches 1.23 V, and therefore deassert the status of $\overline{\text{RESET}}$. In order to have a smaller error in reset delay time, it recommended to use low-leakage ceramic capacitor.

13.2.3. Manual Reset Input

The manual reset input provides an active way to trigger a reset, by switching $\overline{\text{MR}}$ to logic low. This pin is internally pulled up through a resistor to V_{DD}, so this pin can be left floated. It is recommended to use a MOSFET to minimize drawing current in case the driving voltage on $\overline{\text{MR}}$ does not match with V_{DD}.

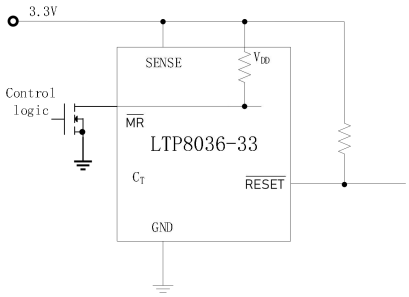


Fig.11 Use a MOSFET to deal with driving voltage mismatch

13.2.4. Reset Output

Either condition which is voltage to be monitored dropping below threshold or $\overline{MR}$ switching to logic low, will assert the reset output, driving the $\overline{RESET}$ pin to a low impedance. After both conditions are removed, the delay circuit starts up to provide a user-defined delay time. The external pull-up resistor help to get a voltage higher than V_{DD}.

13.3. Power-On Reset Function

Depending on power supply condition, the device works in three modes, explained as following:

13.3.1. Normal Operation

When supply voltage V_{DD} meets the basic requirements to make the circuits work, i.e. greater than $V_{DD(min)}$, the output $\overline{RESET}$ behaves according to voltage on the SENSE pin and the logic state of $\overline{MR}$ as introduced in previous sessions.

13.3.2. Above Power-On Reset Voltage but below $V_{DD(min)}$

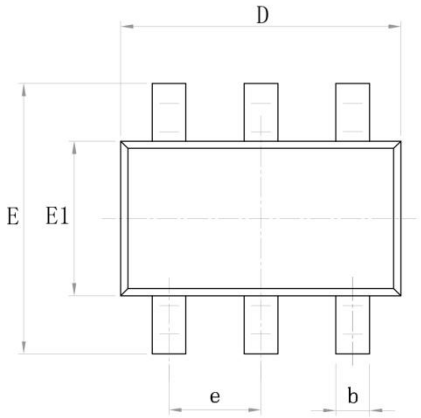
When the supply voltage is above power-on reset voltage V_{POR} but below $V_{DD(min)}$, the $\overline{RESET}$ remains asserted and low impedance no matter what state of voltage is on SENSE pin and $\overline{MR}$.

13.3.3. Below Power-On Reset Voltage

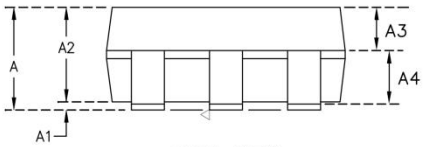
When the supply voltage is below V_{POR}, $\overline{RESET}$ is not defined.

14. Package Outlines

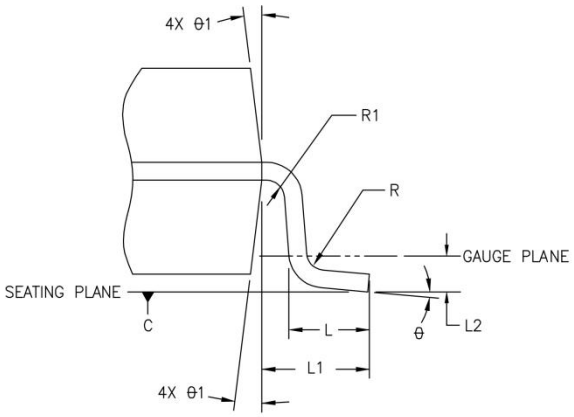
SOT23-6L



TOP VIEW

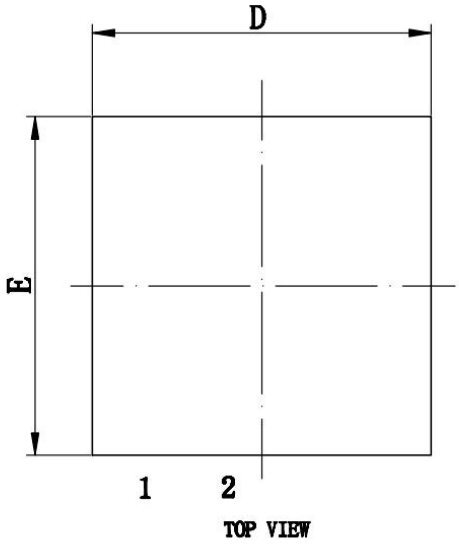


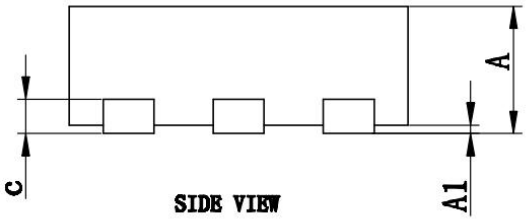
SIDE VIEW

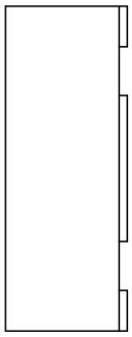


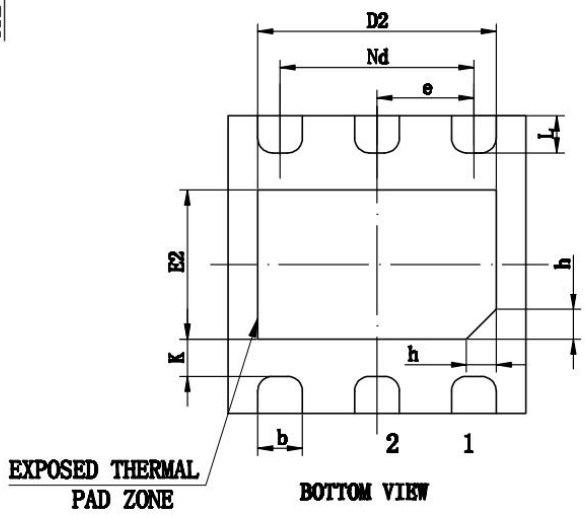
Symbol	尺寸(mm)		
	Min.	Nom.	Max.
A	1.00	---	1.35
A1	0.00	---	0.15
A2	1.00	1.10	1.20
A3	0.349	0.399	0.449
A4	0.511	---	0.701
b	0.35	---	0.45
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
L	0.35	0.45	0.60
L1		0.60 REF	
L2		0.25 REF	
R	0.10	---	---
R1	0.10	---	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

DFN2*2-6L









Symbol	尺寸(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	---	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e		0.65 BSC	
Nd		1.30 BSC	
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
K	0.20	---	---
L	0.20	0.25	0.30
L1	0.15	0.20	0.25