24V, 2.5uA IQ, 100mA Low-Dropout Linear Voltage Regulator

Description

The DX7550M series is a high voltage，ultralow-power，low dropout voltage regulator. The device can deliver 100mA output current with a dropout voltage of 450mV@100mA and allows an input voltage as high as 24V. The typical quiescent current is only 2.5μA.

The DX7550M is ideally suited for standby micro-control-unit systems, especially for always-on applications like E-meters, fire alarms, smoke detectors and other battery operated systems. The DX7550M retains all of the features that are common to low dropout regulators including a low dropout PMOS pass device, short circuit protection, and thermal shutdown.

Applications

- ◆ Portable, Battery Powered Equipment
- ◆ Smoke detector and sensor
- ◆ Audio/Video Equipmen
- ◆ Weighting Scales
- ◆ Home Automation
- ◆ Electronic fingerprint lock

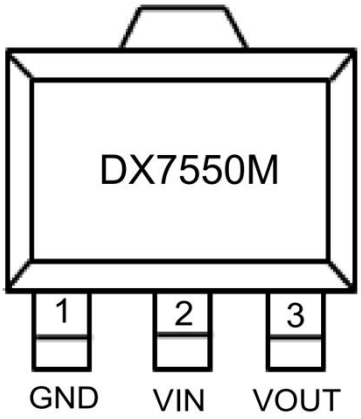
Features

- ◆ Low Power Consumption: 2.5μA (Typ)
- ◆ Maximum Output Current: 150mA
- ◆ Operating Voltage Range: 5.5~24V
- ◆ Output Voltage Accurate: ±2%
- ◆ Good Transient Response
- ◆ Integrated Short-Circuit Protection
- ◆ Over-Temperature Protection

Output Current Limit

- ◆ Low Temperature Coefficient
- ◆ Stable with Ceramic Capacitor
- ◆ RoHS Compliant and Lead (Pb) Free
- ◆ -40℃ to +85℃ Operating Temperature Range
- ◆Fixed Output Voltage Versions: 5.0V
- ◆ Available in Green SOT89-3 Packages

Pin Configuration



Application Circuits

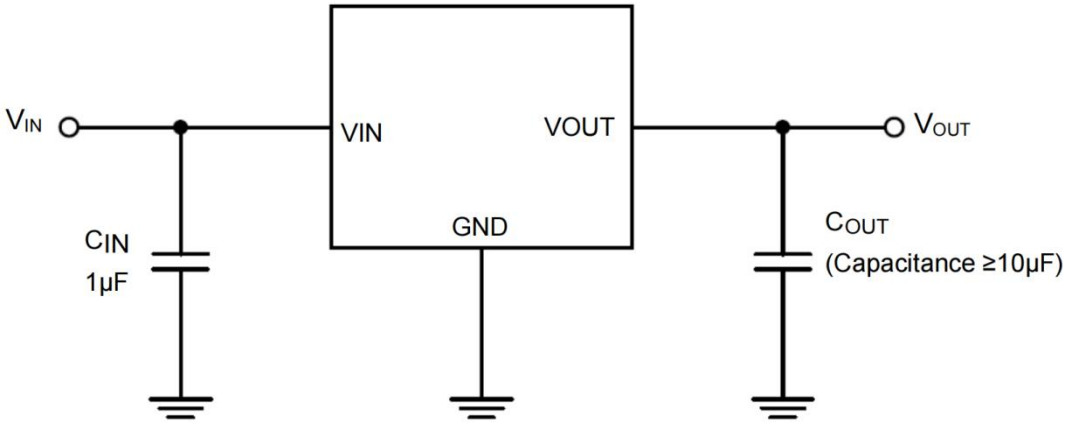


Figure 1. DX7550M Typical Application Circuit

Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground
2	VIN	Power Input
3	VOUT	Output Voltage

Order Information

Part NO.	Package	T/R Qty
DX7550M	SOT89-3	1,000 PCS/4,000 PCS

Marking Information

For marking information, contact our sales representative directly

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Input Voltage	V_{IN}	-0.3 ~ 30	V
Regulated Output Voltage	V_{OUT}	5.0	V
Output Current	I_{OUT}	Internally limited	mA
Power Dissipation PD @TA=+25℃	P_D	700	mW
Thermal Resistance (Junction to air)	θ_{JA}	180	°C /W
Human Body Model (HBM)	±2000		V
Charged Device Mode (CDM)	±1000		V
Machine Mode (MM)	200		V
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Operating Junction Temperature	T_J	+150	°C
Lead Temperature (Soldering 10s)	T_{LEAD}	+260	°C

Note：

1、Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.

2、 Ratings apply to ambient temperature at +25°C

3、The package thermal impedance is calculated in accordance to JESD 51-7.

Recommended Operating Conditions

Item	Min	Max	Unit
Operating Ambient Temperature	-40	+85	°C
Input voltage	5.5	24	V
Output Voltage	4.9	5.1	V

Electronic Characteristics

Test Conditions:VIN=VOUT+1V,CIN=COUT=1uF,TA=25℃, unless otherwise specifi

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		5.5	--	24	V
Quiescent Current	I_Q	V_{IN} =12V, I_{LOAD} =0mA	--	2.5	3.0	μA
Output Voltage	V_{OUT}	V_{IN} =12V, I_{LOAD} =10mA	4.9	5.0	5.1	V
Output Current	I_{OUT}	V_{IN} = V_{OUT} +2V	--	150	--	mA
Dropout Voltage V_{OUT} =5.0V	V_{DROP}	I_{LOAD} =100mA	--	450	--	mV
		I_{LOAD} =150mA	--	700	--	
Line Regulation	Δ V_{LINE}	I_{LOAD} =1mA V_{OUT} +2.0v ≦V_{IN} ≦24V	--	0.15	--	% / V
Load Regulation	Δ V_{LOAD}	V_{IN} = V_{OUT} +2V 1mA≦I_{LOAD} ≦100mA	--	--	20	mV
Short Current	I_{SHORT}	V_{OUT} = GND	--	80	--	mA
Thermal Shutdown Temperature	T_{SHDN}		--	160	--	℃
Thermal Shutdown Hysteresis	ΔT_{SHD}		--	20	--	℃

Note : All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Functional Block Diagram

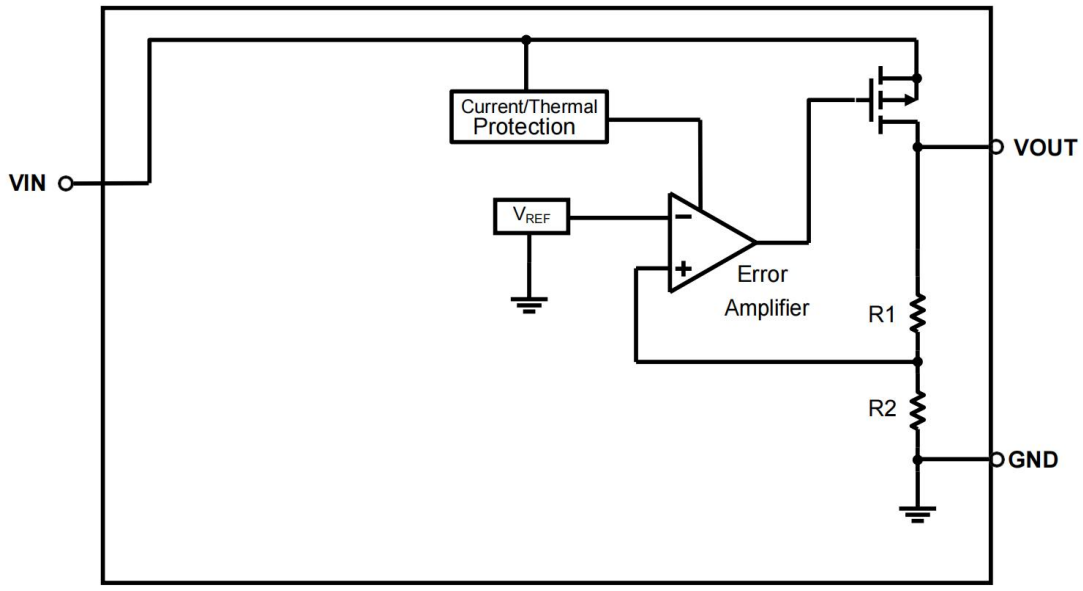


Figure 2. DX7550M Block Diagram

Application Guideline

◆ Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

◆ Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

◆ Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass-FET at specific output current (IRATED) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as (VDROP = VIN − VOUT = RDS(ON) x IRATED). Fornormal operation, the suggested LDO operating range is (VIN > VOUT + VDROP) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

◆ Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: TA=25°C, AISIS DEMO PCB, The max PD= (Tj − TA) / θJA.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

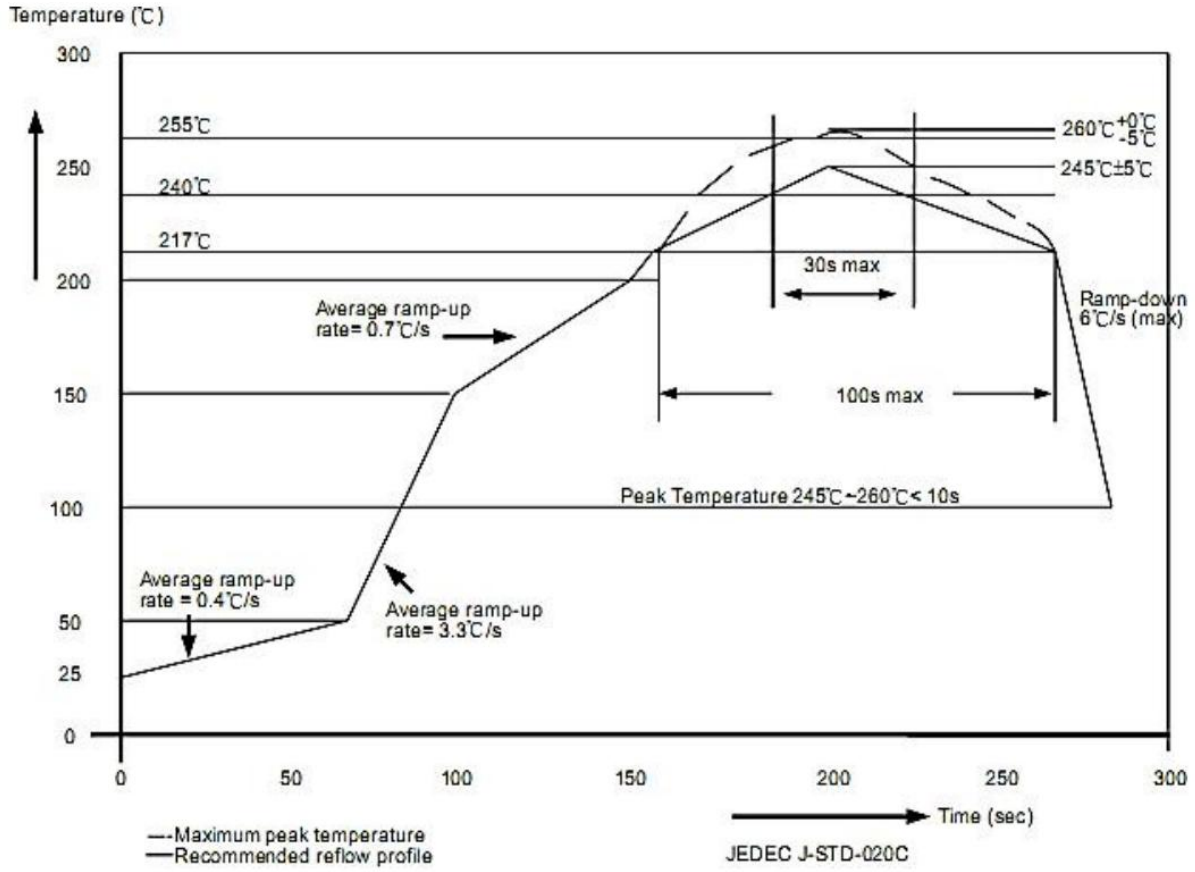
$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$$

◆ Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DX7550M ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

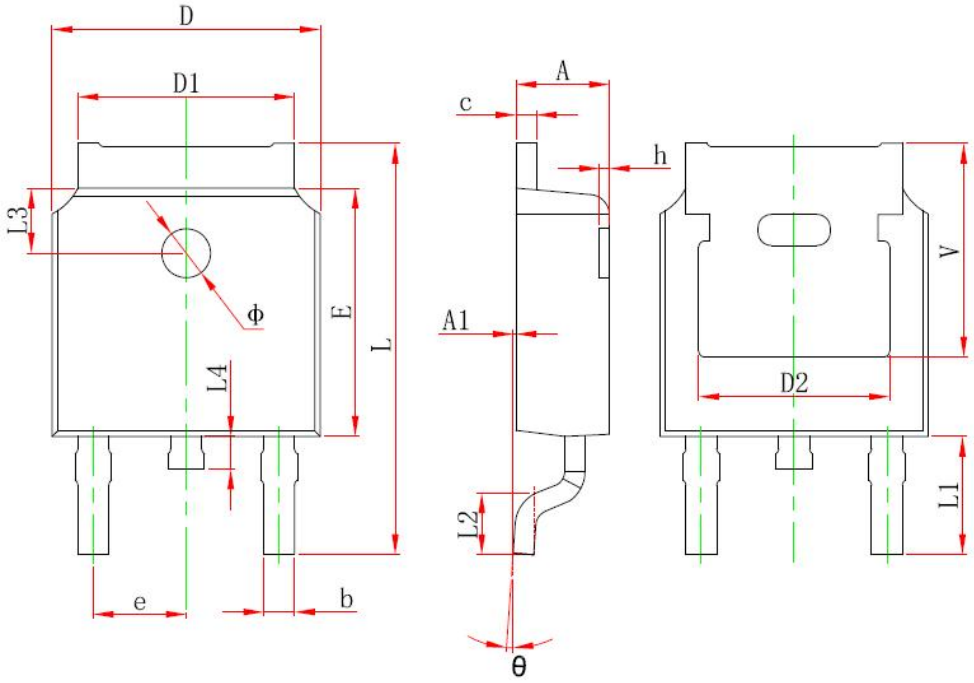
Packaging and welding process

The semiconductor products produced by Dersem Microelectronics follow the European RoHs standard, and the temperature of tin furnace in the packaging and welding process meets the J-STD-020 standard.



Package thickness	Volume mm3 < 350	Volume mm3：350~2000	Volume mm3 ≥ 2000
<1.6mm	260+0°C	260+0°C	260+0°C
1.6mm~2.5mm	260+0°C	250+0°C	245+0°C
≥2.5mm	250+0°C	245+0°C	245+0°C

PACKAGE OUTLINE DRAWING FOR SOT89-3



Symbol	Min(mm)	Max(mm)
A	2.0	2.7
A1	-	0.2
b	0.5	1.1
c	0.3	0.8
D	6.3	6.9
D1	4.9	5.7
D2	4.83(REF)	
E	5.9	6.4
e	2.086	2.486
L	9.5	10.7
L1	2.9(REF)	
L2	1.2	1.9
L3	1.6(REF)	
L4	0.4	1.2
Φ	0.9	1.5
θ	0°	10°
h	-	0.5
V	5.35(REF)	

Declaration of Usage Rights

Shenzhen Dersem Microelectronics reserves the right to make all changes, revisions, modifications, improvements, and terminations to its products, documents, and services. Regarding the aforementioned rights, customers are advised to contact a representative from Dexin Microelectronics before making a product purchase to obtain the latest product information.

Unless authorized by Dersem, the products of Dersem should not be used for medical or military purposes. If the user causes any bodily injury, threat to life, or even death as a result, Dersem will not be liable for any damages.

All text, images, and trademarks on this document belong to Dersem Microelectronics. Without the legitimate authorization of Dersem, no individual or organization may use, modify, reproduce, publicly disclose, adapt, disseminate, issue, publicly publish, or damage the legitimate rights and interests of this enterprise. For related infringement behaviors, our company will immediately initiate comprehensive legal proceedings and pursue legal responsibilities.