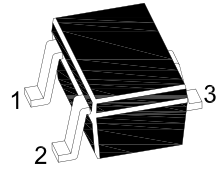
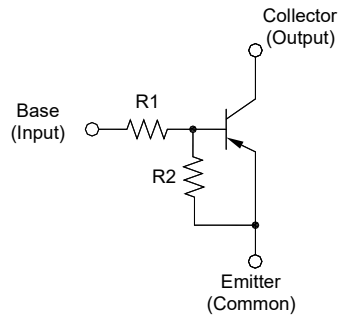


MMDTA114YE

PNP Silicon Epitaxial Planar Digital Transistor

Features

- With built-in bias resistors
- Simplify circuit design
- Reduce a quantity of parts and manufacturing process
- Halogen and Antimony Free(HAF), RoHS compliant



1.Base 2.Emitter 3.Collector
SOT-523 Plastic Package

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Collector Base Voltage	$-V_{CBO}$	50	V
Collector Emitter Voltage	$-V_{CEO}$	50	V
Input Voltage	V_{IN}	- 40 to + 6	V
Collector Current	$-I_C$	100	mA
Total Power Dissipation ¹⁾	P_{tot}	150	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient ¹⁾	$R_{\theta JA}$	833	$^\circ\text{C/W}$

¹⁾ Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

Characteristics at $T_a = 25\text{ }^{\circ}\text{C}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at $-V_{CE} = 5\text{ V}$, $-I_C = 5\text{ mA}$	h_{FE}	68	-	-	-
Collector Base Cutoff Current at $-V_{CB} = 50\text{ V}$	$-I_{CBO}$	-	-	0.5	μA
Emitter Base Cutoff Current at $-V_{EB} = 5\text{ V}$	$-I_{EBO}$	-	-	0.88	mA
Collector Base Breakdown Voltage at $-I_C = 10\text{ }\mu\text{A}$	$-V_{(BR)CBO}$	50	-	-	V
Collector Emitter Breakdown Voltage at $-I_C = 1\text{ mA}$	$-V_{(BR)CEO}$	50	-	-	V
Collector Emitter Saturation Voltage at $-I_C = 5\text{ mA}$, $-I_B = 0.25\text{ mA}$	$-V_{CE(sat)}$	-	-	0.3	V
Input off Voltage at $-V_{CE} = 5\text{ V}$, $-I_C = 100\text{ }\mu\text{A}$	$-V_{I(off)}$	0.3	-	-	V
Input on Voltage at $-V_{CE} = 0.3\text{ V}$, $-I_C = 1\text{ mA}$	$-V_{I(on)}$	-	-	1.4	V
Transition Frequency at $-V_{CE} = 10\text{ V}$, $I_E = 5\text{ mA}$, $f = 100\text{ MHz}$	f_T	-	250	-	MHz
Input Resistance	R_1	7	10	13	$\text{K}\Omega$
Resistance Ratio	R_2 / R_1	3.7	4.7	5.7	-

Electrical Characteristics Curves

Fig 1. Output Characteristics

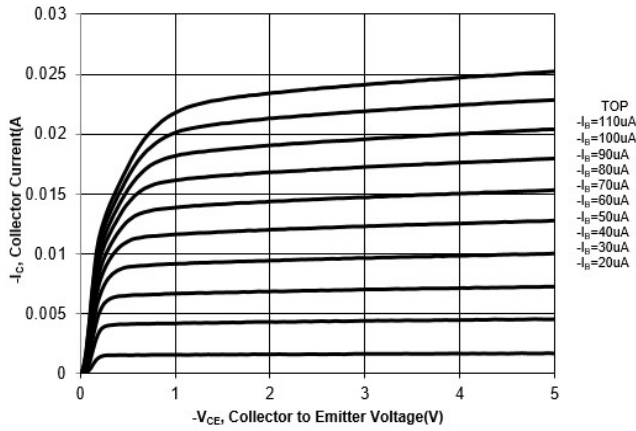


Fig. 2. Collector Current vs. Input On Voltage

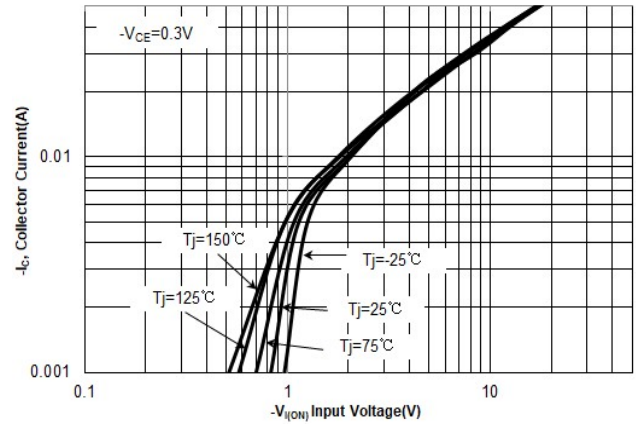


Fig. 3. Collector Current vs. Input Off Voltage

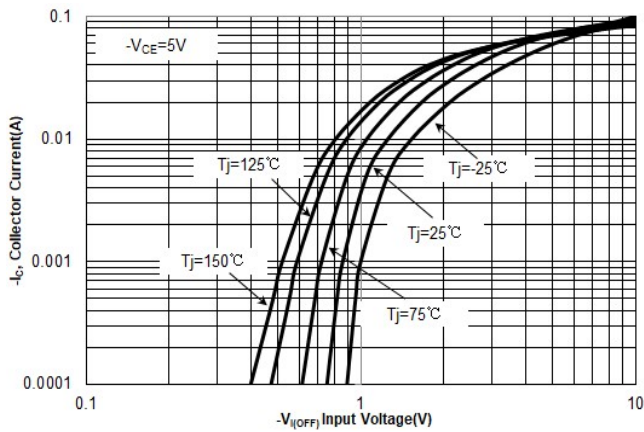


Fig. 4. DC Current Gain vs. Collector Current

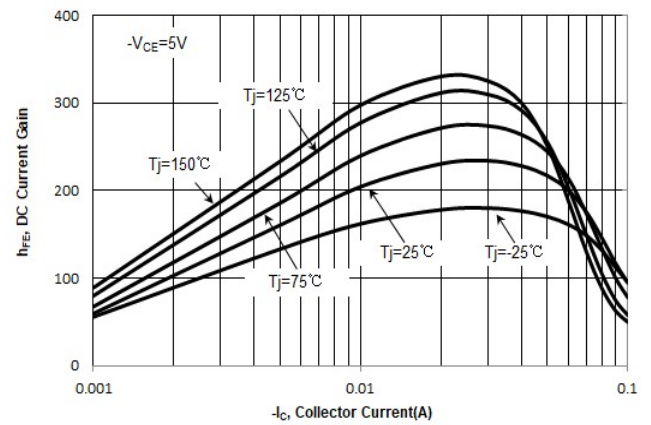


Fig. 5. $V_{CE(SAT)}$ vs. Collector Current

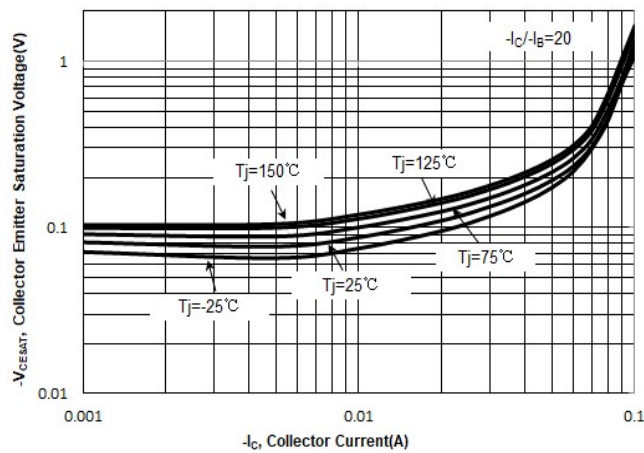
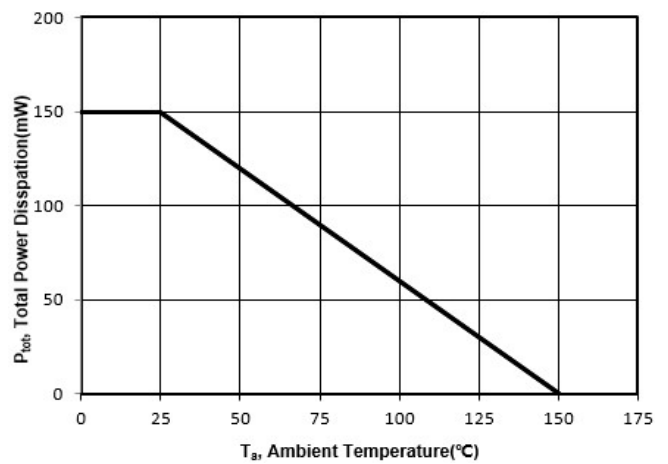
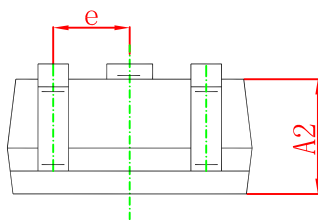
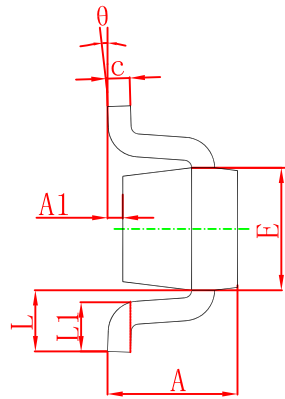
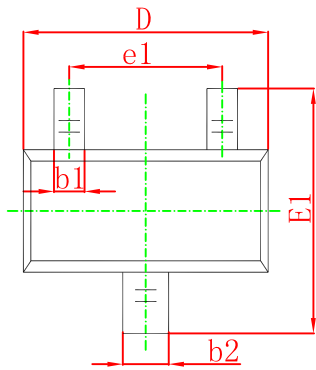


Fig. 6. Power Derating Curve



SOT-523 PACKAGE OUTLINE Plastic surface mounted package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.950	0.026	0.037
A1	0.000	0.100	0.000	0.004
A2	0.650	0.850	0.026	0.033
b1	0.150	0.250	0.006	0.010
b2	0.250	0.350	0.010	0.014
c	0.050	0.200	0.002	0.008
D	1.500	1.700	0.059	0.067
E	0.700	0.900	0.028	0.035
E1	1.450	1.750	0.057	0.069
e	0.500 TYP.		0.020 TYP.	
e1	0.900	1.100	0.035	0.043
L	0.400 REF.		0.016 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°