1. DESCRIPTION

The XLA1051 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The XLA1051 belongs to the third generation of high-speed CAN transceivers, offering significant improvements over first- and second-generation devices such It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off

The XLA1051 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the XLA1051 an excellent choice for all types of HS-CAN networks, in nodes that do not require a standby mode with wake-up capability via the bus.

2. FEATURES AND BENEFITS

2.1. General

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2. Low-power management

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

2.3. Protection

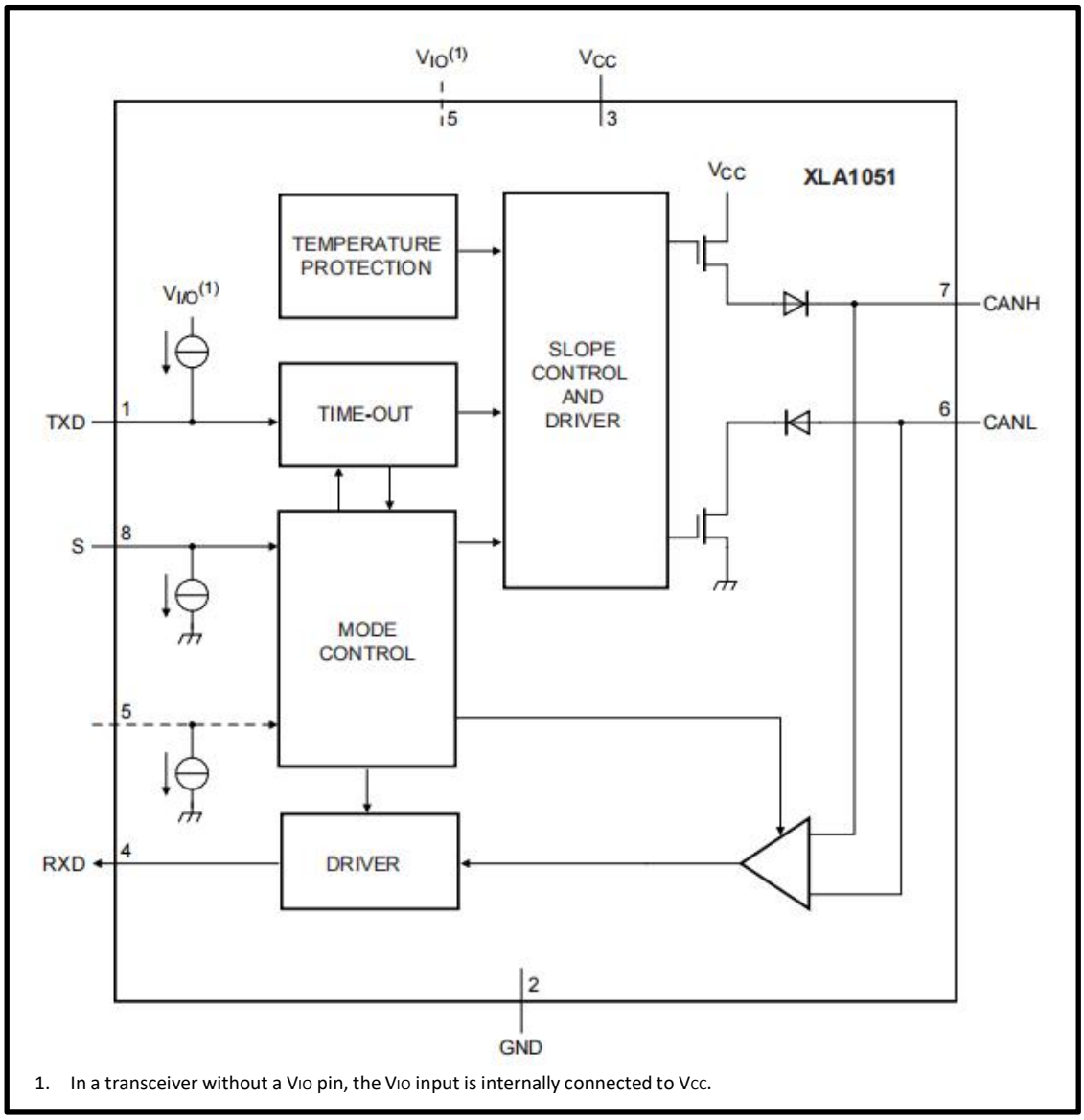
- High ElectroStatic Discharge (ESD) handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

3. QUICK REFERENCE DATA

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
I_{CC}	supply current	Silent mode	0.1	1	2.5	mA
		Normal mode; bus recessive	2.5	5	10	mA
		Normal mode; bus dominant	20	50	70	mA
I_{IO}	supply current on pin V_{IO}	Normal/Silent mode				
		recessive; $V_{TXD} = V_{IO}$	-	80	250	µA
		dominant; $V_{TXD} = 0$ V	-	350	500	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH		-58	-	+58	V
V_{CANL}	voltage on pin CANL		-58	-	+58	V
T_{vj}	virtual junction temperature		-40	-	+125	°C

4. BLOCK DIAGRAM



1. In a transceiver without a VIO pin, the VIO input is internally connected to VCC.

Fig 1. Block diagram

5. PINNING INFORMATION

5.1. Pinning

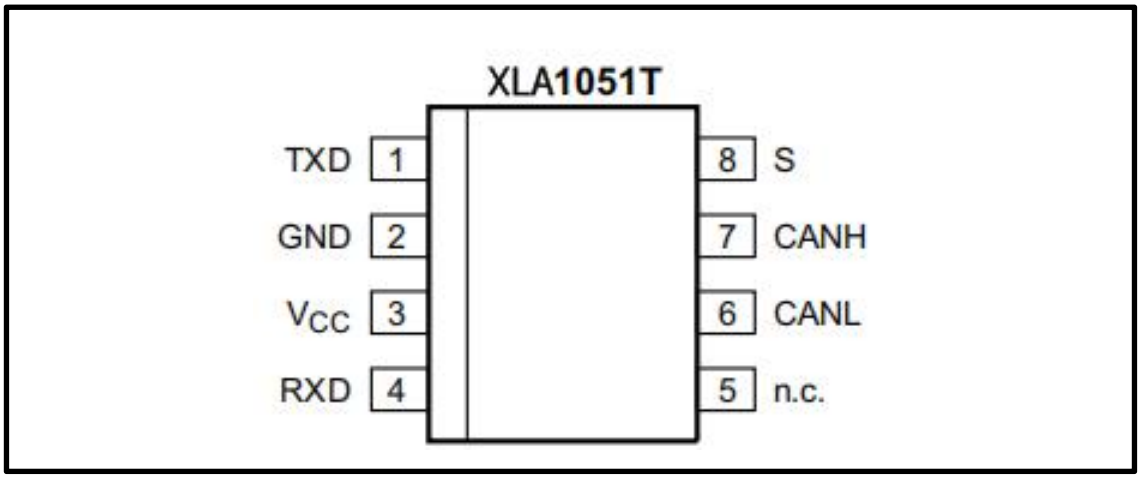


Fig 2. Pin configuration diagrams

5.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2	ground
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
n.c.	5	not connected; in XLA1051T version
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
S	8	Standby mode control input

6. FUNCTIONAL DESCRIPTION

The XLA1051 is a high-speed CAN stand-alone transceiver with Silent mode. It combines the functionality of the transceiver with improved EMC and ESD handling capability. Improved slope control and high DC handling capability on the bus pins provides additional application flexibility.

6.1. Operating modes

The XLA1051 supports two operating modes, Normal and Silent, which are selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Inputs			Outputs	
	Pin EN	PIN S	PIN TXD	CAN driver	PIN RXD
Normal	HIGH	LOW	LOW	dominant	active[1]
	HIGH	LOW	HIGH	recessive	active[1]
Silent	HIGH	HIGH	X[2]	recessive	active[1]
Off	LOW	X[2]	X[2]	floating	floating

[1] LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.
[2] 'X' = don't care.

6.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver is able to transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible ElectroMagnetic Emission (EME).

6.1.2 Silent mode

A HIGH level on pin S selects Silent mode. In Silent mode the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

6.2. Fail-sate features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 20 kbit/s.

6.2.2 Internal biasing of TXD, S and EN input pins

Pin TXD has an internal pull-up to V_{IO} and pins S have internal pull-downs to GND. This ensures a safe, defined state in case one or more of these pins is left floating.

6.2.3 Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} or V_{IO} drop below their respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd\ (VIO)}$; see Table 7), the transceiver will switch off and disengage from the bus (zero load) until V_{CC} and V_{IO} have recovered.

6.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature falls below Tj(sd) and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

7. LIMITING VALUES

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND

Symbol	Parameter	Conditions	Min	Max	Unit
V_X	voltage on pin x[1]	on pins CANH, CANL	-58	+58	V
		on any other pin	-0.3	+7	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-27	+27	V
V_{trt}	transient voltage	on pins CANH and CANL [2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330Ω) [3]			
		at pins CANH and CANL	-8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ [4]			
		at pins CANH and CANL	-8	+8	kV
		at any other pin	-4	+4	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10Ω [5]			
		on any pin	-300	+300	kV
		Charged Device Model (CDM); field Induced charge; 4 pF [6]			
		at corner pins	-750	+750	V
		at any pin	-500	+500	V
T_{vj}	virtual junction temperature	[7]	-40	+150	°C
T_{stg}	storage temperature		-55	+150	°C

Note:

(1) The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

(2) According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

(3) According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

(4) In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: Tvj = Tamb + P × Rth(vj-a), where Rth(vj-a) is a fixed value to be used for the calculation of Tvj. The rating for Tvj limits the allowable combinations of power dissipation (P) and ambient temperature (Tamb).

8. THERMAL CHARACTERISTICS

Table 6. Thermal characteristics

According to IEC 60747-1

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	155	K/W

9. STATIC CHARACTERISTICS

Table 7. Static characteristics

Tvj = -40 °C to +125°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Silent mode	0.1	1	2.5	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	-	5	10	mA
		dominant; V_{TXD} = 0 V	-	50	70	mA
		dominant; lines; V_{TXD} = 0 V; short circuit on bus -3 V < ($V_{CANH} = V_{CANL}$) < +18 V	2.5	80	110	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
I/O level adapter supply; pin V_{IO} [1]						
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.5	V
I_{IO}	supply current on pin V_{IO}	Normal mode				
		recessive; $V_{TXD} = V_{IO}$	-	80	250	µA
		dominant; V_{TXD} = 0 V	-	350	500	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
Mode control inputs; pins S and EN						
V_{IH}	HIGH-level input voltage	[3]	0.7V_{IO}	-	V_{IO}+0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.3V_{IO}	V
I_{IH}	HIGH-level input current	$V_S = V_{IO}$; $V_{EN} = V_{IO}$	1	4	10	µA
I_{IL}	LOW-level input current	V_S = 0 V; V_{EN} = 0 V	-1	0	+1	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage	[3]	0.7V_{IO}	-	V_{IO}+0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	+0.3V_{IO}	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}$	-5	0	+5	µA
I_{IL}	LOW-level input current	Normal mode; V_{TXD} =0V	-260	-150	-30	µA
C_i	input capacitance	[4]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ - 0.4 V	-8	-3	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CAN						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; [4] f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz [5] V_{CC} = 4.75 V to 5.25 V; C_{SPLIT} = 4.7 nF	0.9V_{CC}	-	1.1V_{CC}	V
$V_{O(dif)}$	differential output voltag	dominant: Normal mode; V_{TXD} = 0 V; t<$t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; no load				
		Normal mode: $V_{TXD} = V_{IO}$	-50	-	+50	mV
$V_{O(rec)}$	ecessive output voltage	Normal/Silent mode; $V_{TXD} = V_{IO}$; no load	2	0.5 V_{CC}	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal/Silent mode; -30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V	0.5	0.7	0.9	V
$V_{rec(RX)}$	receiver recessive voltage	Normal/Silent mode; -30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V	-4	-	0.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dom(RX)}$	receiver dominant voltage	Normal/Silent mode; -30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V	0.9	-	9.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal mode; -30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V	50	120	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -15 V to +40 V	-100	-70	-40	mA
		pin CANL; V_{CANL} = -15 V to +40 V	40	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal/Silent mode; V_{TXD} = V_{IO}; V_{CANH} = V_{CANL} = -27 V to +32 V	-5	-	+5	mA
I_L	leakage current	V_{CC} = V_{IO} = 0 V or V_{CC} = V_{IO} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} =5V	-5	-	+5	µA
R_i	nput resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V [4]	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V [4]	-1	-	+1	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V [4]	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[4]	-	-	20	pF
	differential input capacitance	[4]	-	-	10	
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[4]	-	190	-	°C

NOTE:
(1) In transceivers without a VIO pin, the VIO input is internally connected to VCC.
(2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
(3) Maximum value assumes VCC < VIO; if VCC > VIO, the maximum value will be VCC + 0.3 V.
(4) Not tested in production; guaranteed by design.
(5) The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in Figure 6.

10. DYNAMIC CHARACTERISTICS

Table 8. Dynamic characteristics

Tvj =-40°C; to +125°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; RL = 60Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	65	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	60	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	65	-	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode: versions with V_{IO} pin	40	-	250	ns
		Normal mode: other versions	40	-	220	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode: versions with V_{IO} pin	40	-	250	ns
		Normal mode: other versions	40	-	220	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns [3]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [3]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [3]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [3]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [4]	0.3	1	5	ms

(1) In transceivers without a VIO pin, the VIO input is internally connected to VCC.
(2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
(3) See Figure 4.
(4) Minimum value of 0.8ms required according to SAE J2284; 0.3ms is allowed according to ISO11898-2:2016 for legacy devices.

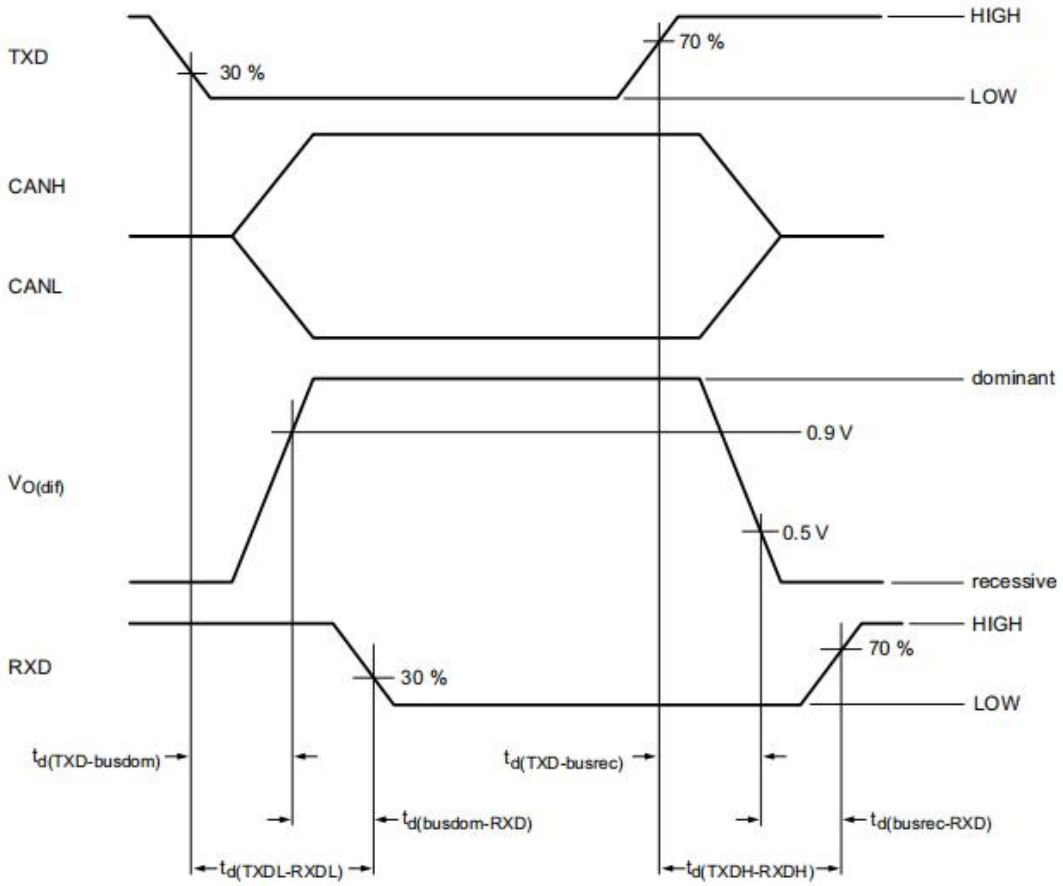


Fig 3. CAN transceiver timing diagram

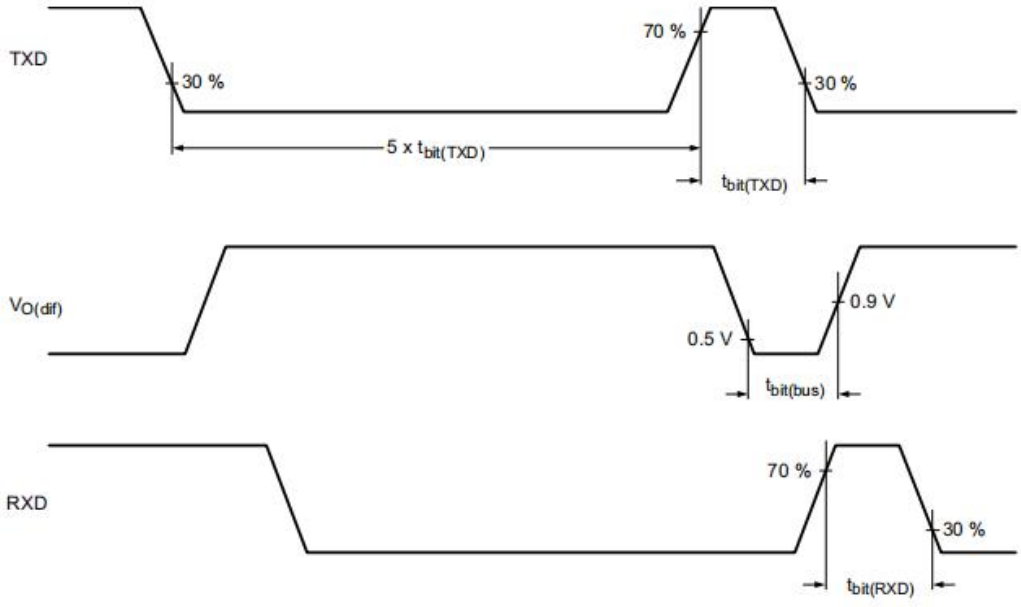


Fig 4. CAN FD timing definitions according to ISO 11898-2:2016

11. TEST INFORMATION

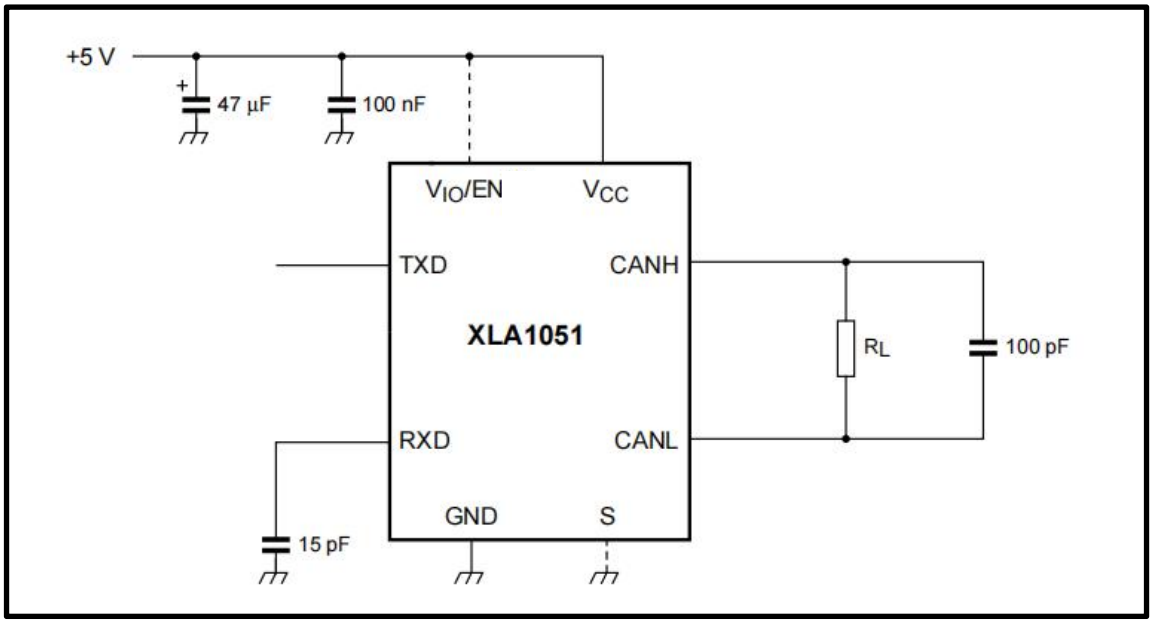


Fig 5. Timing test circuit for CAN transceiver

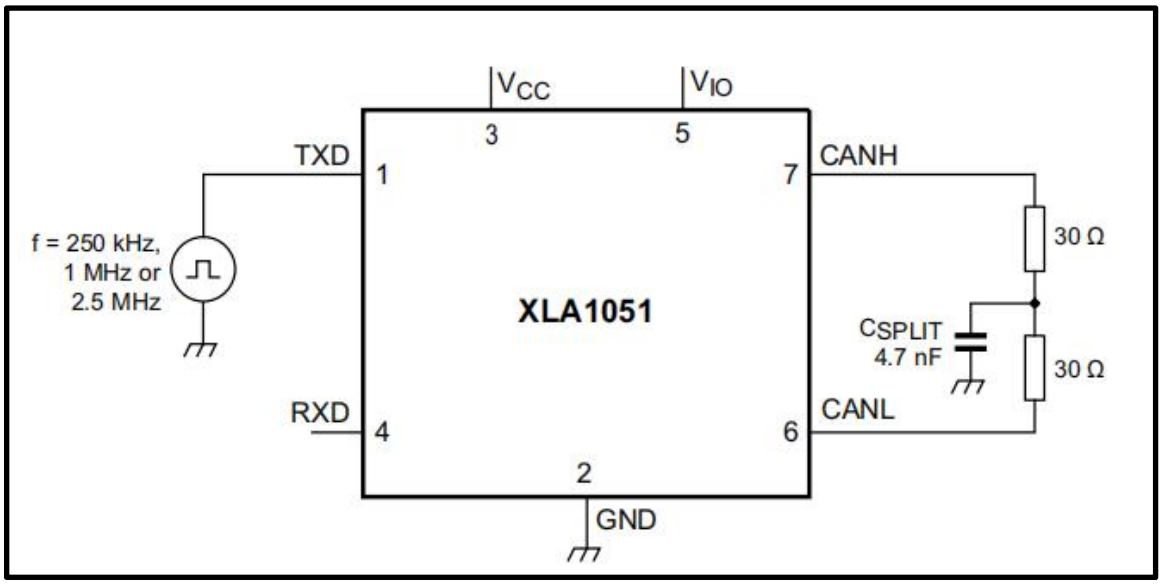


Fig 6. Test circuit for measuring transceiver driver symmetry

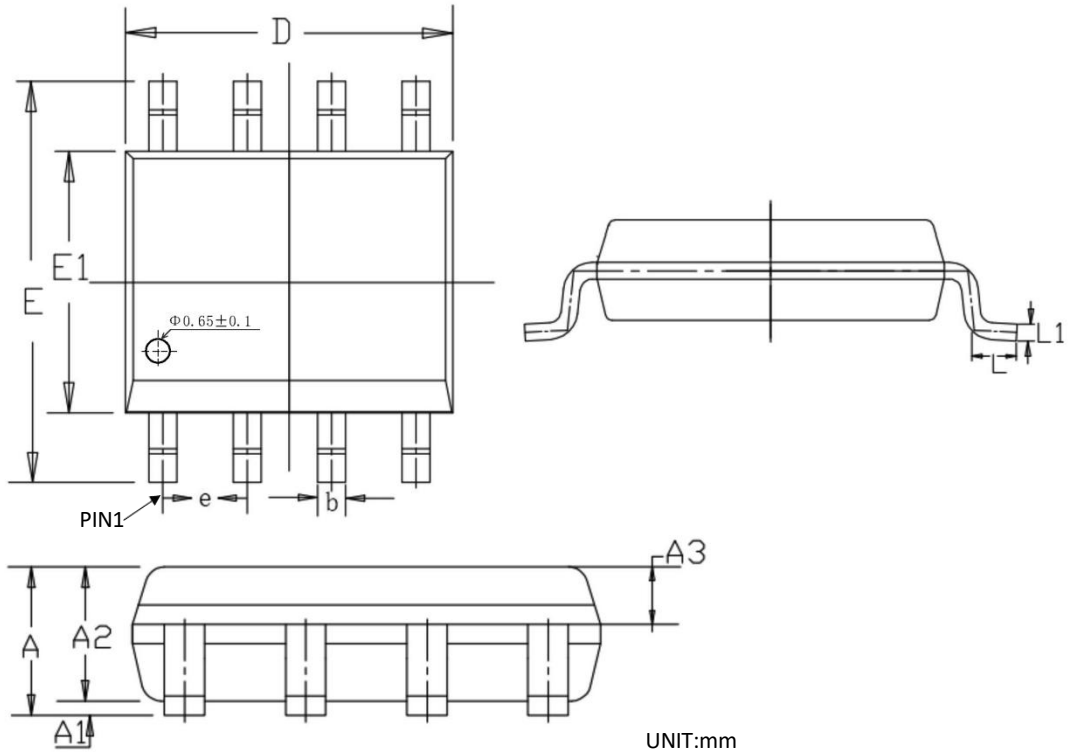
12. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XLA1051T/1	XL1051T1	SOP-8	4.90*3.90	-40 to +125	MSL3	T&R	2500

13. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—