1. DESCRIPTION

The XLA1042 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The XLA1042 belongs to the third generation of high-speed CAN transceivers , Significant improvements have been made. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

• Ideal passive behavior to the CAN bus when the supply voltage is off

• A very low-current Standby mode with bus wake-up capability

• Variants with a VIO pin can be interfaced directly with microcontrollers with supply voltages from 3.3 V to 5 V

The XLA1042 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

2. FEATURES AND BENEFITS

2.1. General

- Fully ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V and 24 V systems
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI), according to proposed EMC Standards IEC 62228-3 and SAE J2962-2
- Variants with a V_{IO} pin allow for direct interfacing with 3.3 V to 5 V microcontrollers
- SPLIT voltage output on XLA1042 for stabilizing the recessive bus level
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2. Predictable and fail-safe behavior

- Very low-current Standby mode with host and bus wake-up capability
- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops
- below the switch-off undervoltage threshold
- Transmit Data (TXD) dominant time-out function
- Bus-dominant time-out function in Standby mode
- Undervoltage detection on pins V_{CC} and V_{IO}

2.3. Protections

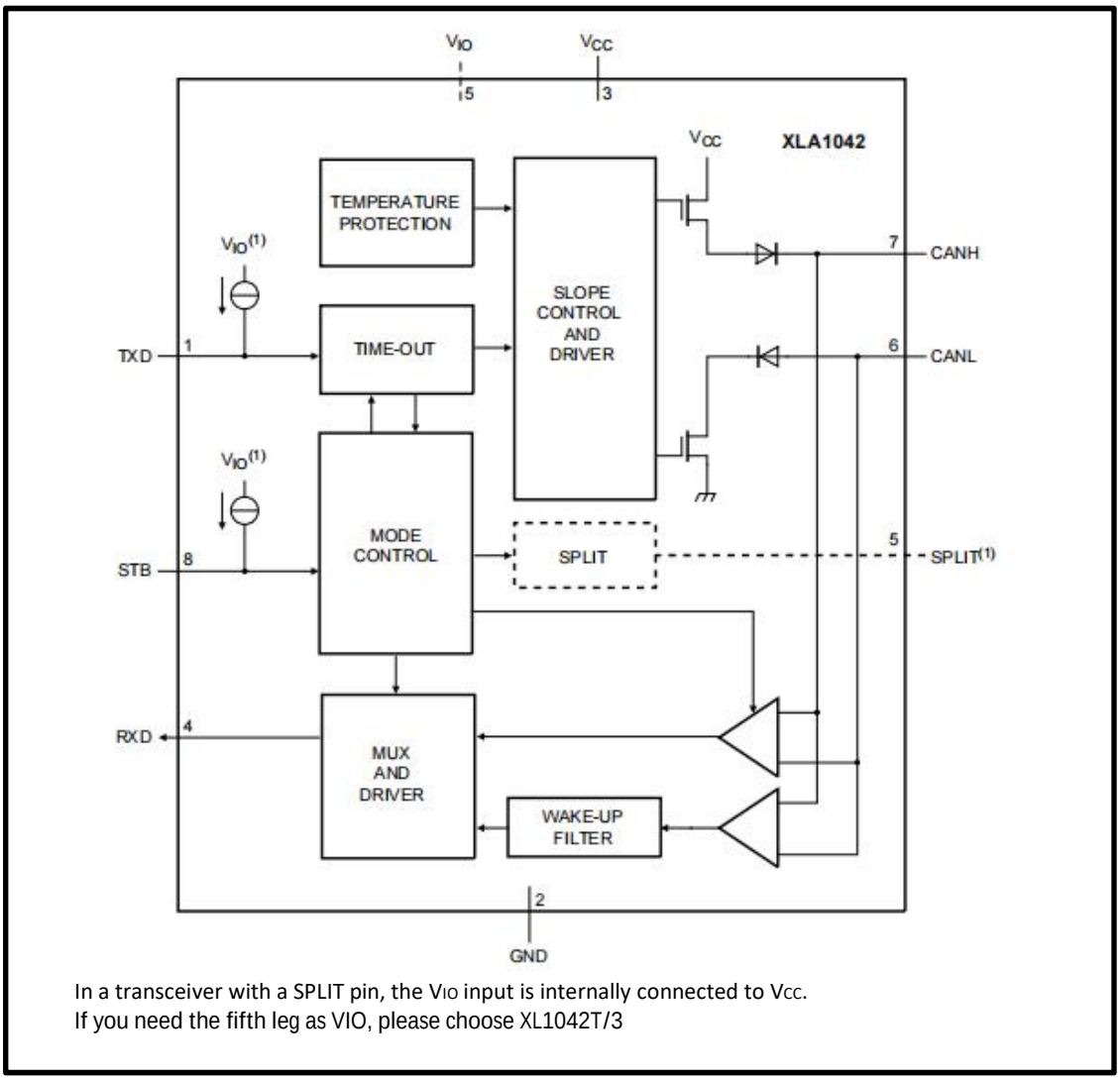
- High ESD handling capability on the bus pins (±8 kV)
- High voltage robustness on CAN pins (±58 V)
- Bus pins protected against transients in automotive environments
- Thermally protected

3. QUICK REFERENCE DATA

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5		5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.8		5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5		4.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
I_{CC}	supply current	Standby mode		10	15	µA
		Normal mode; bus recessive	2.5	5	10	mA
		Normal mode; bus dominant	20	45	70	mA
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	5		14	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	15	80	200	µA
		dominant; V_{TXD} = 0 V		350	1000	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	-8		+8	kV
V_{CANH}	voltage on pin CANH		-58		+58	V
V_{CANL}	voltage on pin CANL		-58		+58	V
T_{vj}	virtual junction temperature		-40		+150	°C

4. BLOCK DIAGRAM



In a transceiver with a SPLIT pin, the V_{IO} input is internally connected to V_{CC}.
If you need the fifth leg as VIO, please choose XL1042T/3

Figure 1. Block diagram

5. PINNING INFORMATION

5.1. Pinning

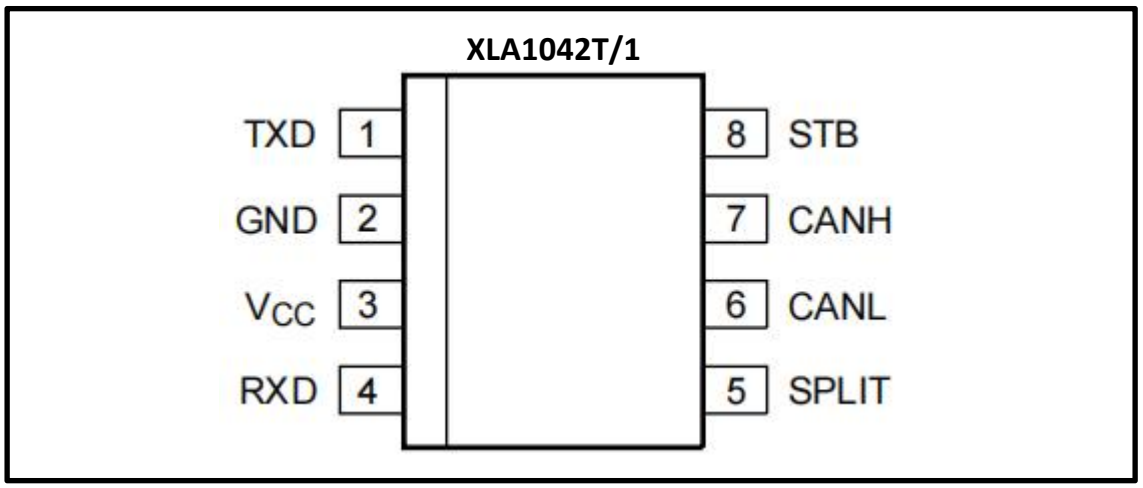


Figure 2. Pin configuration diagrams

5.2. Pin description

Table 3. Pin description

Symbol	Pin	Type(1)	Description
TXD	1	I	transmit data input
GND	2	G	ground supply
VCC	3	P	supply voltage
RXD	4	O	receive data output; reads out data from the bus lines
SPLIT	5	O	common-mode stabilization output
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
STB	8	I	Standby mode control input

(1) I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

6. FUNCTIONAL DESCRIPTION

6.1. Operating modes

The XLA1042 supports two operating modes, Normal and Standby, which are selected via pin STB. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Pin STB	Pin RXD	
		LOW	HIGH
Narmal	LOW	bus dominant	bus recessive
Stangdby	HIGH	wake-up request detected	no wake-up request detected

6.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normalmode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than tfltr(wake)bus are reflected on pin RXD.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

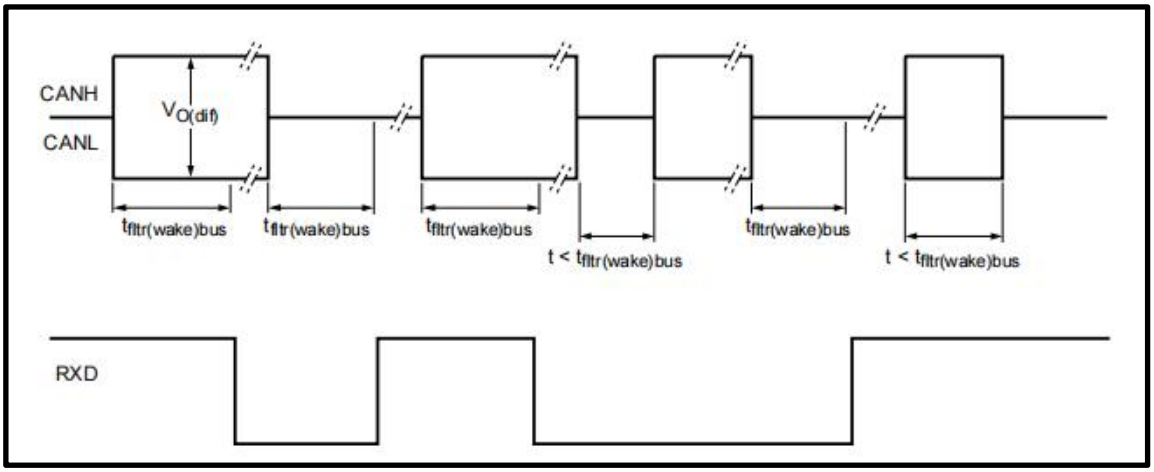


Figure 3. Wake-up timing

6.2. Fail-safe features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

6.2.2 Bus dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than tto(dom)bus, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

6.2.3 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

6.2.4 Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} drop below the V_{CC} undervoltage detection level, Vuvd(V_{CC}), the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered.

Should VIO drop below the V_{IO} undervoltage detection level, Vuvd(V_{IO}), the transceiver will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

6.2.5 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), the output drivers will be disabled until the virtual junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

6.3. SPLIT output pin and V_{IO} supply pin

Two versions of the XLA1042 are available, only differing in the function of a single pin. Pin 5 is either a SPLIT output pin or a VIO XL1042T/3 supply pin.

6.3.1 SPLIT pin

Using the SPLIT pin on the XLA1042 in conjunction with a split termination network (see Figure 4 and Figure 7) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of 0.5VCC. In Standby mode or when VCC is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

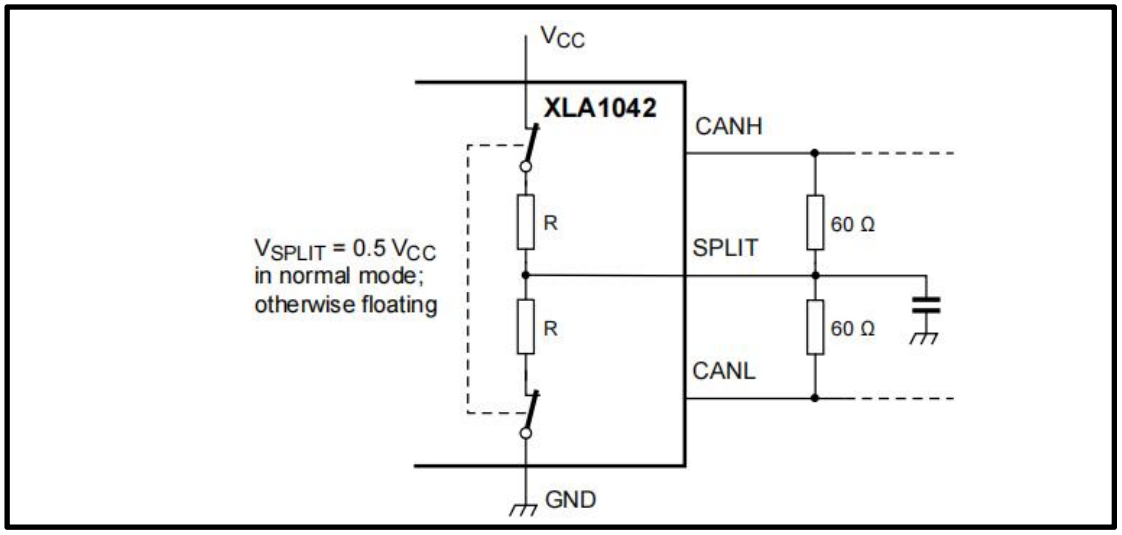


Figure 4. Stabilization circuitry and application for version with SPLIT pin

7. LIMITING VALUES

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to ground

Symbol	Parameter	Conditions	Min	Max	Unit
V_X	voltage on pin x[1]	on pins CANH, CANL and SPLIT	-58	+58	V
		on any other pin	-0.3	+7	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-27	+27	V
V_{trt}	transient voltage	on pins CANH, CANL [2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [3]			
		at pins CANH and CANL	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [4]	-4	+4	kV
		at pins CANH and CANL [5]	-8	+8	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [6]			
		at any pin	-300	+300	V
		Charged Device Model (CDM) [7]			
		at corner pins	-750	+750	V
		at any pin	-500	+500	V
T_{vj}	virtual junction temperature	[8]	-40	+125	°C
T_{stg}	storage temperature	[9]	-55	+150	°C

Note:

(1) The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

(2) Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

(3) Verified by an external test house according to IEC TS 62228, Section 4.3.

(4) Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 7 and Figure 8).

8. THERMAL CHARACTERISTICS

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	92	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SOP8 package; in free air	12	K/W

Note:(1) According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μ m)and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm)

9. STATIC CHARACTERISTICS

Table 7. Static characteristics

T_{vj} = -40 °C to +125°C; V_{CC} = 4.5 V to 5.5V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	[3]	3.8	-	4.5	V
I_{CC}	supply current	Standby mode				
		XLA1042; $V_{TXD} = V_{CC}$	-	10	15	μA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$ [4]	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	20	45	70	mA
		dominant; V_{TXD} = 0 V; short circuit on bus lines; -3 V < ($V_{CANH} = V_{CANL}$) < +18 V	2.5	80	110	mA
I/O level adapter supply; pin V_{IO} [1]						
V_{IO}	supply voltage on pin V_{IO}		2.5	-	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}	[3]	1.3	2.0	2.7	V
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	5	-	14	μA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	15	80	200	μA
		dominant; V_{TXD} = 0 V	-	350	1000	μA
Standby mode control input; pin STB						
V_{IH}	HIGH-level input voltage	[5]	0.7V_{IO}[4]	-	V_{IO} [4] + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.3VIO [4]	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{IO}$ [4]	-1	-	+1	μA
I_{IL}	LOW-level input current	V_{STB} = 0 V	-15	-	-1	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage	[5]	0.7V_{IO}[4]	-	V_{IO} [4] + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.3V_{IO} [4]	V
I_{HH}	HIGH-level input current	$V_{TXD} = V_{IO}$ [4]	-5	-	+5	μA
I_{LL}	LOW-level input current	V_{TXD} = 0 V	-260	-150	-30	μA
C_i	input capacitance	[6]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ - 0.4 V [4]	-9	-3	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	VTXD = 0 V; t < tto(dom)TXD				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = VCANH + VCANL; fTXD = 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF; V_{CC} = 4.75 V to 5.25 V [6] [7]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant: Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 45 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.5	-	3.3	V
		R_L = 2 240 Ω	1.5	-	5	V
		recessive; no load				
		Normal mode: V_{TXD} = V_{IO} [4]	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; V_{TXD} = V_{IO} [4]; no load	2	0.5Vcc	3	V
		Standby mode; no load	-0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	-30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V				
		Normal mode	0.5	0.7	0.9	V
		Standby mode [8]	0.4	0.7	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	-30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V [6]				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V
$V_{dom(RX)}$	receiver dominant voltage	-30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V [6]				
		Normal mode	0.9	-	9.0	V
		Standby mode	1.15	-	9.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	-30 V ≤ V_{CANL} ≤ +30 V; -30 V ≤ V_{CANH} ≤ +30 V	50	120	200	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -15 V to +40 V	-100	-70	-	mA
		pin CANL; V_{CANL} = -15 V to +40 V	-	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; V_{TXD} = V_{IO} [4] V_{CANH} = V_{CANL} = -27 V to +32 V	-5	-	+5	mA
I_L	leakage current	V_{CC} = V_{IO} = 0 V or V_{CC} = V_{IO} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	-5	-	+5	µA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V [6]	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V [6]	-1	-	+1	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V [6]	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[6]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[6]	-	-	10	pF
Common mode stabilization output; pin SPLIT; only for XLA1042						
V_O	output voltage	Normal mode I_{SPLIT} = -500 µA to +500µA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal mode; RL = 1 MΩ	$0.45V_{CC}$	$0.5V_{CC}$	0.55 V_{CC}	V
I_L	leakage current	Standby mode V_{SPLIT} = -58 V to +58 V	-5	-	+5	µA
$T_{j(sd)}$	shutdown junction temperature	[6]	-	190	-	°C

Note:

(1) For the XLA1042 variants, the V_{IO} input is internally connected to V_{CC}.
(2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
(3) Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
(4) V_{IO} = V_{CC} for the non-V_{IO} product variants.
(5) Maximum value assumes V_{CC} < V_{IO}; if V_{CC} > V_{IO}, the maximum value will be V_{CC} + 0.3 V.
(6) Not tested in production; guaranteed by design.
(7) The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in Figure 10.
(8) Variants with a a V_{IO} pin: values valid when -12 V ≤ V_{CANL} ≤ +12 V and -12 V ≤ V_{CANH} ≤ +12 V

10. DYNAMIC CHARACTERISTICS

Table 8. Dynamic characteristics

Tvj = -40 °C to +125°C; V_{CC} = 4.5 V to 5.5 V; VIO = 2.8 V to 5.5 V[1]; RL = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; seeFigure 5, Figure 6 and Figure 9						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	XLA1042	-	65	100	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	XLA1042	-	90	125	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	XLA1042	-	60	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	XLA1042	-	65	155	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	XLA1042; Normal mode	60	-	220	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	XLA1042; Normal mode	60	-	220	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns[3]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns[3]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns[3]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns[3]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode[4]	0.3	2	5	ms
$t_{to(dom)bus}$	bus dominant time-out time	Standby mode[5]	0.3	2	5	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	version with SPLIT pin; Standby mode	0.5	1	3	µs
		versions with VIO pin; Standby mode	0.5	1.5	5	µs
$t_{d(stb-norm)}$	standby to normal mode delay time		7	25	47	µs

Note:

(1) For the XLA1042 variants, the VIO input is internally connected to V_{CC}.

(2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

(3) See Figure 6.

(4) Minimum value of 0.8 ms required according to SAE J2284; 0.3 ms is allowed according to ISO11898-2:2016 for legacy devices. Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

(5) Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value

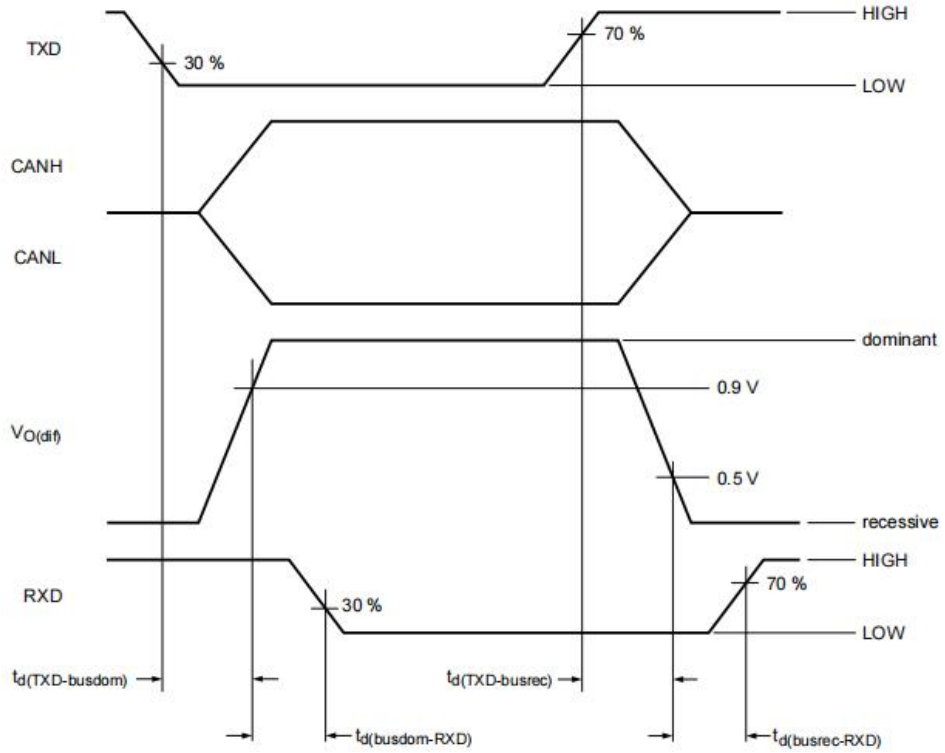


Figure 5. CAN transceiver timing diagram

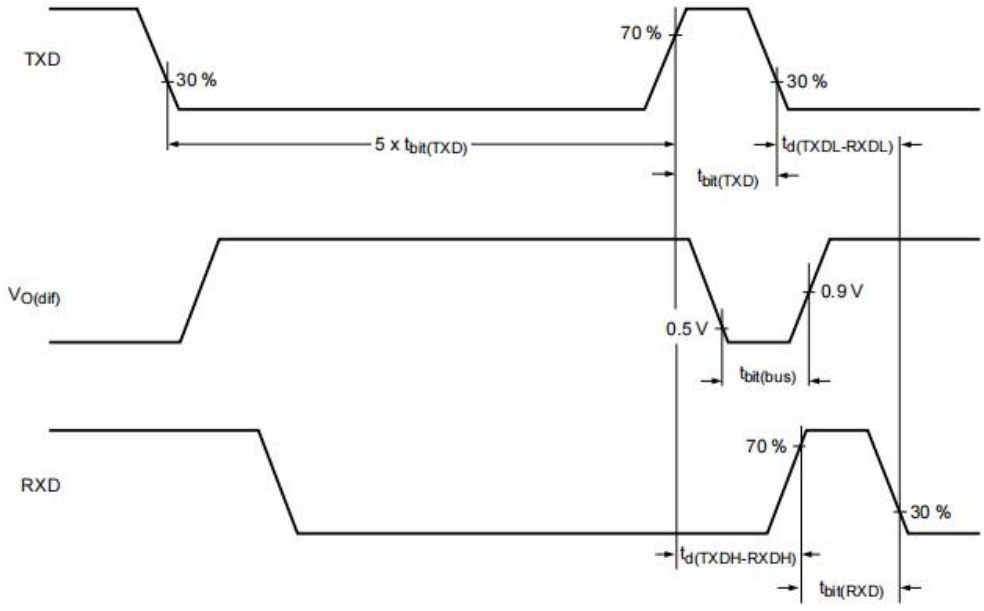
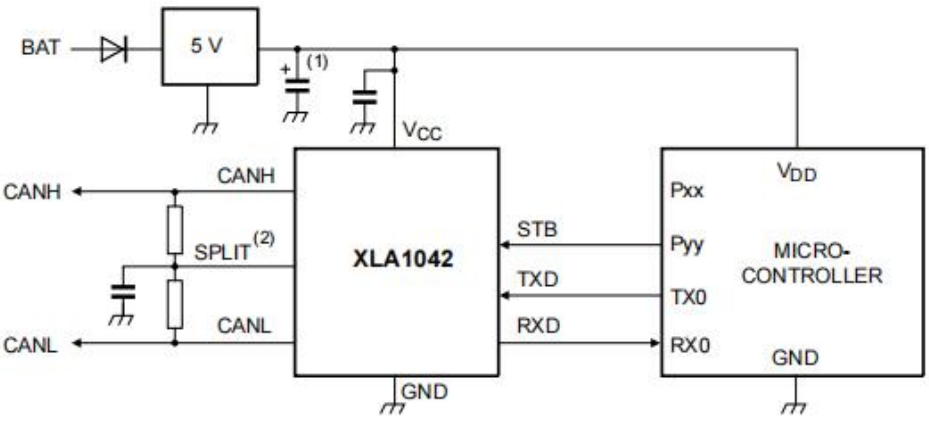


Figure 6. CAN FD timing definitions according to ISO 11898-2:2016

11. APPLICATION INFORMATION

The minimum external circuitry needed with the XLA1042 is shown in Figure 7.

11.1. Application diagrams



1. Optional, depends on regulator.
2. Optional common mode stabilization by a voltage source of $V_{CC}/2$ at pin SPLIT.

Figure 7. Typical XLA1042 application with a 5 V microcontroller (non-V_{IO} variants)

12. TEST INFORMATION

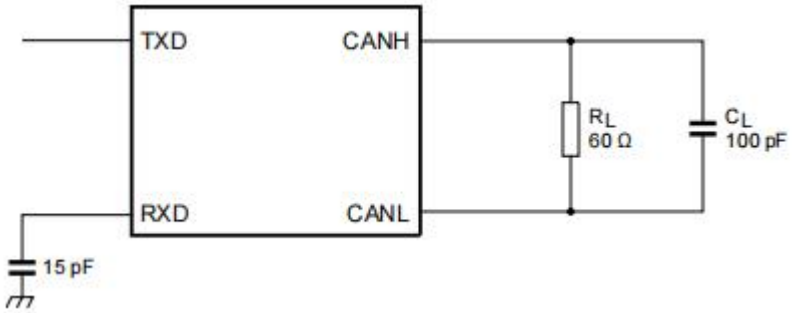


Figure 9. CAN transceiver timing test circuit

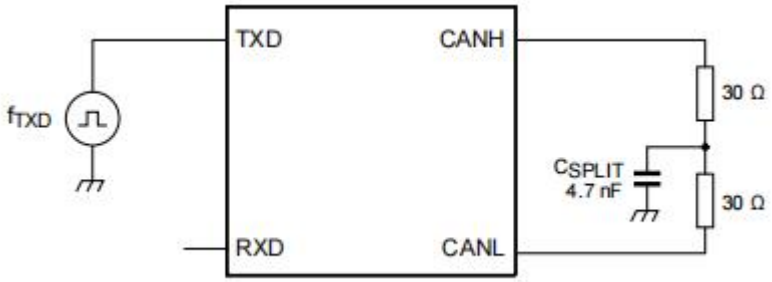


Figure 10. Test circuit for measuring transceiver driver symmetry

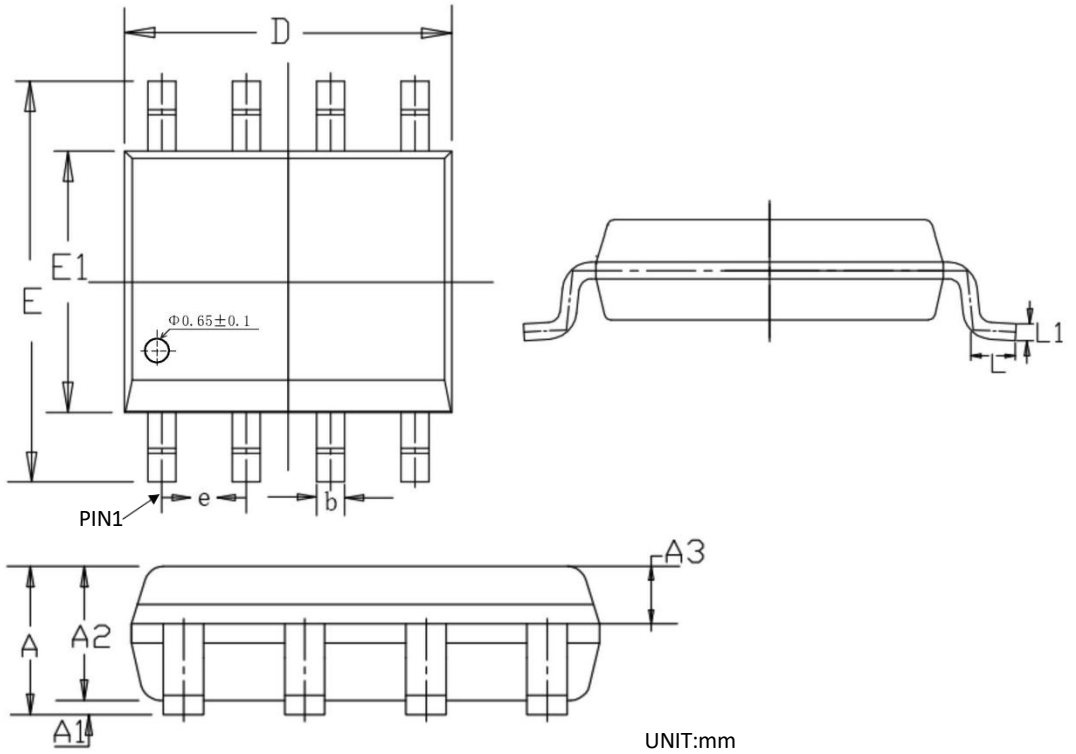
13. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XLA1042T/1	XL1042T1	SOP-8	4.90*3.90	-40 to +125	MSL3	T&R	2500

14. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—