1. DESCRIPTION

The XLA1057 is part of the Mantis family of high-speed CAN transceivers. It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus.The transceiver is designed for high-speed CAN applications in the automotive industry,providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The XLA1057 offers a feature set optimized for 12 V automotive applications, Significant improvements have been made. The XLA1057 also displays ideal passive behavior to the CAN bus when the supply voltage is off.

Variants with a V_{IO} pin can be interfaced directly with microcontrollers with supply voltages from 3.3 V to 5 V.

The XLA1057 implements the CAN physical layer as defined in ISO 11898-2:2024 third edition and SAE J2284-1 to SAE J2284-5. The XLA1057T is specified for data rates up to 1 Mbit/s. Additional timing parameters defining loop delay symmetry are specified for the other variants. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the XLA1057 an excellent choice for HS-CAN networks that only require basic CAN functionality.

2. FEATURES

2.1. General

- Fully ISO 11898-2:2024, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant[1]
- Optimized for use in 12 V automotive systems
- Low electromagnetic emission and high electromagnetic immunity, according to EMC standards IEC TS62228 and SAE J2962-2:2019[2]
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Variants with a V_{IO} pin allow for direct interfacing with 3.3 V to 5 V microcontrollers. Variants without a V_{IO} pin can interface with 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

2.2. Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the undervoltage threshold
- Transmit Data (TXD) dominant time-out function
- Internal biasing of TXD and S input pins

2.3. Protection

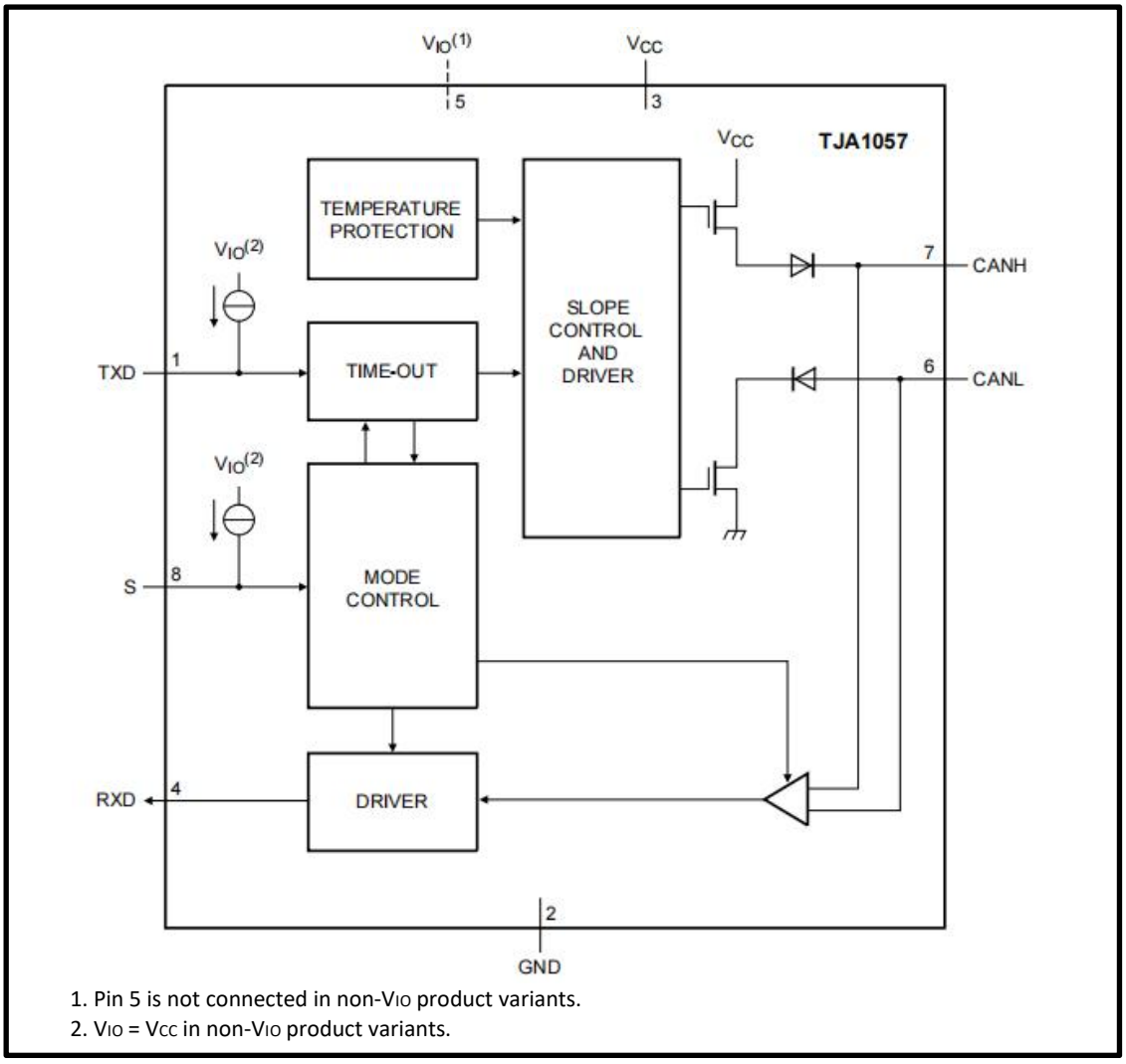
- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

3. QUICK REFERENCE DATA

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.91	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	4	4.3	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.1	-	2.8	V
I_{CC}	supply current	Standby mode	0.1	-	1.2	µA
		Normal mode; bus recessive	2	5	10	mA
		Normal mode; bus dominant	20	45	70	mA
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	-	3	16	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	-	7	30	µA
		dominant; $V_{TXD} = 0$ V	-	110	320	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC60134	-42	--	+42	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC60134	-42	-	+42	V
T_{vj}	virtual junction temperature		-40	-	-125	°C

4. BLOCK DIAGRAM



1. Pin 5 is not connected in non-V_{IO} product variants.
2. V_{IO} = V_{CC} in non-V_{IO} product variants.

Figure 1. Block diagram

5. PINNING INFORMATION

5.1. Pinning

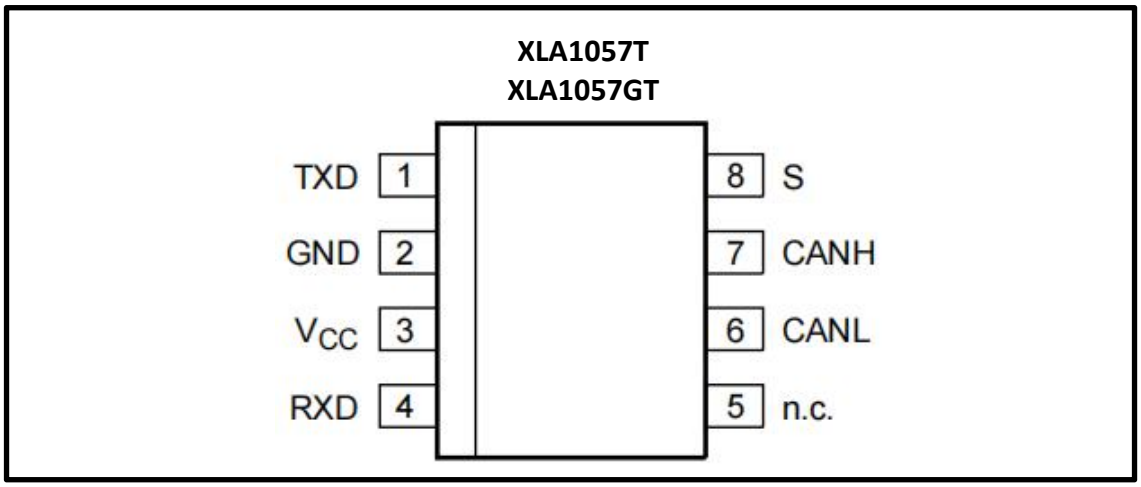


Figure 2. Pin configuration diagrams

5.2. Pin description

Table 3. Pin description

Symbol	Pin	Type[(1)]	Description
TXD	1	I	transmit data input
GND	2	G	ground
V_{CC}	3	P	supply voltage
RXD	4	O	receive data output; reads out data from the bus lines
n.c.	5	-	not connected in XLA1057T, XLA1057GT
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
STB	8	I	Silent mode control input

I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

6. FUNCTIONAL DESCRIPTION

6.1. Operating modes

The XLA1057 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	x [1]	biased to ground	LOW when bus dominant
				HIGH when bus recessive

Note:[1] 'x' = don't care

6.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines, CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.1.2 Silent mode

A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting all network communications.

6.2. Fail-safe features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

6.2.2 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to V_{CC} (or V_{IO} in variants with a V_{IO} pin) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Silent mode to minimize supply current.

6.2.3 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), both output drivers are disabled. When the virtual junction temperature drops below Tj(sd) again, the output drivers recover once TXD has been reset to HIGH (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature)

7. LIMITING VALUES

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_X	voltage on pin x[1]	on pins CANH, CANL	-42	+42	V
		on pin VCC, VIO	-0.3	+7	V
		on any other pin [2]	-0.3	V_{IO}[3]+ 0.3	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-27	+27	V
V_{trt}	transient voltage	on pins CANH and CANL [4]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [5]			
		on pins CANH and CANL	-8	+8	kV
		SAE J2962-2:2019 (330 pF, 2kΩ) on pins CANH, CANL			
		powered air discharge	-15	+15	kV
		powered contact discharge	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [6]	-4	+4	kV
		on pins CANH and CANL [7]	-4	+8	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω [8]			
		on any pin	-200	+200	V
		Charged Device Model (CDM) [9]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[10]	-40	+125	°C
T_{stg}	storage temperature	[11]	-55	+150	°C

Note:

(1) The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

(2) Maximum voltage should never exceed 7 V.

(3) V_{IO} + 0.3 = V_{CC} + 0.3 in the non-V_{IO} product variants.

(4) Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

(5) Verified by an external test house according to IEC TS 62228, Section 4.3.

(6) In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb})

(7) T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8. THERMAL CHARACTERISTICS

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	94	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SOP8 package; in free air	13	K/W

Note:(1) According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm)

9. STATIC CHARACTERISTICS

Table 7. Static characteristics

Tvj = -40 °C to +125°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	[3]	3.5	4	4.3	V
	supply current	Silent mode; VTXD = V_{IO} [4]	0.1	-	1.2	mA
		Normal mode				
		recessive; V_{TXD} = V_{IO} [4]	2	5	10	mA
		dominant; V_{TXD} = 0 V	20	45	70	mA
		dominant; short circuit on bus lines; V_{TXD} = 0 V; -3 V < (V_{CANH} = V_{CANL}) < +18 V	2	80	110	mA
I/O level adapter supply; pin V_{IO} [1]						
VI_O	supply voltage on pin V_{IO}		2.91	-	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}	[3]	2.1	-	2.8	V
I_{IO}	supply current on pin V_{IO}	Silent mode	-	3	16	µA
		Normal mode				
		recessive; V_{TXD} = V_{IO} [4]	-	7	30	µA
		dominant; V_{TXD} = 0 V	-	110	320	µA
Silent mode control input; pin S						
V_{IH}	HIGH-level input voltage		2	-	V_{IO}[4]+0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V
I_{IH}	HIGH-level input current	VS = V_{IO} [4]	-1	-	+1	µA
I_{IL}	LOW-level input current	VS = 0 V	-15	-	-1	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		2	-	V_{IO}[4]+0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{IO} [4]	-5	-	+5	µA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	-260	-	-30	µA
C_i	input capacitance	[5]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} [4] - 0.4 V	-9	-3	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	12	mA
Bus lines; pins CANH and CAN						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} - V_{CANH} - V_{CANL}	-400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; [5] F_{TXD}= 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF[6]	0.9V_{CC}	-	1.1V_{CC}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(dif)}$	differential output voltag	dominant; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; V_{TXD} = V_{IO} [4]; no load	-50	-	+50	mV
$V_{O(rec)}$	ecessive output voltage	V_{TXD} = V_{IO} [4]; no load	2	0.5 V_{CC}	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal/Silent mode; -12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V	0.5	-	0.9	V
$V_{rec(RX)}$	receiver recessive voltage	Normal/Silent mode; [5] -12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V	-4	-	0.5	V
$V_{dom(RX)}$	receiver dominant voltage	Normal/Silent mode; [5] -12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V	0.9	-	-.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal mode; -12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V	50	-	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -15 V to +40 V	-100	-70	-	mA
		pin CANL; V_{CANL} = -15 V to +40 V	-	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; V_{TXD} = V_{CC}; V_{CANH} = V_{CANL} = -27 V to +32 V	-5	-	+5	mA
I_L	leakage current	V_{CC} = 0 V or V_{CC} = VIO = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	-5	-	+5	µA
R_i	nput resistance	[5] -2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	9	15	28	kΩ
ΔR_i	input resistance deviation	[5] 0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	[5] -2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[5]	-	-	20	pF
	differential input capacitance	[5]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature		-	185	-	℃

Note:
(1) All circuitry is connected to VCC in the other variants..
(2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
(3) Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
(4) VIO = VCC in non-VIO product variants.
(5) Not tested in production; guaranteed by design.
(6) The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in Figure 6.

10. DYNAMIC CHARACTERISTICS

Table 8. Dynamic characteristics

T_{vj} = -40 °C to +125°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; RL = 60 Ω; C_L = 100 pF unless specified otherwise; all voltages are defined with respect to ground.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3 and Figure 5						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	other variants; Normal mode[3]	-	65	105	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	other variants; Normal mode[3]	-	90	105	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	other variants; Normal mode[3]	-	60	115	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	other variants; Normal mode[3]	-	65	135	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	other variants; Normal mode[3]	50	-	230	ns
		other variants; Normal mode; V_{CC} = 4.75 V to 5.25 V	50	-	210	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	other variants; Normal mode	50	-	230	ns
		other variants; Normal mode; V_{CC} = 4.75 V to 5.25 V	50	-	210	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbit/s); see Figure 3 and Figure 5						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-45	-	+10	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-80	-	+20	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-45	-	+15	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s); see Figure 3 and Figure 5						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-65	-	+30	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-100	-	+50	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-65	-	+40	ns
Dominant time-out time						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode[4]	0.8	3	6.5	ms

Note:

(1) The VIO input is internally connected to VCC in the other variants.

(2) All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range..

(3) Not tested in production; guaranteed by design.

(4) Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

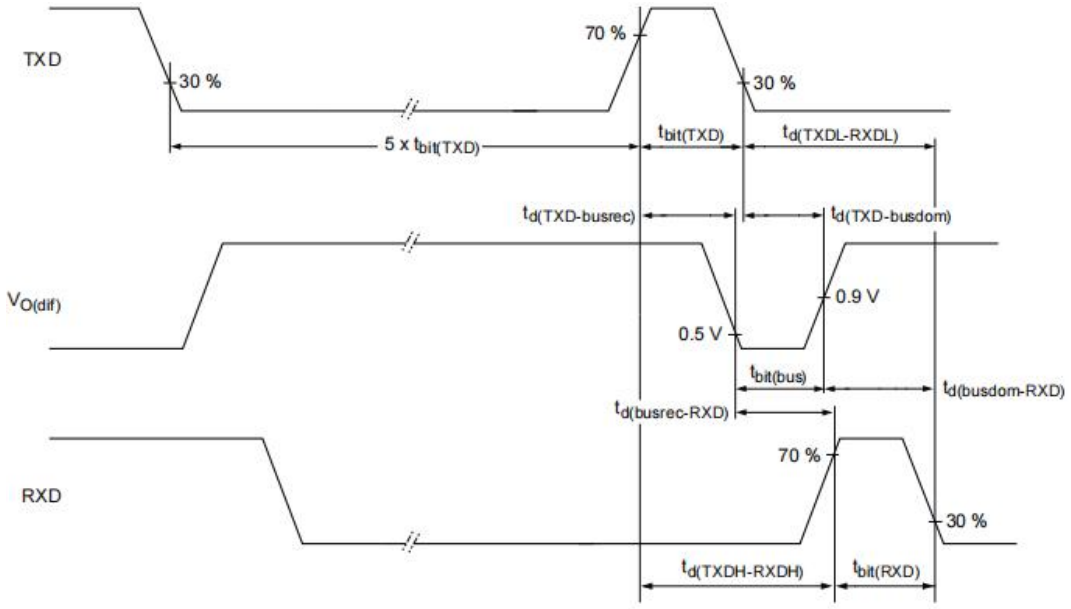
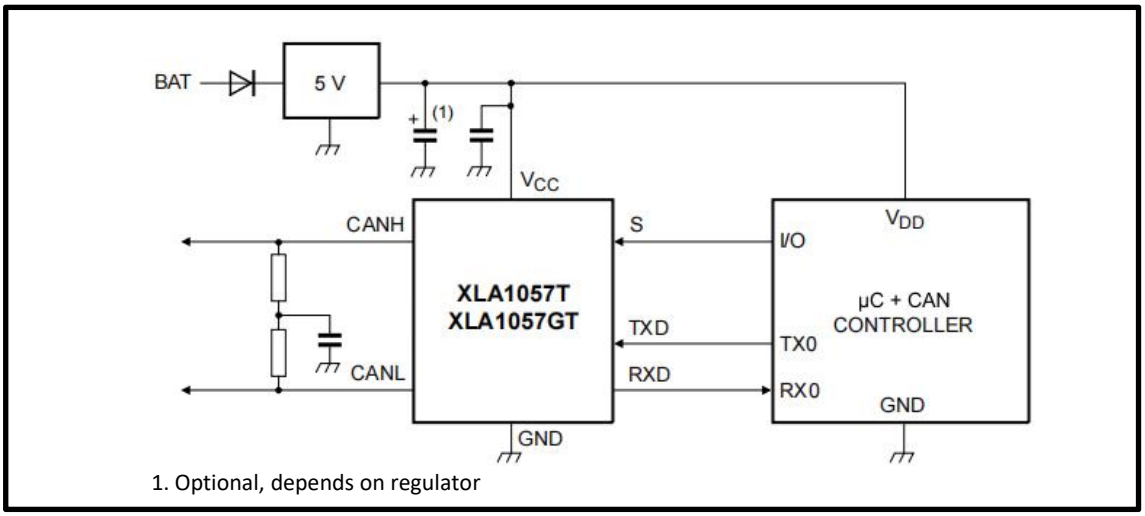


Figure 3. CAN transceiver timing diagram according to ISO 11898-2:2024

11. APPLICATION INFORMATION

11.1. Application diagrams



1. Optional, depends on regulator

Figure 4. Typical XLA1057 application with a 5 V microcontroller (non-V_{IO} variants)

12. TEST INFORMATION

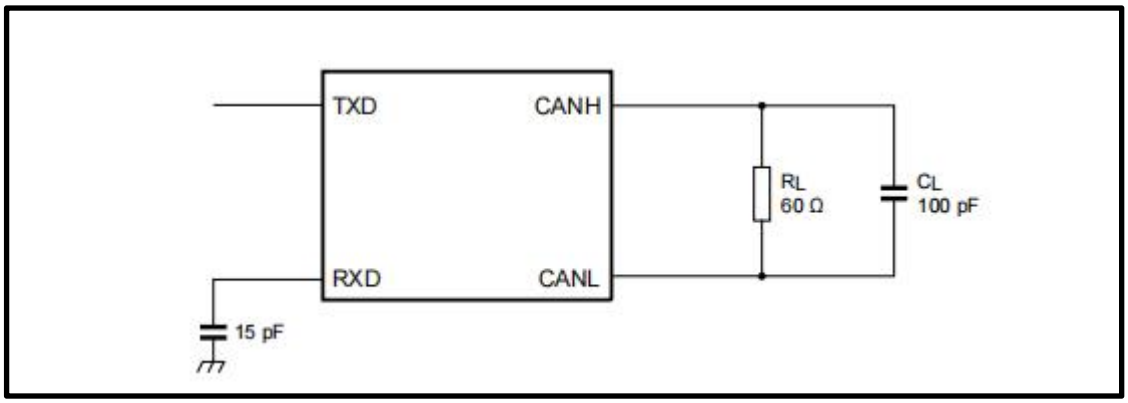


Figure 5. CAN transceiver timing test circuit

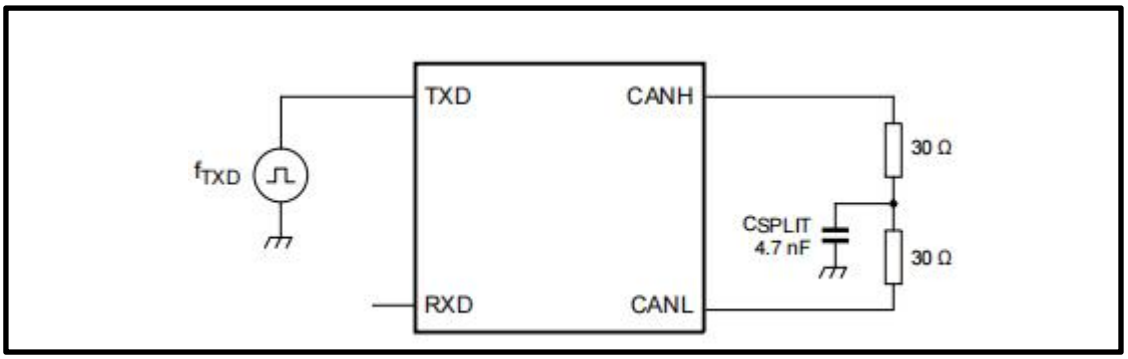


Figure 6. Test circuit for measuring transceiver driver symmetry

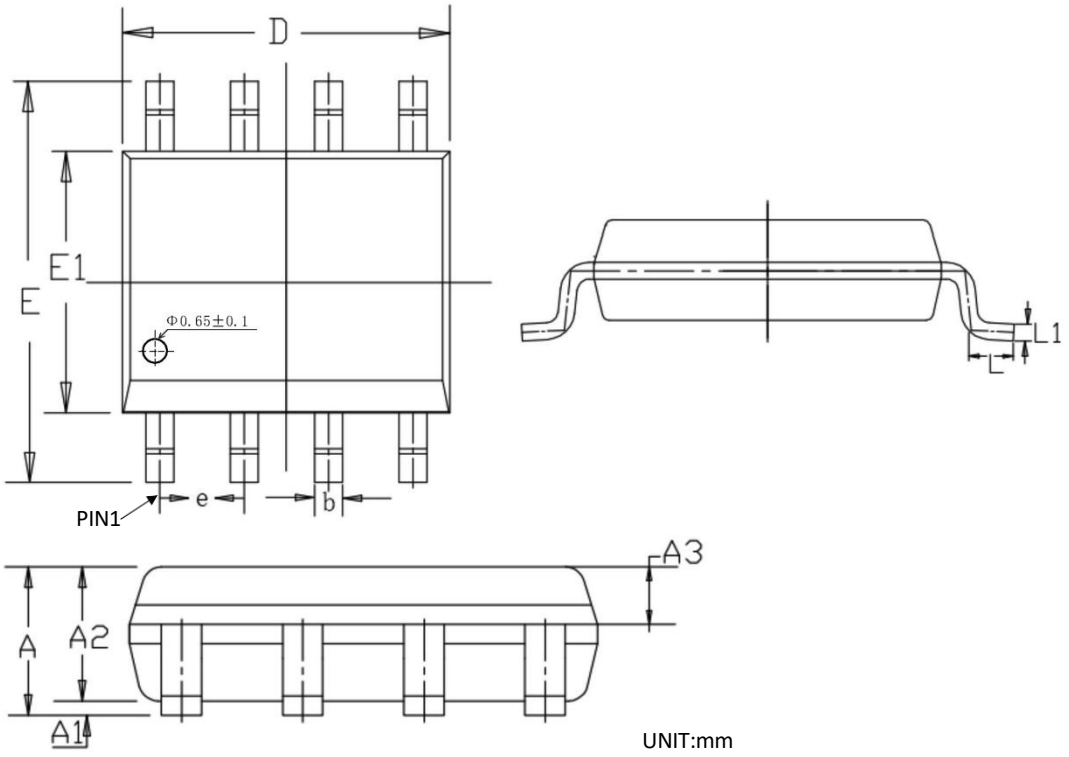
13. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XLA1057T/1	XL1057T1	SOP-8	4.90*3.90	-40 to +125	MSL3	T&R	2500
XLA1057GT	XL1057GT	SOP-8	4.90*3.90	-40 to +125	MSL3	T&R	2500

14. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—