

SCR

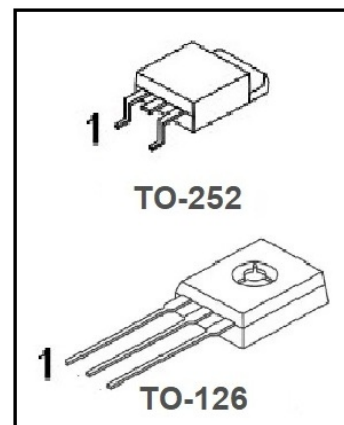
C106

DESCRIPTION

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance,
- High Heat Dissipation and Durability
- Sensitive Gate Triggering

FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
I_{TSM}	20	A
V_{DRM}, V_{RRM}	600/800	V
I_{GT}	15-200	μA



Package	Pin assignment		
	1	2	3
TO-252	K	A	G
TO-126	K	A	G

SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE		UNIT
Repetitive Peak Off-State Voltages	V_{DRM}, V_{RRM}	C106D	400	V
		C106M	600	
RMS on-State Current	$I_{T(RMS)}$	4		A
Non-Repetitive Peak On-State Current	I_{TSM}	20		A
Peak gate current	I_{GM}	1.0		A
Peak Gate Power	P_{GM}	1		W
Peak Reverse Gate Voltage	V_{RGM}	5		V
Operating junction temperature	T_J	-40~+125		°C
Storage Temperature	T_{STG}	-40~+150		°C

ELECTRICAL CHARACTERISTICS (T_J=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Repetitive Forward or Reverse Blocking Current	I _{DRM} I _{RRM}	V _{AK} = Rated V _{DRM} or V _{RRM} ;			5	uA
Gate Trigger Current	I _{GT}	V _D =12V, R _L =100Ω	10		200	uA
Gate Trigger Voltage	V _{GT}	V _D =12V, R _L =100Ω		0.65	0.8	V
Peak Forward On-State Voltage	V _{TM}	I _T = 4A, I _G =50mA			1.7	V
Latch Current	I _L	I _G =1.2I _{GT}			6	mA
Holding Current	I _H	I _T =50mA			5	mA
Gate Non-Trigger Voltage	V _{GD}	V _D = V _{DRM} 12V	0.2			v
Critical Rate of Rise of Off-State Voltage	dV/dt	V _D =67%V _{DRM} , R _{GK} =1kΩ,	10			V/μs

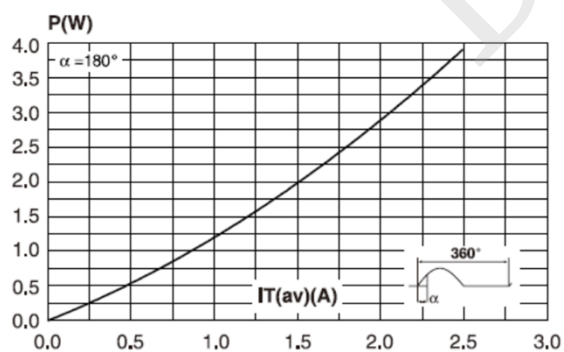
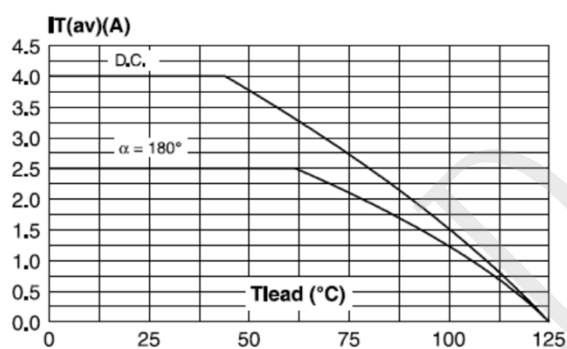
ELECTRICAL CHARACTERISTIC CURVE
Fig. 1: Maximum average power dissipation versus average on-state current.

Fig. 2-1: Average and D.C. on-state current versus lead temperature.


Fig. 2-2: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout).

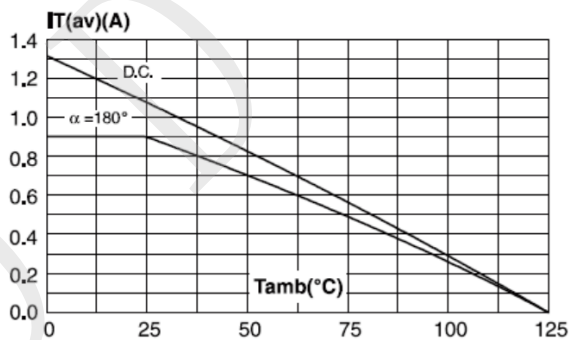


Fig. 3: Relative variation of thermal impedance junction to ambient versus pulse duration.

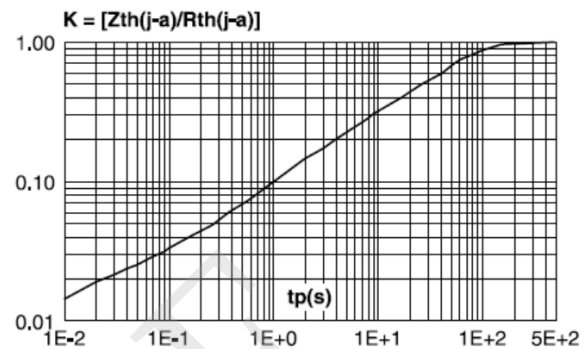


Fig. 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

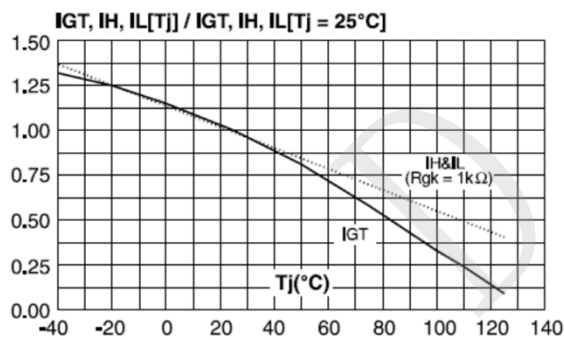
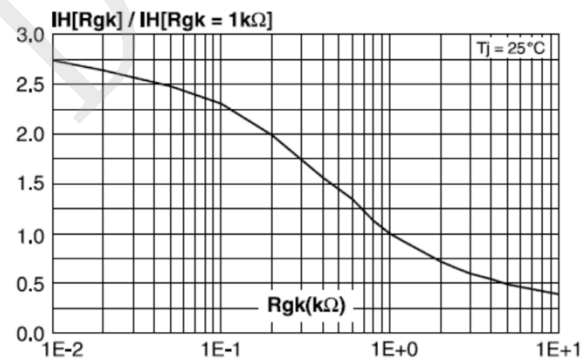


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).



SCR

C106

Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

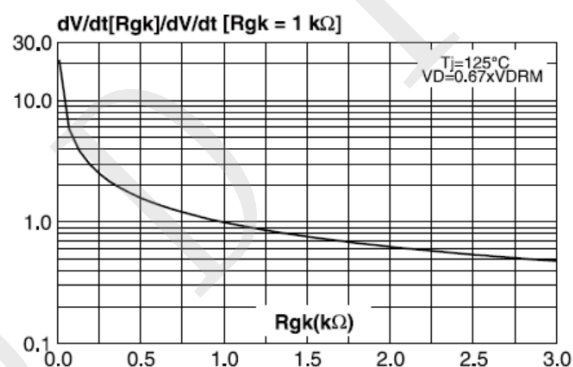


Fig. 8: Surge peak on-state current versus number of cycles.

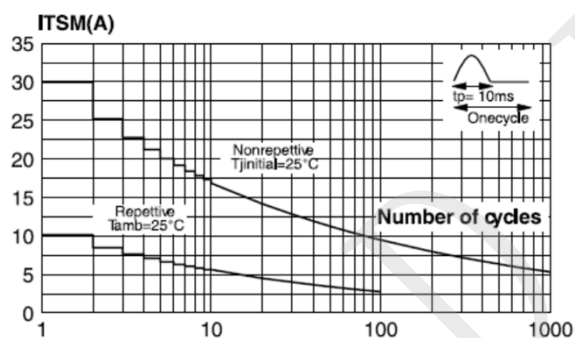


Fig. 10: On-state characteristics (maximum values).

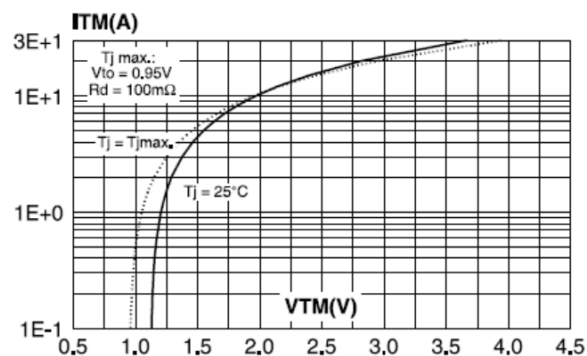


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values).

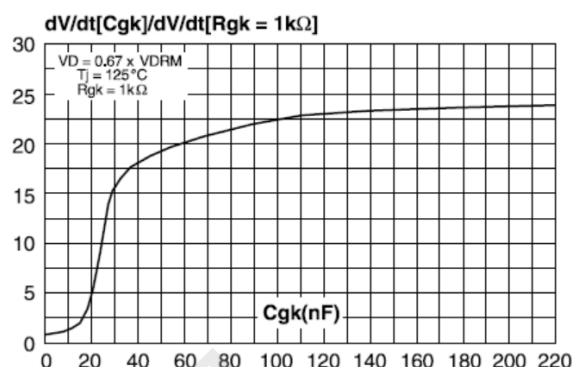


Fig. 9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms, and corresponding value of I^2t .

