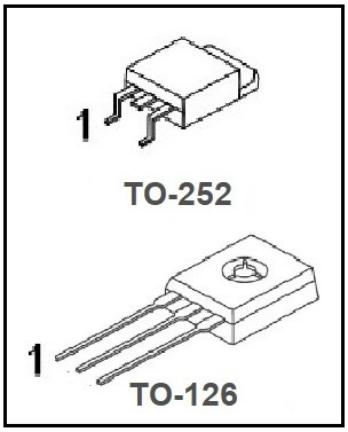
鼎德丰
DING DE FENG

SCR C106

DESCRIPTION

- ●Glassivated Surface for Reliability and Uniformity
- ●Power Rated at Economical Prices
- ●Practical Level Triggering and Holding Characteristics
- ●Flat, Rugged, Thermopad Construction for Low Thermal Resistance,
  High Heat Dissipation and Durability
- ●Sensitive Gate Triggering



FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
I_{TSM}	20	A
$V_{DRM,}V_{RRM}$	600/800	V
I_{GT}	15-200	μA

Package	Pin assignment		
	1	2	3
TO-252	K	A	G
TO-126	K	A	G

SYMBOL

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE		UNIT
Repetitive Peak Off-State Voltages	V_{DRM}, V_{RRM}	C106D	400	V
		C106M	600	
RMS on-State Current	$I_{T(RMS)}$	4		A
Non-Repetitive Peak On-State Current	I_{TSM}	20		A
Peak gate current	I_{GM}	1.0		A
Peak Gate Power	P_{GM}	1		W
Peak Reverse Gate Voltage	V_{RGM}	5		V
Operating junction temperature	T_J	-40~+125		℃
Storage Temperature	T_{STG}	-40~+150		℃

ELECTRICAL CHARACTERISTICS (TJ=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Repetitive Forward or Reverse Blocking Current	I_{DRM} I_{RRM}	V_{AK} = Rated V_{DRM} or V_{RRM};			5	uA
Gate Trigger Current	I_{GT}	V_D=12V, R_L=100Ω	10		200	uA
Gate Trigger Voltage	V_{GT}	V_D=12V, R_L=100Ω		0.65	0.8	V
Peak Forward On-State Voltage	V_{TM}	I_T= 4A, I_G=50mA			1.7	V
Latch Current	I_L	I_G=1.2I_{GT}			6	mA
Holding Current	I_H	I_T=50mA			5	mA
Gate Non-Trigger Voltage	V_{GD}	V_D= V_{DRM} 12V	0.2			v
Critical Rate of Rise of Off-State Voltage	dV/dt	VD=67%VDRM, RGK=1kΩ,	10			V/μs

ELECTRICAL CHARACTERISTIC CURVE

Fig. 1: Maximum average power dissipation versus average on-state current.

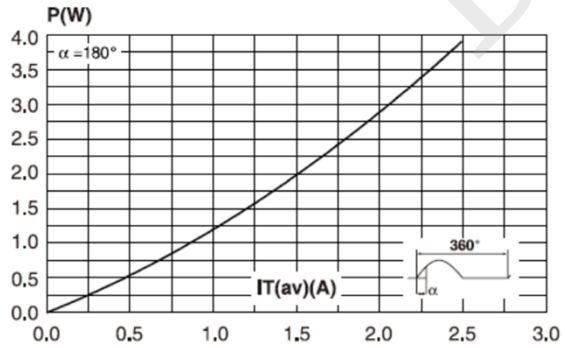


Fig. 2-1: Average and D.C. on-state current versus lead temperature.

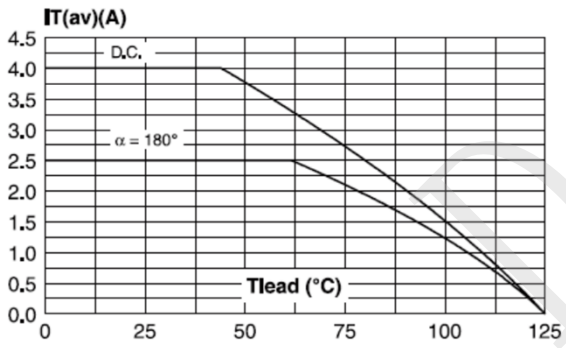


Fig. 2-2: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout).

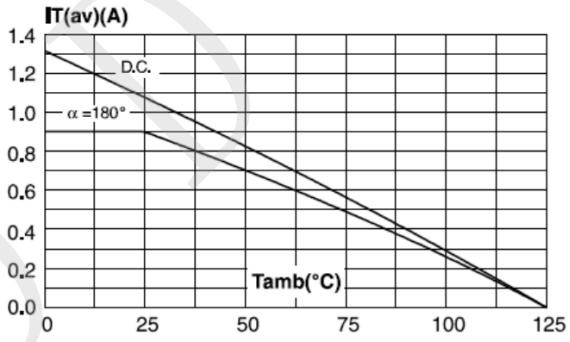


Fig. 3: Relative variation of thermal impedance junction to ambient versus pulse duration.

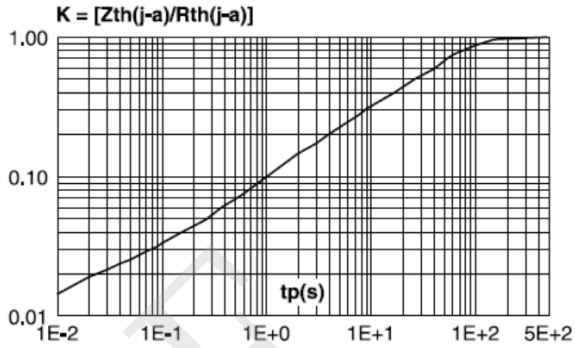


Fig. 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

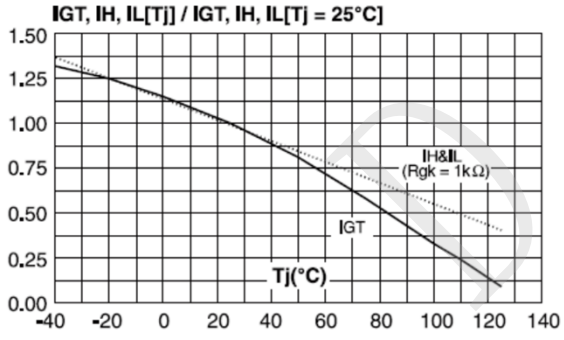


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

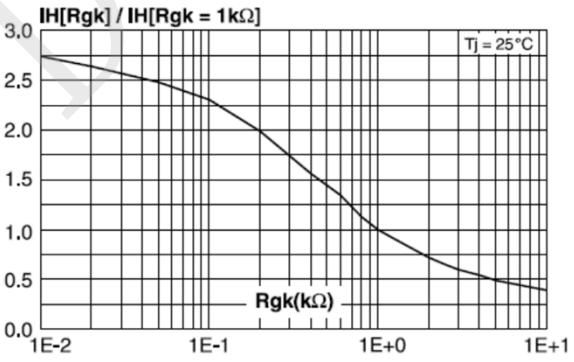


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

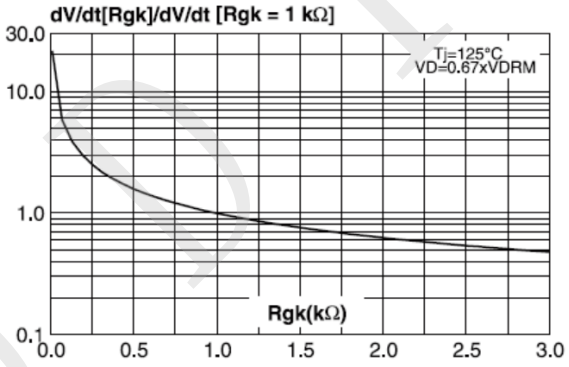


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values).

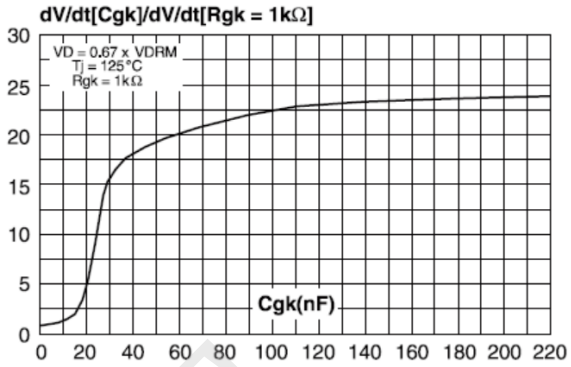


Fig. 8: Surge peak on-state current versus number of cycles.

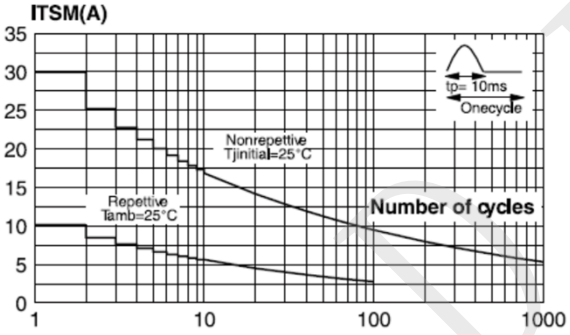


Fig. 9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding value of I^2t.

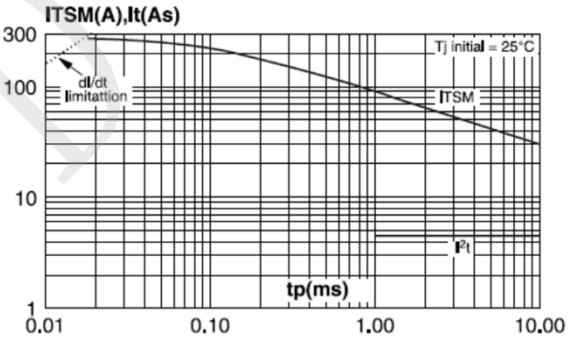


Fig. 10: On-state characteristics (maximum values).