SA21340

300mA, 36V Fast-Response LDO Regulator

General Description

The SA21340 is a 300mA high current capacity linear regulator, which features ultra-low ground current and low drop out voltage. The SA21340 has an adjustable output which can be set by two external resistors. The device with fully protection includes over current limit, output short protection and over temperature operation.

Ordering Information

SA21340 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SA21340FCA	SO8E	--

Features

- High-current Capability: 300mA Over Full Temperature Range
- Low-dropout Voltage of 300mV at Full Load 300mA.
- Adjustable Output Voltage
- Low Ground Current
- Over Current Limit Protection
- Output Short Circuit Protection(Hiccup Mode)
- Over Temperature Protection.
- Reset Output with Programmable Timeout Period
- Packages: SO8E
- RoHS Compliant and Halogen Free
- Automotive AEC- Q100 Grade 1 Certified

Applications

- Industrial/Automotive Application
- Portable/Battery-Powered Equipment
- Ultra Low-Power Microcontrollers
- Cellular Handsets
- Medical Imaging

Typical Application

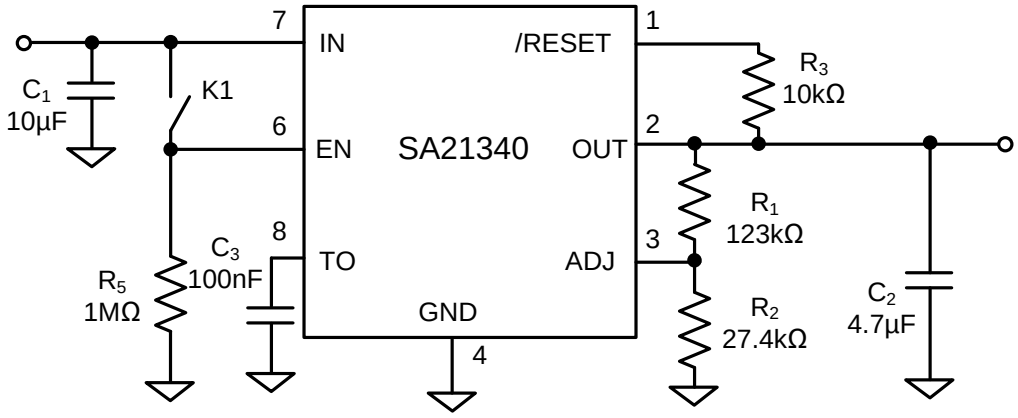
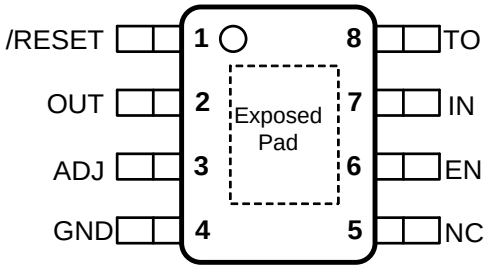


Figure1. Schematic

Pinout



SO8E

Top Mark: BTE*xyz* (device code: BTE, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
/RESET	1	Open drain reset output. /RESET low when OUT below the reset threshold and remains low for the duration of the reset timeout period after the reset conditions end. If no cap connect at TO pin, RESET pull high immediately after V_{OUT} exceeds the reset threshold. if it isn't used, leave it floating or connect to GND.
OUT	2	Output pin. Bypass this pin to Ground pin with a low ESR 4.7μF output capacitor.
ADJ	3	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. V_{OUT}=0.6×(1+R1/R2).
GND	4	Ground pin.
NC	5	No connection.
EN	6	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave floating.
IN	7	IC power supply input. Bypass this pin to Ground pin with a 4.7μF capacitor.
TO	8	Reset timeout programming pin. Connect a capacitor from this pin to GND for different reset timeout time.
	Exposed Pad	The exposed pad should be connected to ground plane for better thermal performance.

Block Diagram

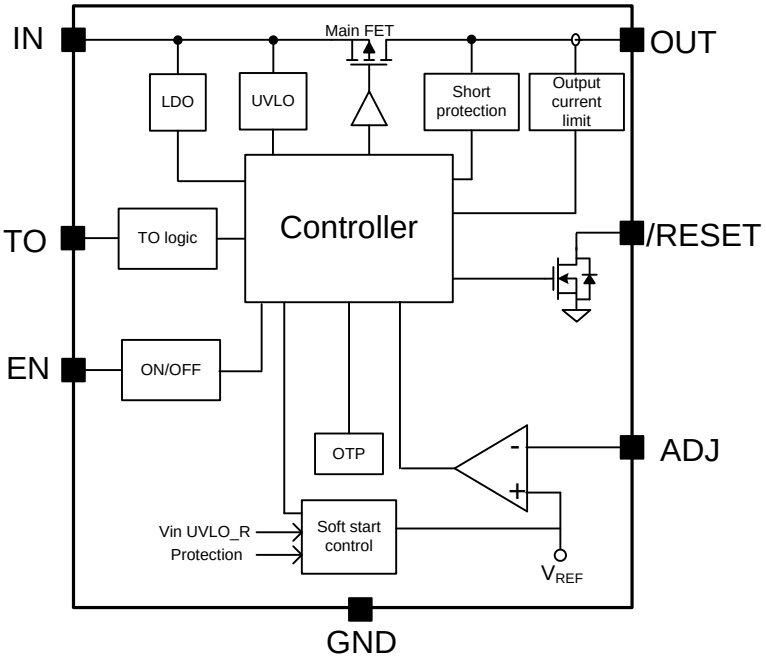


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, EN, OUT, ADJ, /RESET ---------- -0.3V to 40V
TO---------- -0.3V to 3.6V
Power Dissipation, @ T_A = 25°C SO8E---------- 2.6W
Package Thermal Resistance (Note 2)
SO8E, θ_{JA}---------- 38.3°C/W
SO8E, θ_{JC} ---------- 12.6°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ----------260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 36V
EN, OUT, ADJ, /RESET ---------- 0V to 36V
TO----------0V to 3.3V
Ambient Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{EN}=12V, T_A = -40°C~125°C, unless otherwise specified, the values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}		4		36	V
Reference Voltage	V_{REF}	T_J= -40°C ~125°C	0.588	0.6	0.612	V
		T_A=25°C	0.594	0.6	0.606	
ADJ pin Bias Current	I_{ADJ_Bias}	EN=0, ADJ pin floating	-50		50	nA
Line Regulation	ΔV_{LNR}	I_{OUT} = 10mA, 4 ≦ V_{IN} ≦36V		1	1.5	mV/V
Load Regulation	ΔV_{LDR}	V_{IN} = 5V, 10mA ≦ I_{OUT} ≦ 0.3A,		0.25	0.5	%
Dropout Voltage	ΔV_{DROP}	I_{OUT} = 10mA		10	20	mV
		I_{OUT} = 300mA		300	540	mV
Quiescent Current	I_Q	I_{OUT} = 0mA, V_{IN}=(V_{OUT}+1V)~36V		7	14	µA
Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=24V			5	µA
Current Limit	I_{limit}	V_{OUT}=0.9xV_{OUT}(normal)	600	900	1200	mA
Output Short Protection Threshold	$V_{ADJ,SHORT}$	V_{FB} Falling	8	16	30	%V_{REF}
Output Short Off Time	t_{short_off}			16		ms
Power Supply Rejection	PSRR	Frequency=100Hz, C_{OUT}=4.7µF,I_{OUT}=10mA T_A=25°C		60		dB
		Frequency=100kHz, C_{OUT}=4.7µF I_{OUT}=10mA T_A=25°C		35		
Input Voltage UVLO Threshold	V_{UVLO}	V_{IN} rising	2.9	3.3	4	V
UVLO Hysteresis	V_{UVLO_th}			200		mV
Enable Input Logic-High Voltage	$V_{EN,H}$		1.5			V
Enable Input Logic-Low Voltage	$V_{EN,L}$				0.4	V
Soft Start Time	t_{SS}			1		ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
V_{TO} /REST High-level Threshold	V_{TR}	VTO rising	1.4	1.8	2.2	V
To Default Rise Up time	$t_{To,Rise}$	OUT High, TO Floating, Rising from 0 to V_{TR}		1.6		us
To Charge Current	I_{TR}		8	16	24	uA
V_{OUT} /RESET Threshold	V_{OR}	V_{OUT} rising	85	90	95	% V_{OUT}

V_{OUT} /RESET Threshold Hysteresis	$V_{OR,HYS}$	V_{OUT} falling		5		% V_{OUT}
/RESET Output-Voltage Low					0.4	V

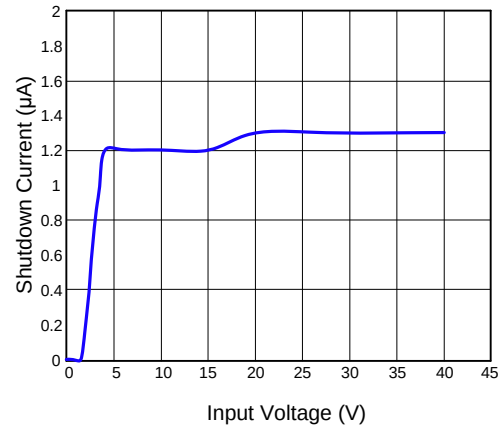
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

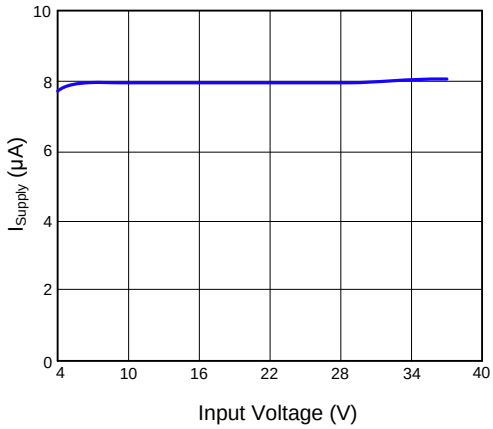
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

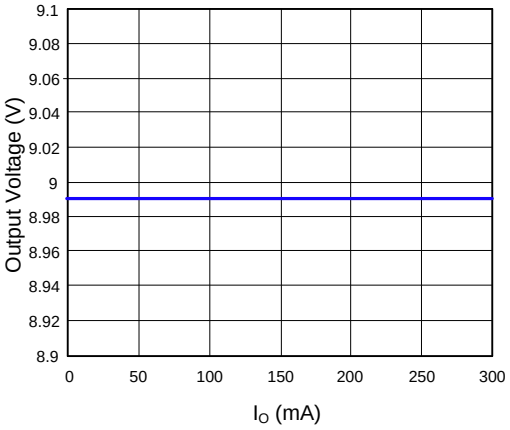
Shutdown Current vs. Input Voltage



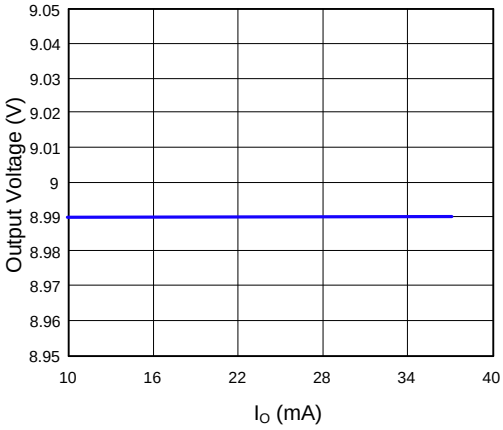
Supply Current vs. Input Voltage



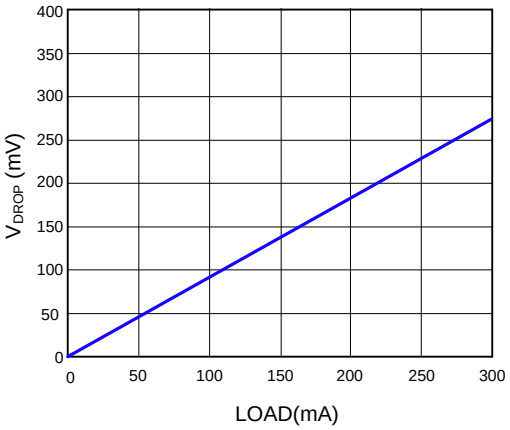
Load Regulation



Line Regulation

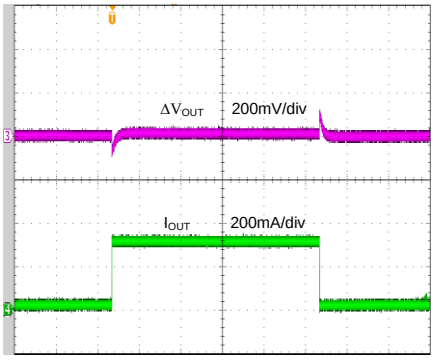


DropOUT vs. LOAD



Load Transient

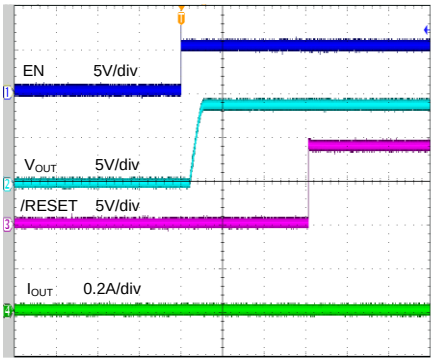
(V_{IN}=14V, V_{OUT}=9V, I_{OUT}=10mA~300mA)



Time (400μs/div)

Startup from EN

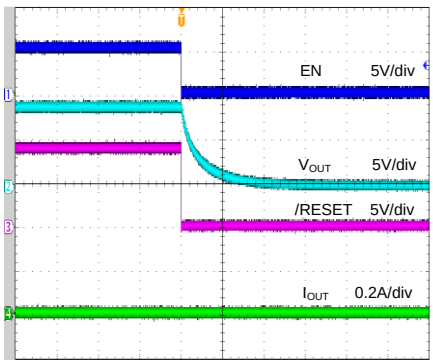
(V_{IN}=14V, V_{OUT}=9V, NO LOAD, EN=0V to 5V, C_{TO}=100nF)



Time (4ms/div)

Shutdown from EN

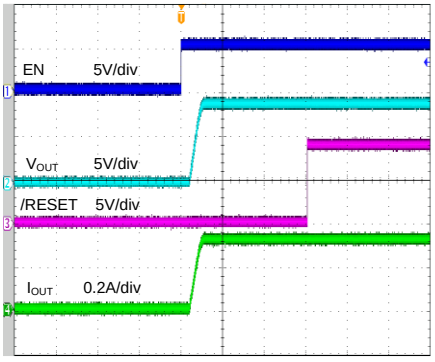
(V_{IN}=14V, V_{OUT}=9V, NO LOAD, EN=5V to 0V, C_{TO}=100nF)



Time (2ms/div)

Startup from EN

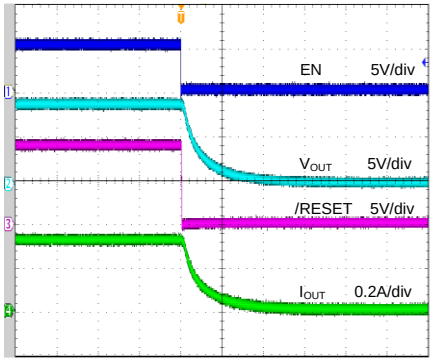
(V_{IN}=14V, V_{OUT}=9V, 300mA LOAD, EN=0V to 5V, C_{TO}=100nF)



Time (4ms/div)

Shutdown from EN

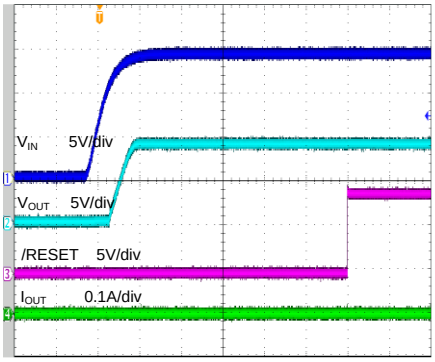
(V_{IN}=14V, V_{OUT}=9V, 300mA LOAD, EN=5V to 0V, C_{TO}=100nF)



Time (100μs/div)

Startup from VIN

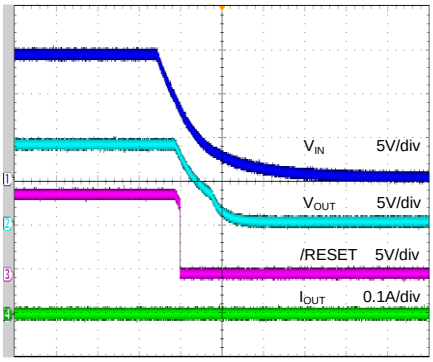
(EN=5V, V_{OUT}=9V, NO LOAD, V_{IN}=0V to 14V, C_{TO}=100nF)



Time (2ms/div)

Shutdown from VIN

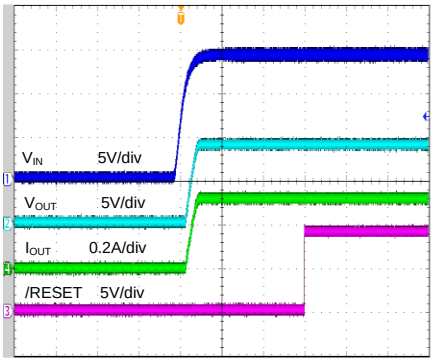
(EN=5V, V_{OUT}=9V, NO LOAD, V_{IN}=14V to 0V, C_{TO}=100nF)



Time (100ms/div)

Startup from VIN

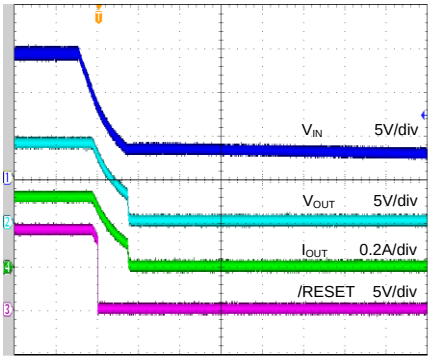
(EN=5V, V_{OUT}=9V, 300mA LOAD, V_{IN}=0V to 14V, C_{TO}=100nF)



Time (4ms/div)

Shutdown from VIN

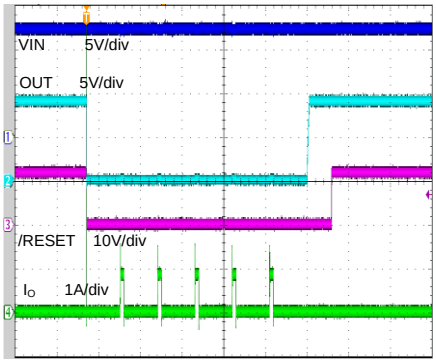
(EN=5V, V_{OUT}=9V, 300mA LOAD, V_{IN}=14V to 0V, C_{TO}=100nF)



Time (4ms/div)

Short Protect

(VIN=12V, OUT=9V)

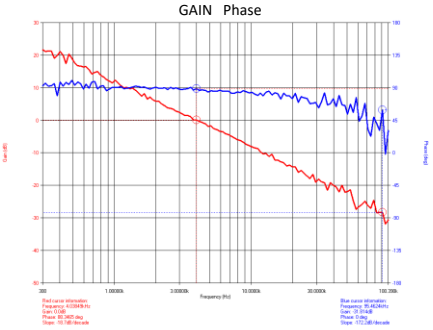


Time (20ms/div)

LOOP GAIN

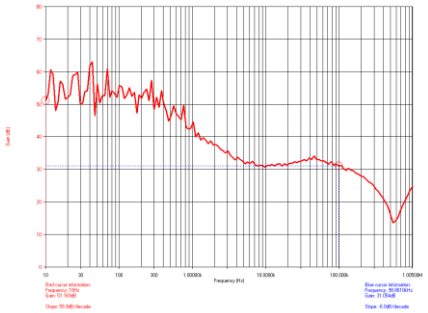
(VIN=12V, OUT=9V, COUT=4.7uF, 300mA Load)

GAIN Phase



PSRR

(VIN=12V, OUT=9V, COUT=4.7uF, 300mA Load)



Operation

SA21340 is a 300mA high current capacity linear regulator, which features ultra-low ground current and low drop out voltage. SA21340 has an adjustable output which can be set by two external resistors. The device with fully protection includes over current limit, output short protection and over temperature operation.

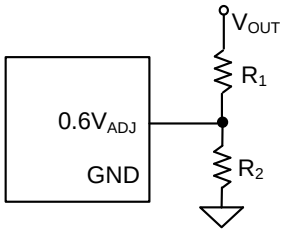
Applications Information

Adjustable Output Voltage

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 2MΩ is highly recommended for both resistors.

The output voltage can be selected using the following equation:

$VOUT = 0.6V \times (1 + R_1/R_2)$



Over Temperature Protection (OTP)

SA21340 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation

Output Short Circuit Protect

If V_{OUT} drop below than 16% of the OUT set point, the short circuit protection mode will be initiated, and the device will be shut down for approximately 16ms. The device will then restart with a complete soft-start cycle. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the OTP threshold is reached.

/RESET Function

SA21340 includes an open-drain reset output. Once the output voltage exceeds the reset threshold voltage (90% of the OUT set point), the C_{TO} is charged with the current I_{TR}, /RESET will be high when the voltage on C_{TO} is larger than V_{TR}. If output voltage is lower than the reset threshold voltage, the device discharges C_{TO} fast and /RESET is set to low when the voltage on TO is lower than V_{TF}.

Timeout

The SA21340 features a reset timeout period adjustable input. The internal capacitance produces a 1.6μs default delay when TO pin is floating. Connect a capacitor from TO to GND to set a higher timeout period than default. Use the following formula to determine the reset timeout capacitor:

$$C_{TO} = \frac{16\mu A \times T_{TIMEOUT}}{1.8V}$$

Input Capacitor C_{IN} and Output Capacitor C_{OUT}

To minimize the potential noise problem and improve power-supply rejection(PSRR) and transient response, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7uF low ESR ceramic capacitor is recommended.

For stable operation over the full temperature range, a 4.7μF low-ESR ceramic capacitor is recommended. Use larger output-capacitor values such as 22μF to reduce noise, improve load-transient response and PSRR. Some ceramic dielectrics exhibit large capacitance and ESR variations with temperature.

PCB Layout Guide

For best performance of the SA21340, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 2-layer or 4-layer board for thermal performance and better capability of current flow. At least 6 vias are suggested to put around each power pin to distribute current to different PCB layer. These power pins include IN and OUT.

2. Place input/output capacitor close to the IC for better transient performance.

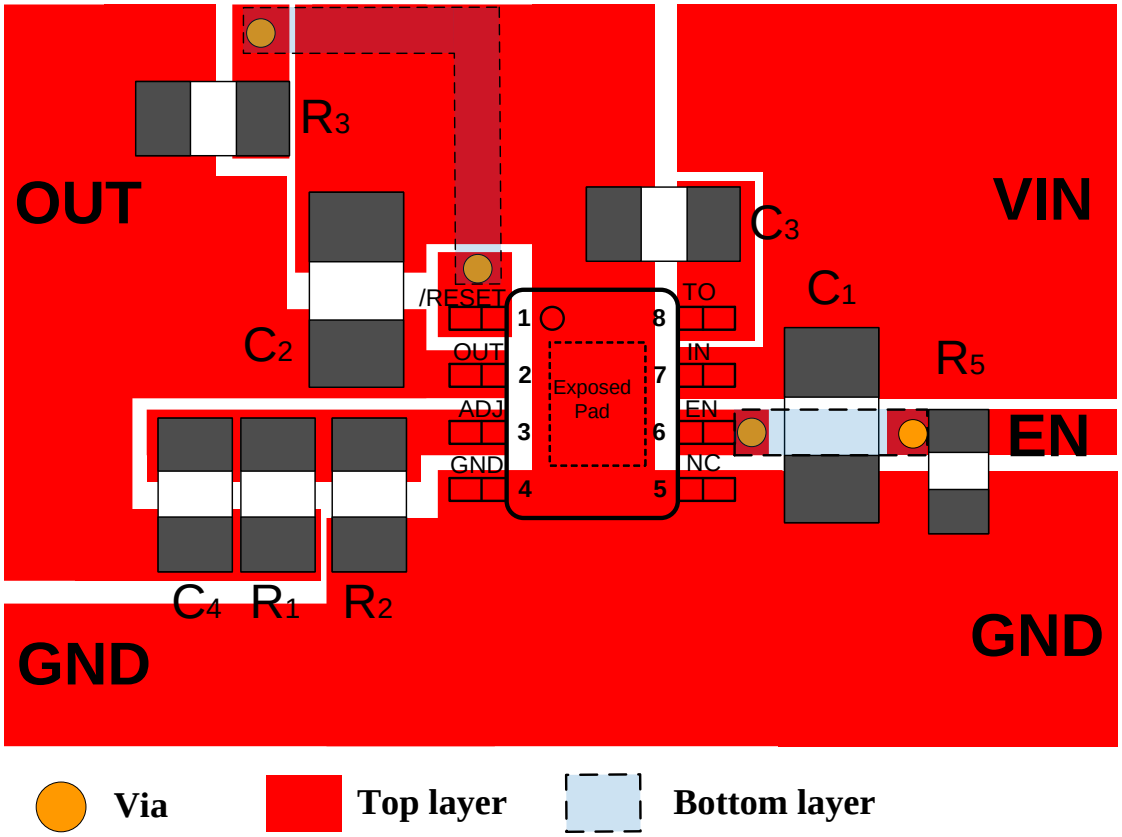
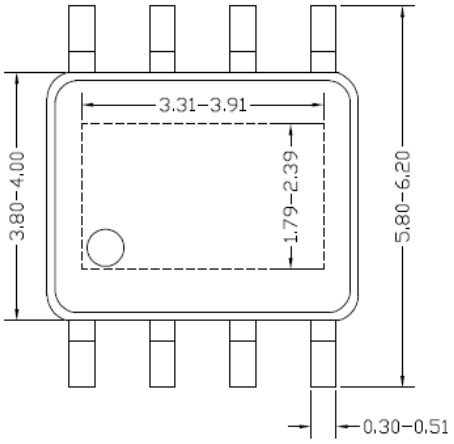
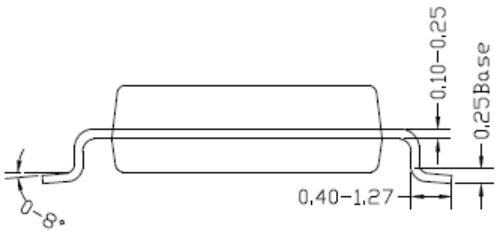


Figure3. PCB Layout Suggestion

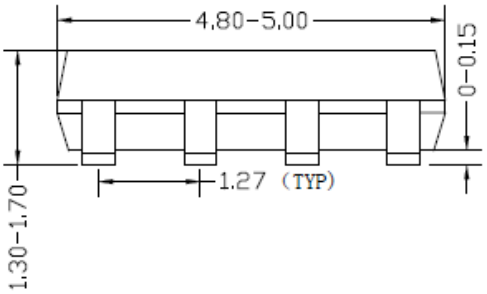
SO8E Package Outline & PCB Layout



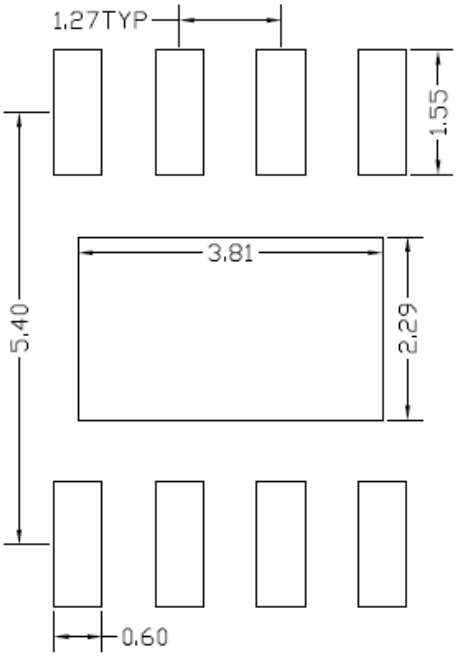
Top view



Side view



Front view



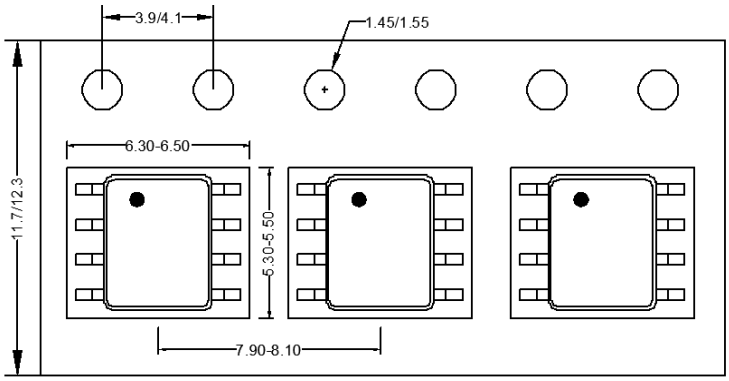
Recommended PCB Layout (Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

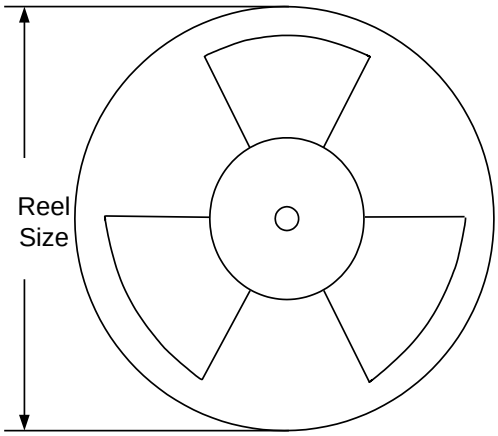
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.13, 2022	Revision 0.9C	Update the Input Voltage UVLO Threshold & Output Short Protection Threshold in EC table (page 4)
Sep.07, 2021	Revision 0.9B	1. Update the package outline drawing.
Jun.12, 2020	Revision 0.9A	1. Update the schematic diagram (page1); 2. Update the startup/shutdown waveforms (page7~8); 3. Update the PCB layout suggestion (page10).
Dec.27, 2019	Revision 0.9	Initial Release

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