

## TRIAC

## MAC97A6

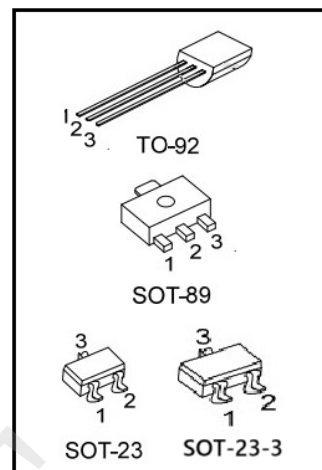
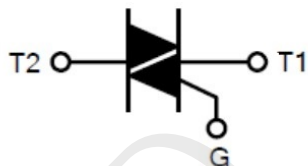
### FEATURES

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits and microcontrollers
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

### APPLICATIONS

- General purpose bi-directional switching and phase control application.
- Air conditioner indoor fan control
- General purpose motor control
- General purpose switching

### SYMBOL:



| Package  | Pin assignment |    |    |
|----------|----------------|----|----|
|          | 1              | 2  | 3  |
| TO-92    | T1             | G  | T2 |
| SOT-23   | T1             | G  | T2 |
| SOT-23-3 | T1             | G  | T2 |
| SOT-89   | T1             | T2 | G  |

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER                                                    | SYMBOL              | VALUE      |    | UNIT             |
|--------------------------------------------------------------|---------------------|------------|----|------------------|
| Repetitive Peak Off-State Voltages                           | $V_{\text{DRM}}$    | 400/600    |    | V                |
|                                                              | $V_{\text{RRM}}$    | 400/600    |    |                  |
| RMS on-State Current                                         | $I_{\text{T(RMS)}}$ | 0.8        |    | A                |
| Non-Repetitive Peak On-State Current                         | $I_{\text{TSM}}$    | 8          |    | A                |
| $I^2t$ for fusing                                            | $I^2t$              | 0.26       |    | A <sup>2</sup> s |
| Repetitive rate of rise of on-state current after triggering | $dI_{\text{T}}/dt$  | I-II-III   | 50 | A/ $\mu$ S       |
|                                                              |                     | IV         | 10 |                  |
| Peak gate current                                            | $I_{\text{GM}}$     | 1          |    | A                |
| Peak Gate Power                                              | $P_{\text{GM}}$     | 1          |    | W                |
| Average Gate Power                                           | $P_{\text{G(AV)}}$  | 0.1        |    | W                |
| Operating junction temperature                               | $T_{\text{J}}$      | -40~+125   |    | °C               |
| Storage Temperature                                          | $T_{\text{STG}}$    | -40 ~ +150 |    | °C               |

**ELECTRICAL CHARACTERISTICS** (T<sub>J</sub>=25°C)

| PARAMETER                                           | SYMBOL                 | TEST CONDITIONS                                    |     | MIN | MAX | UNITS      |
|-----------------------------------------------------|------------------------|----------------------------------------------------|-----|-----|-----|------------|
| Peak Repetitive Forward or Reverse Blocking Current | $I_{DRM}$<br>$I_{RRM}$ | $V_{AK} = \text{Rated } V_{DRM}$<br>or $V_{RRM}$ ; |     |     | 5   | uA         |
| Gate Trigger Current                                | $I_{GT}$               | $V_D=12V$ ,<br>$R_L=100\Omega$                     | I   |     | 5   | mA         |
|                                                     |                        |                                                    | II  |     | 5   |            |
|                                                     |                        |                                                    | III |     | 5   |            |
|                                                     |                        |                                                    | IV  |     | 10  |            |
| Gate Trigger Voltage                                | $V_{GT}$               | $V_D=12V$ ,<br>$R_L=100\Omega$                     |     |     | 1.3 | V          |
| Peak Forward On-State Voltage                       | $V_{TM}$               | $I_T=1.0A$                                         |     |     | 1.5 | V          |
| Latch Current                                       | $I_L$                  | $I_G = 1.2 I_{GT}$                                 | I   |     | 10  | mA         |
|                                                     |                        |                                                    | II  |     | 20  |            |
|                                                     |                        |                                                    | III |     | 10  |            |
|                                                     |                        |                                                    | IV  |     | 10  |            |
| Holding Current                                     | $I_H$                  | $I_T=0.1A$                                         |     |     | 8   | mA         |
| Gate Non-Trigger Voltage                            | $V_{GD}$               | $V_D=V_{DRM}$                                      |     | 0.2 |     | V          |
| Critical Rate of Rise of Off-State Voltage          | $dV/dt$                | $V_D=67\%V_{DRM}$ ,<br>$R_{GK}=1k\Omega$           |     | 5   |     | V/ $\mu s$ |