50-V 8-Ch Low-side Driver Array with Shift Register Interface

Features

- 8-channel 50-V Low-side Driver Array
- 500-mA Rated Drain Current (Per Channel)
- Very Low Output Leakage < 10 nA Per Channel
- Power Efficient with Low R_{DS-on}
- Extended Temperature Range: T_A = −40°C to 125°C
- High-voltage Outputs: 50 V
- Compatible with 1.8-V to 5.0-V Logic Interface
- Integrated Free-wheeling Diodes for Inductive Load
- Improved Noise Immunity with Integrated RC Filter
- ESD Protection Exceeds JESD 22 – 2.5-kV HBM, 2-kV CDM
- Available in TSSOP16 Package

Applications

- Inductive Loads
  - Relays
  - Unipolar Stepper & Brushed DC Motors
  - Solenoids & Valves
- LED Indicators
- Logic Level Shifting
- Gate & IGBT Drive

Description

The TPM0596 is a high-voltage, high-current NMOS transistor array with a shift register interface. This device consists of eight channels of low-side NMOS transistors with high-voltage outputs and a free-wheeling diode for inductive loads.

The maximum drain-current rating of a single NMOS channel is 500 mA. The device supports a wide I/O voltage range from 1.8 V to 5 V. The transistors can be paralleled for higher current capability.

The TPM0596 can replace traditional bipolar Darlington arrays with better thermal efficiency and reliability and saves I/Os.

Typical Application Circuit

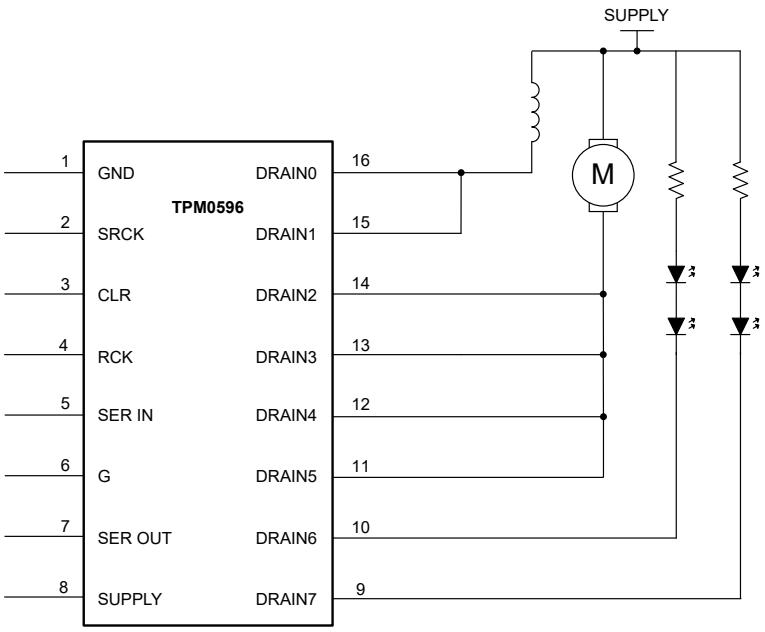


Table of Contents

Product Family Table

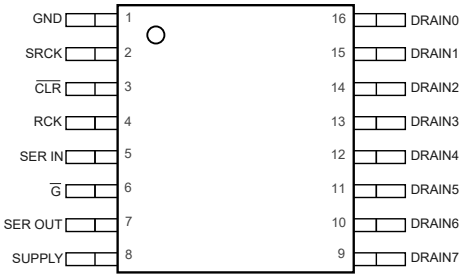
Orderable Part Number	Package
TPM0596-TS3R	TSSOP16
TPM0596C-TS3R	TSSOP16
TPM0596C-QFNR	QFN3X3-16

Revision History

Date	Revision	Notes
2020-12-15	Rev A.0	Initial version
2022-03-10	Rev A.1	Updated transport media, quantity
2022-03-10	Rev A.2	Correction on interface description
2024-08-30	Rev A.3	Updated the datasheet format Added the TPM0596C part number and the QFN package

Pin Configuration and Functions

TPM0596
TSSOP16
Top View



TPM0596
QFN3X3-16
Top View

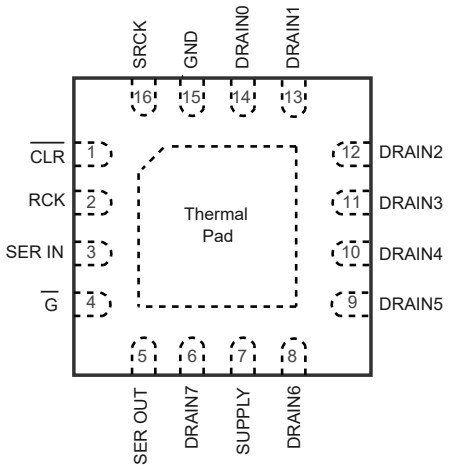


Table 1. Pin Functions: TSSOP16

Pin No.	Name	I/O	Description
3	$\overline{CLR}$	Input	Shift register clear, active-low
6	$\overline{G}$	Input	Output gating, active-low
1	GND	Ground	Device ground
16	DRAIN0	Output	Low-side driver output
15	DRAIN1	Output	Low-side driver output
14	DRAIN2	Output	Low-side driver output
13	DRAIN3	Output	Low-side driver output
12	DRAIN4	Output	Low-side driver output
11	DRAIN5	Output	Low-side driver output
10	DRAIN6	Output	Low-side driver output
9	DRAIN7	Output	Low-side driver output
4	RCK	Input	Register clock
5	SER IN	Input	Serial data input
7	SER OUT	Output	Serial data output
2	SRCK	Input	Shift register clock
8	SUPPLY	Power	Device supply voltage, should be tied above 3.3 V.

Table 2. Pin Functions: QFN3X3-16

Pin No	Name	I/O	Description
1	$\overline{CLR}$	Input	Shift register clear, active-low
4	$\overline{G}$	Input	Output gating, active-low
15	GND	Ground	Device ground
14	DRAIN0	Output	Low-side driver output
13	DRAIN1	Output	Low-side driver output
12	DRAIN2	Output	Low-side driver output
11	DRAIN3	Output	Low-side driver output
10	DRAIN4	Output	Low-side driver output
9	DRAIN5	Output	Low-side driver output
8	DRAIN6	Output	Low-side driver output
6	DRAIN7	Output	Low-side driver output
2	RCK	Input	Register clock
3	SER IN	Input	Serial data input
5	SER OUT	Output	Serial data output
16	SRCK	Input	Shift register clock
7	SUPPLY	Power	Device supply voltage, should be tied above 3.3 V.
Thermal Pad	Thermal Pad	GND	Connect Thermal Pad to GND for better thermal dissipation

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	−0.3	52	V
V_{OUTx}	Output Voltage Range DRAIN0 − DRAIN7	−0.3	55	V
V_{IN}	Input Voltage Range SER IN, RCK, SRCK, $\overline{CLR}$, $\overline{G}$	−0.3	30	V
I_{OUTx}	Continuous Output Channel Current DRAIN0 − DRAIN7		500	mA
I_{GND}	Continuous Ground Current GND-pin		2	A
T_J	Operating Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC}	Power Supply Voltage	4.5	50	V
	Output Voltage Range DRAIN0 − DRAIN7	0	50	V
	Logic Low Voltage		0.9	V
	Logic High Voltage		1.5	V
	Continuous output current DRAIN0 − DRAIN7		500	mA
T_A	Operating Ambient Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	114.5	50.5	°C/W

Electrical Characteristics

All test conditions: V_{COM} = 12 V, T_A = −40 °C – 125 °C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{UVLO}	COM Under-voltage Lock-Out Threshold	Outputs off;	2.8	3.4	4.2	V
$R_{DS(on)}$	DRAIN0-DRAIN7 Output Drain-Source On-State Resistance	I_{OUTx} = 50 mA, V_{SUPPLY} = 4.5 V T_J = −40 °C – 125 °C		3	5.8	Ω
		I_{OUTx} = 100 mA, V_{SUPPLY} = 4.5 V T_J = −40 °C – 125 °C		3	5.9	
I_{DS-OFF}	Off-state Output Leakage Current	Outputs off; V_{DRAINx} = 12 V		10	500	nA
V_{OH}	High-level Output Voltage, SER OUT	I_{OH} = −20 μA	4.4	5.5	6.6	V
		I_{OH} = −4 mA	4.15	5.1	6.0	V
V_{OL}	Low-level Output Voltage, SER OUT	I_{OL} = 20 μA		0.005	0.01	V
		I_{OL} = 4 mA		0.3	0.5	V
V_{FWD}	Clamp Forward Voltage	I_F = 100 mA		325		mV
$I_{IN(ON)}$	High-Level Input Current	V_I = 5 V			20	μA
$I_{IN(OFF)}$	Low-Level Input Current	V_I = 0 V			−1	μA
I_{COM}	Quiescent Supply Current	Outputs off; V_{DRAINx} = 12 V		55	500	μA
I_{COM}	Active Supply Current	Outputs on; V_{DRAINx} = 0 V		122	500	μA
t_{pLH}	Propagation Delay Time, LOW to HIGH, from $\overline{G}$ to DRAINx	$V_{pull-up}$ = 12 V; $R_{pull-up}$ = 48Ω		350		ns
t_{pHL}	Propagation Delay Time, HIGH to LOW, from $\overline{G}$ to DRAINx	$V_{pull-up}$ = 12 V; $R_{pull-up}$ = 48Ω		350		ns
T_{OTP}	Thermal Shutdown Threshold	Outputs off;	150	165		°C

Typical Performance Characteristics

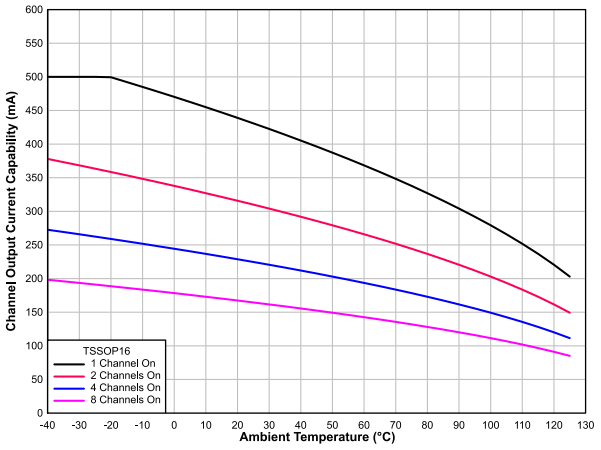
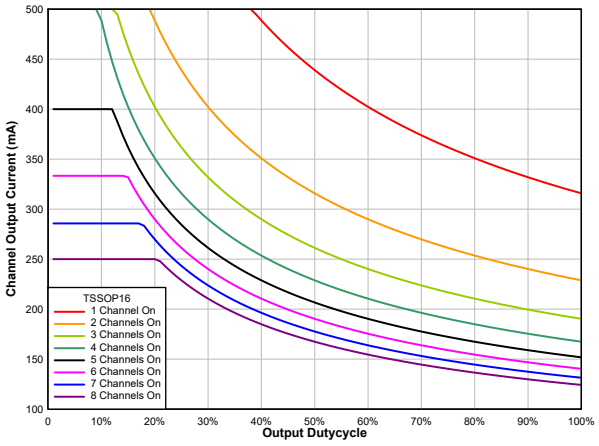


Figure 1. Output Current Capability vs. Ambient Temperature



T = 85 °C

Figure 2. Output Current Capability vs. Duty Cycle

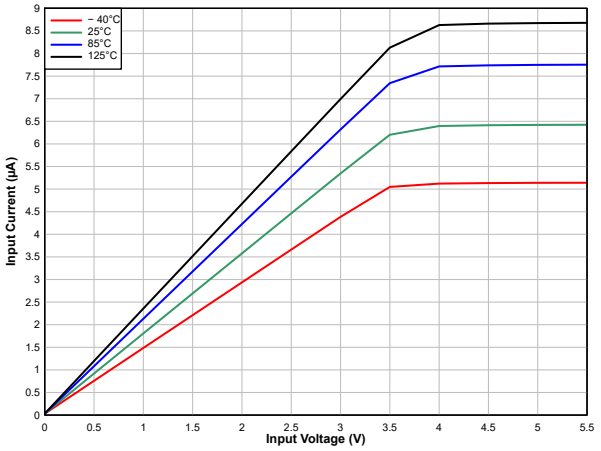


Figure 3. Input Current vs. Input Voltage

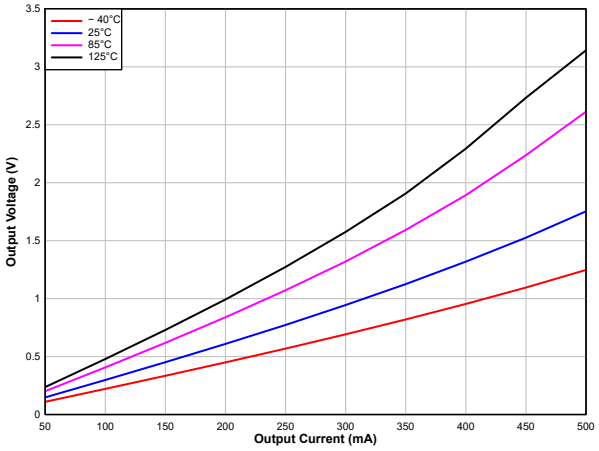


Figure 4. Output Voltage vs. Output Current

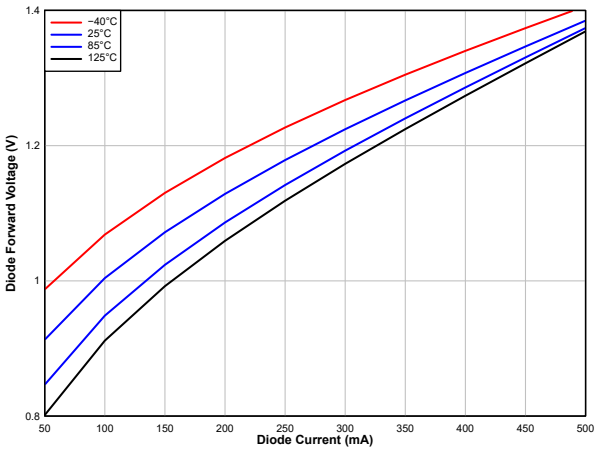


Figure 5. Output Diode Forward Voltage Drop vs. Diode Current

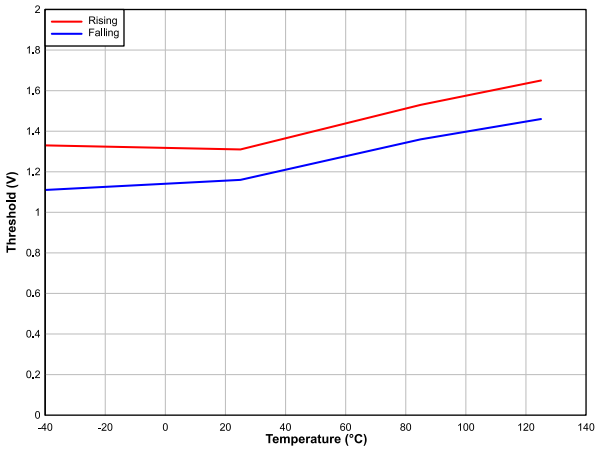


Figure 6. Input Threshold vs. Temperature

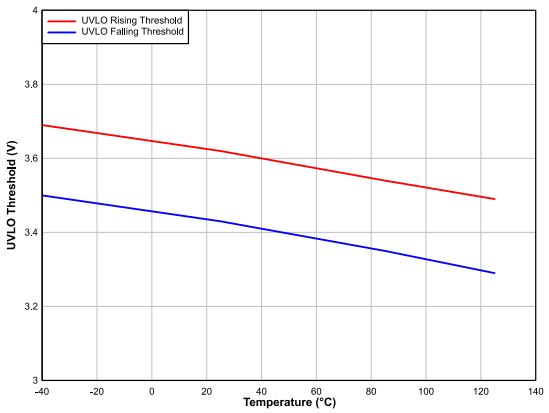
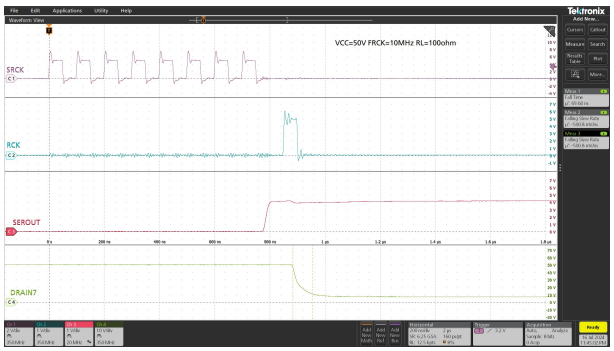


Figure 7. UVLO Threshold vs Temperature



f_{SCLK} = 10 MHz

Figure 8. Serial Interface Communication

Detailed Description

Overview

The TPM0596 is a high-voltage, high-current NMOS transistor array with a shift register interface. This device consists of eight channels of low-side NMOS transistors with high-voltage outputs and a free-wheeling diode for inductive loads.

The maximum drain-current rating of a single NMOS channel is 500 mA. The device supports a wide I/O voltage range from 1.8 V to 5 V. The transistors can be paralleled for higher current capability.

The TPM0596 can replace traditional bipolar Darlington arrays with better thermal efficiency and reliability and saves I/Os.

Functional Block Diagram

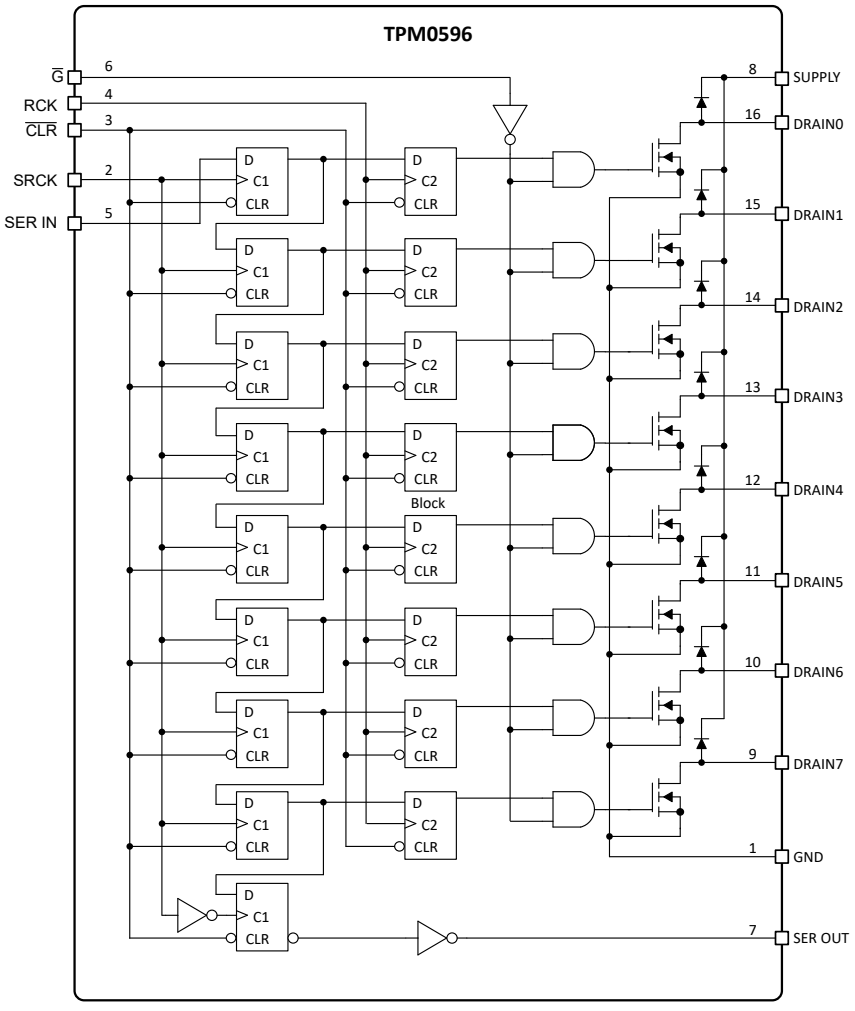


Figure 9. Functional Block Diagram

Device Thermal Capability

DRAIN0 to DRAIN7 drives loads with 100-Ω resistance and 1.36-mH inductance with 10-kHz frequency and 50% duty cycle. The top temperature of the package is measured as 58.9 °C.

Feature Description

The TPM0596 is an 8-ch low-side driver array. It consists of 8 channels of high-voltage low-side MOSFET. Its outputs can drive inductive loads up to 500 mA per channel with a wide temperature range. Its outputs can drive inductive loads, such as solenoids, relays, motors, and lamps up to 500 mA per channel with a wide temperature range. Multiple channels can be paralleled to increase driving capabilities or reduce thermal dissipation.

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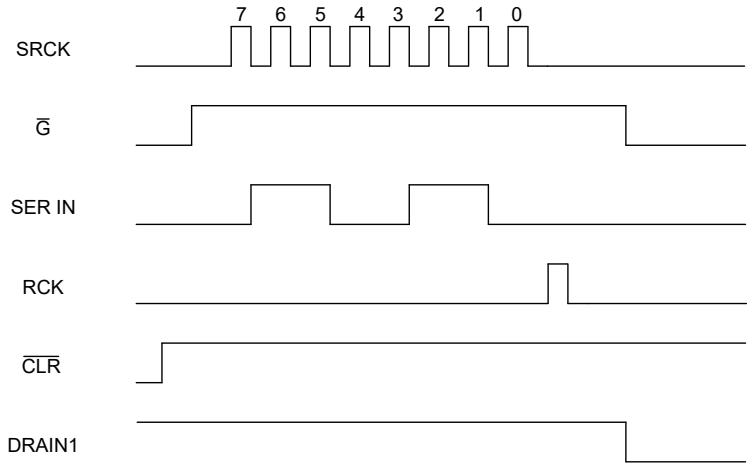
The device uses a serial shift register to control outputs. The shift register interface helps the system to save I/Os by using a minimal 3 pins only. The input pins support a wide range of voltage ratings from 1.8-V logic, and TTL logic up to 30-V voltage rail. With the integrated noise filter, the inputs improve system robustness in support robust industrial environment. The CMOS input gates can support modern microcontrollers without the need for current sourcing capabilities on microcontroller GPIOs.

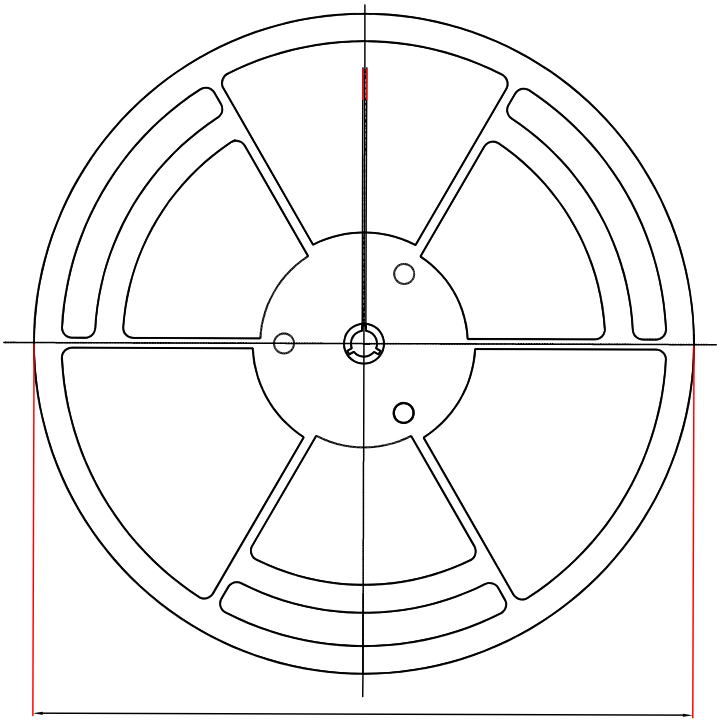
The minimal I/Os are SRCK, RCK, and SER IN. SER OUT is optional to read back the shift register values to improve system robustness. SER OUT needs an external pull-up resistor, 3PEAK recommends a 10-kΩ pull-up resistor. $\overline{G}$ is the output gating control input, setting $\overline{G}$ to low enables all outputs. $\overline{CLR}$ is the chip-level clear input. Setting $\overline{CLR}$ to low can clear the internal shift registers.

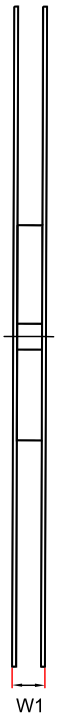
Integrated over-temperature protection and under-voltage lockout protection provide advanced robustness to the system compared to the older generation of Darlington arrays. The low on-resistance of output ensures lower power dissipated on the device. The low on-resistance increases driving efficiency and reduces device temperature, thus improving the system robustness.

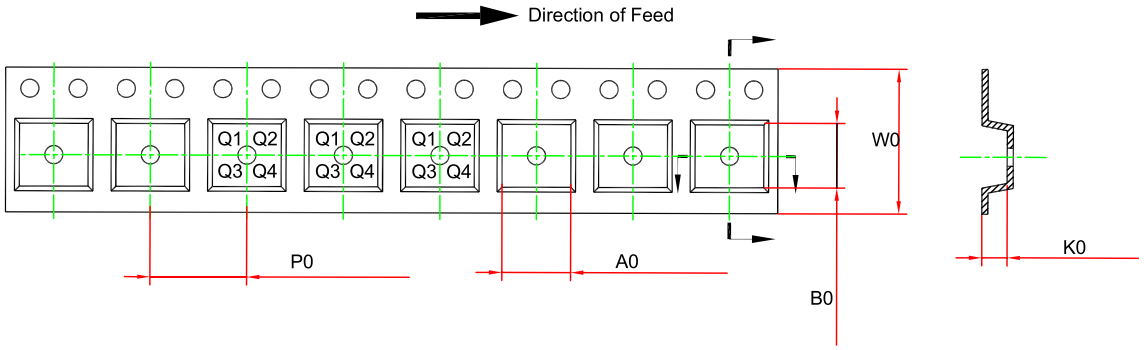
The device also supports a wide ambient temperature range (−40°C to 125°C)



Tape and Reel Information





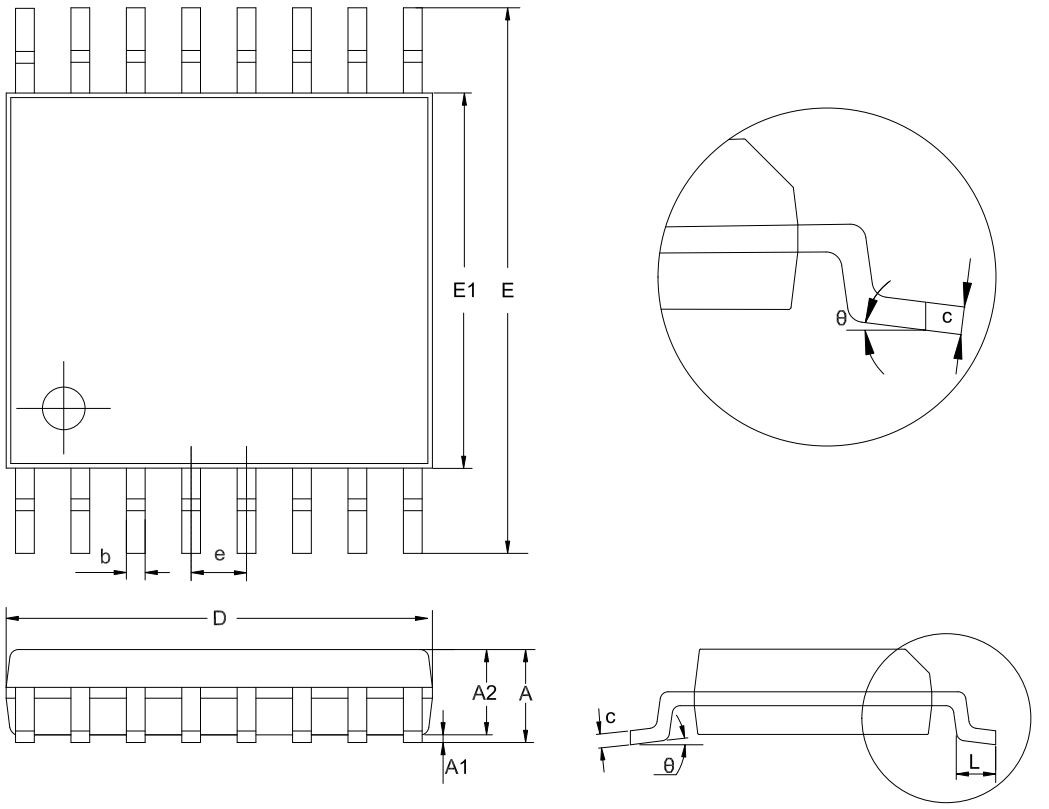


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM0596-TS3R	TSSOP16	330	17.6	6.8	5.5	1.3	8	12	Q1
TPM0596C-TS3R	TSSOP16	330	17.6	6.8	5.5	1.3	8	12	Q1
TPM0596C-QFNR	QFN3X3-16	330	17.6	3.3	3.3	1.1	8	12	Q2

Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



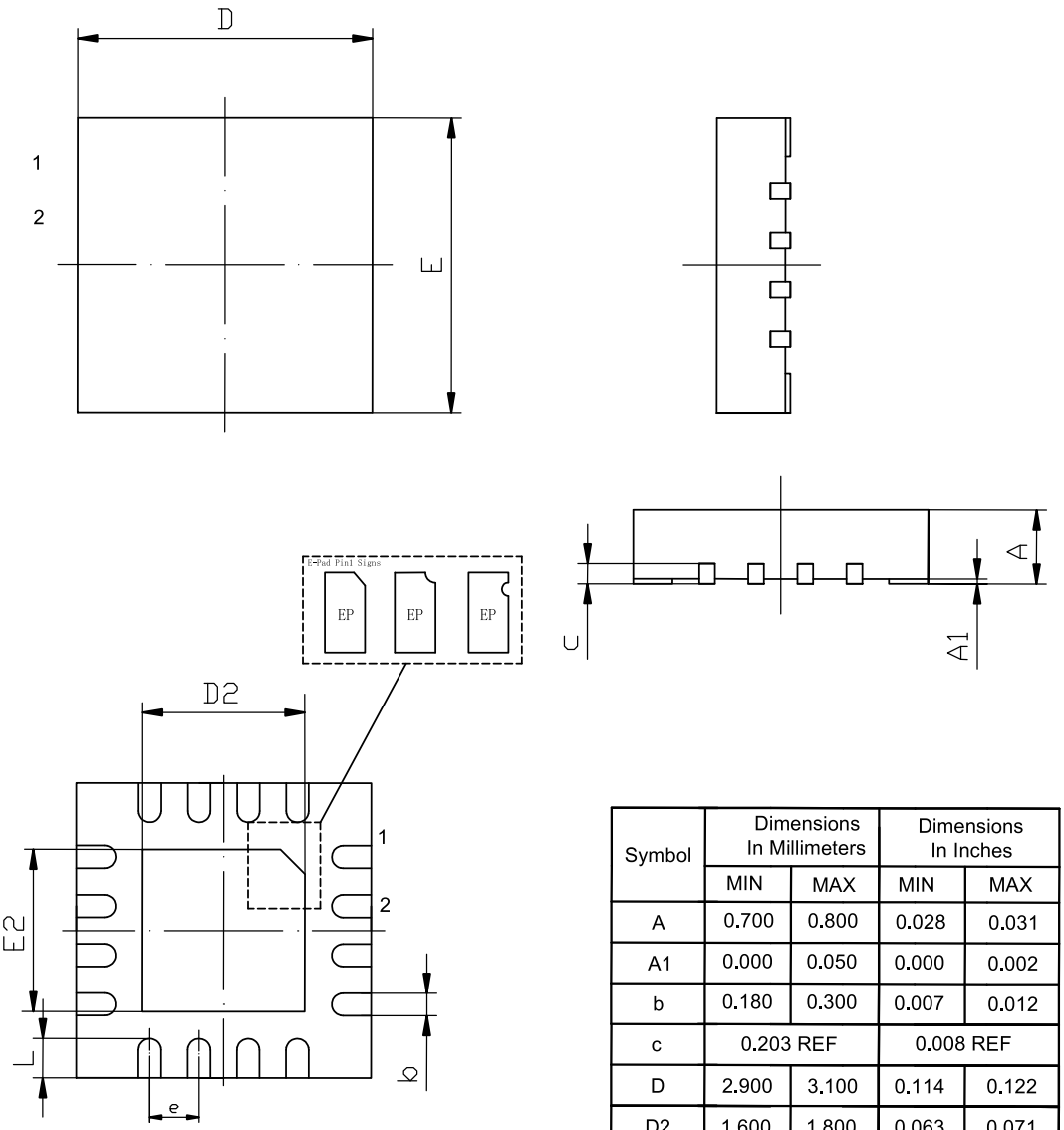
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

QFN3X3-16

Package Outline Dimensions QFN(QFN3X3-16-B)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D2	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E2	1.600	1.800	0.063	0.071
e	0.500 BSC		0.020 BSC	
L	0.250	0.500	0.010	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM0596-TS3R	−40 °C – 125 °C (1)	TSSOP16	M0596	MSL3	Tape & Reel, 3000	Green
TPM0596C-TS3R	−40 °C – 125 °C (1)	TSSOP16	0596C	MSL3	Tape & Reel, 3000	Green
TPM0596C-QFNR(2)	−40 °C – 125 °C (1)	QFN3X3-16	0596C	MSL3	Tape & Reel, 4000	Green

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios

(2) Contact 3PEAK representatives for more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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