

Features

- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® II Technology
- 100% Avalanche Tested, Rg 100% Tested

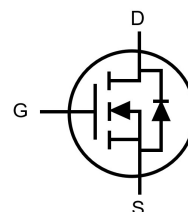
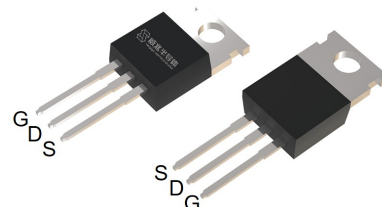


Halogen-Free

Part ID	Package Type	Marking	Packing
VS1602GTH	TO-220AB	1602GTH	50pcs/Tube

V_{DS}	100	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	3.6	mΩ
$I_D(\text{Wire bond limited})$	130	A

TO-220AB



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$	130	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	130	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	120	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	675	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	16	A
		$T_A = 70^\circ\text{C}$	12	A
EAS	Maximum Avalanche energy, single pulsed ②		484	mJ
PD	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	250	W
PDSM	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	2.1	W
T_J, T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.5	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
IDSS	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =100V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)⑦	V _{DS} =100V,V _{GS} =0V	--	--	100	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2.5	3	3.5	V
RDS(on)	Drain-Source On-State Resistance ⑧	V _{GS} =10V, I _D =40A	--	3.6	4.5	mΩ
		(T _j =100°C)⑦	--	4.7	--	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V _{DS} =50V,V _{GS} =0V, f=100KHz	--	5195	--	pF
Coss	Output Capacitance ⑦		--	875	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	30	--	pF
Rg	Gate Resistance	f=1MHz	--	1.8	--	Ω
Qg	Total Gate Charge ⑦	V _{DS} =50V,I _D =40A, V _{GS} =10V	--	91	--	nC
Qgs	Gate-Source Charge ⑦		--	25	--	nC
Qgd	Gate-Drain Charge ⑦		--	25	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	21	--	ns
Tr	Turn-on Rise Time		--	69	--	ns
Td(off)	Turn-Off Delay Time		--	57	--	ns
Tf	Turn-Off Fall Time		--	70	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
VSD	Forward on voltage	I _{SD} =40A,V _{GS} =0V	--	0.8	1.2	V
Trr	Reverse Recovery Time ⑦	I _{sd} =40A, V _{GS} =0V	--	59	--	ns
Qrr	Reverse Recovery Charge ⑦	di/dt=100A/μs	--	71	--	nC

NOTE:

- ① Single pulse; pulse width $\leq 100\mu\text{s}$.
- ② This maximum value is based on starting $T_j = 25^{\circ}\text{C}$, $L = 0.5\text{mH}$, $R_{\text{G}} = 25\Omega$, $I_{\text{AS}} = 44\text{A}$, $V_{\text{GS}}=10\text{V}$; 100% FT tested at $L = 0.5\text{mH}$, $I_{\text{AS}} = 22\text{A}$.
- ③ The power dissipation P_{d} is based on $T_j(\text{max})$, using junction-to-case thermal resistance $R_{\theta\text{JC}}$.
- ④ The power dissipation P_{dsm} is based on $T_j(\text{max})$, using junction-to-ambient thermal resistance $R_{\theta\text{JA}}$.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
- ⑥ The value of $R_{\theta\text{JA}}$ is measured with the device in a still air environment with $T_{\text{A}}=25^{\circ}\text{C}$.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width $\leq 380\mu\text{s}$; duty cycles $\leq 2\%$.

Typical Characteristics

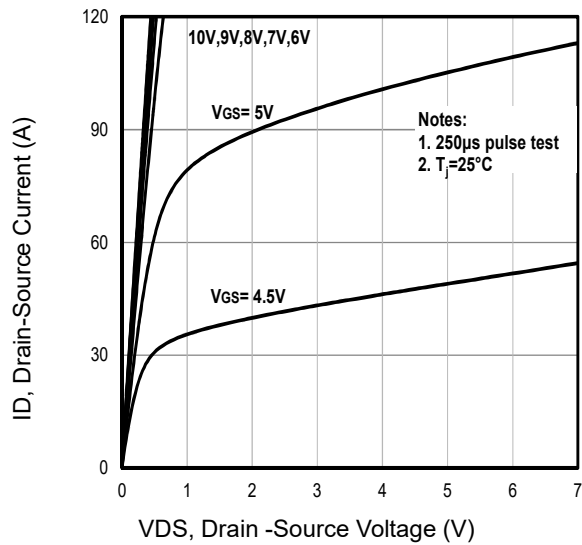


Fig1. Typical Output Characteristics

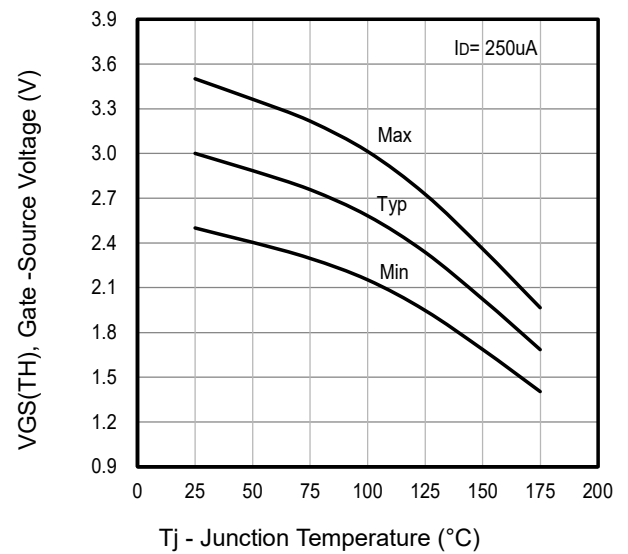


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

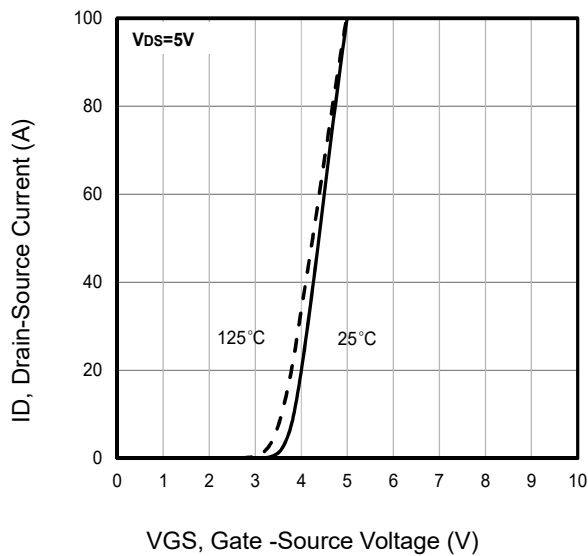


Fig3. Typical Transfer Characteristics

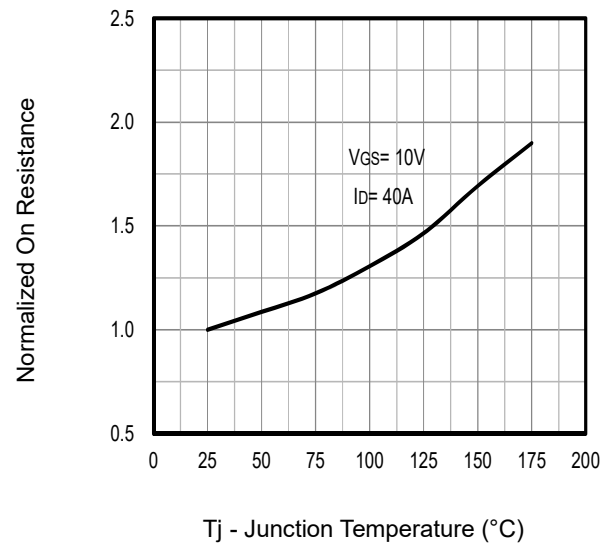


Fig4. Typical Normalized On-Resistance Vs. T_j

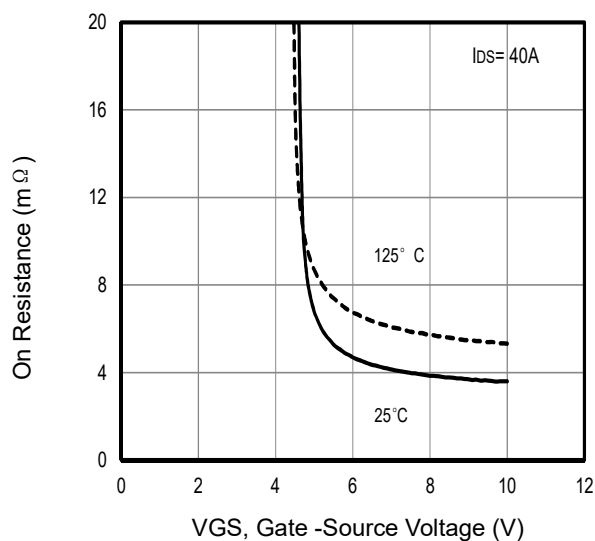


Fig5. Typical On Resistance Vs Gate-Source Voltage

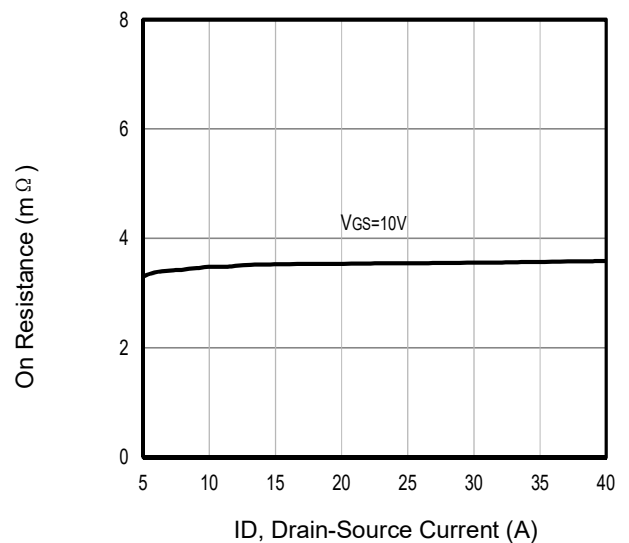


Fig6. Typical On Resistance Vs Drain Current and Gate

Typical Characteristics

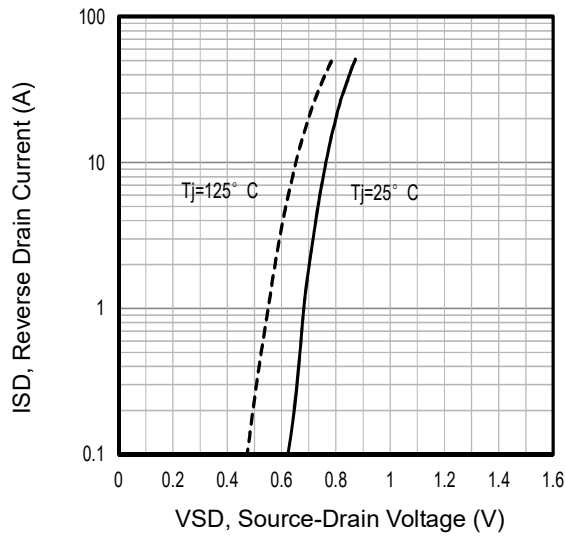


Fig7. Typical Source-Drain Diode Forward Voltage

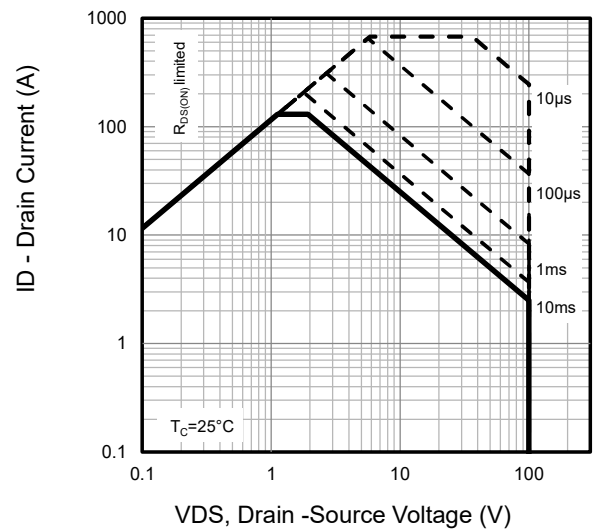


Fig8. Maximum Safe Operating Area

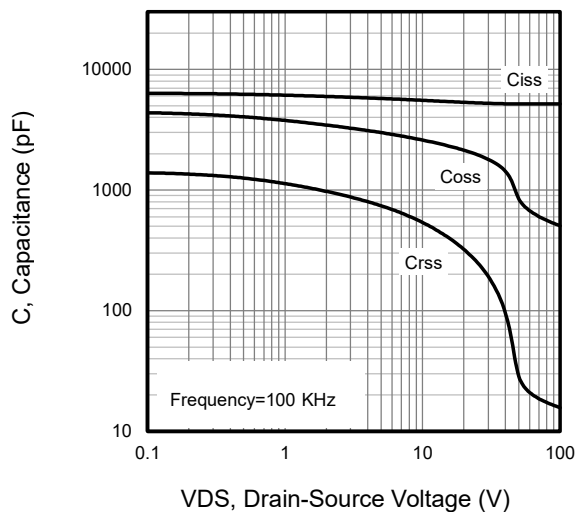


Fig9. Typical Capacitance Vs. Drain-Source Voltage

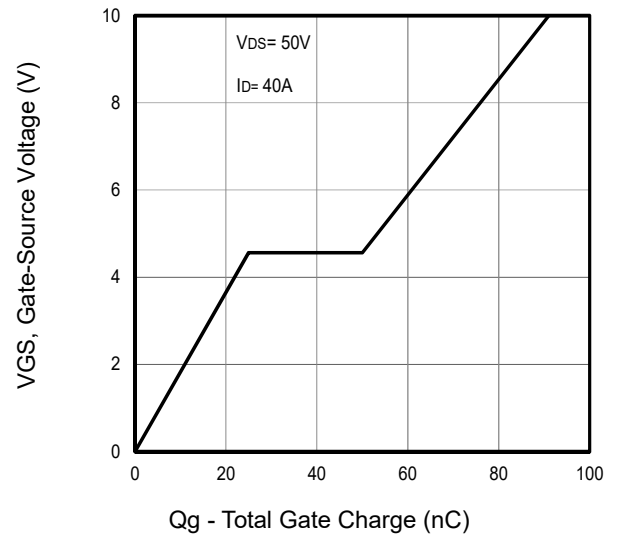


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

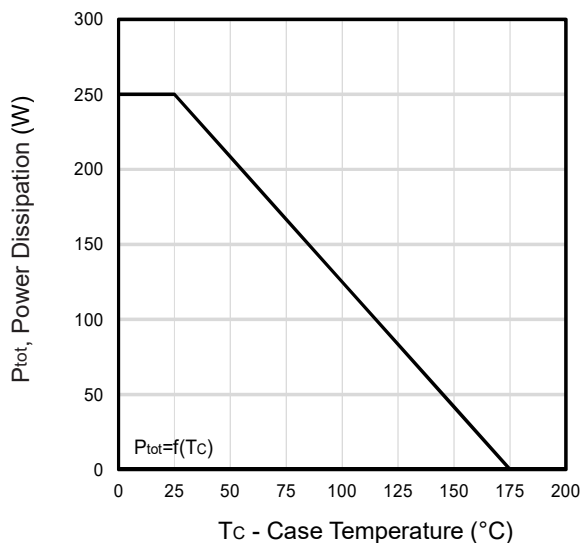


Fig11. Power Dissipation Vs. Case Temperature

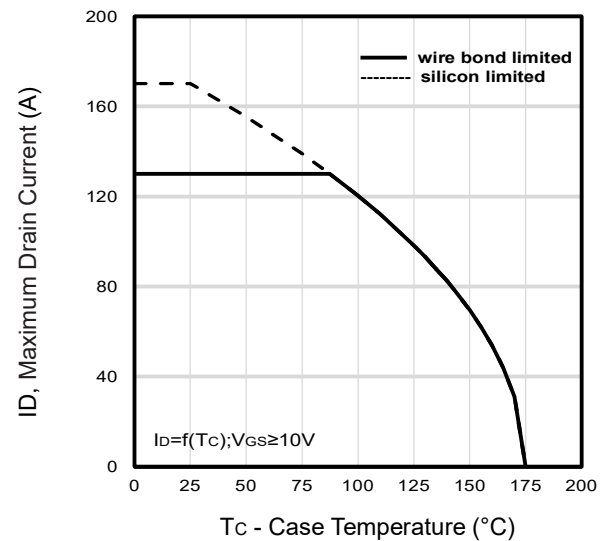


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

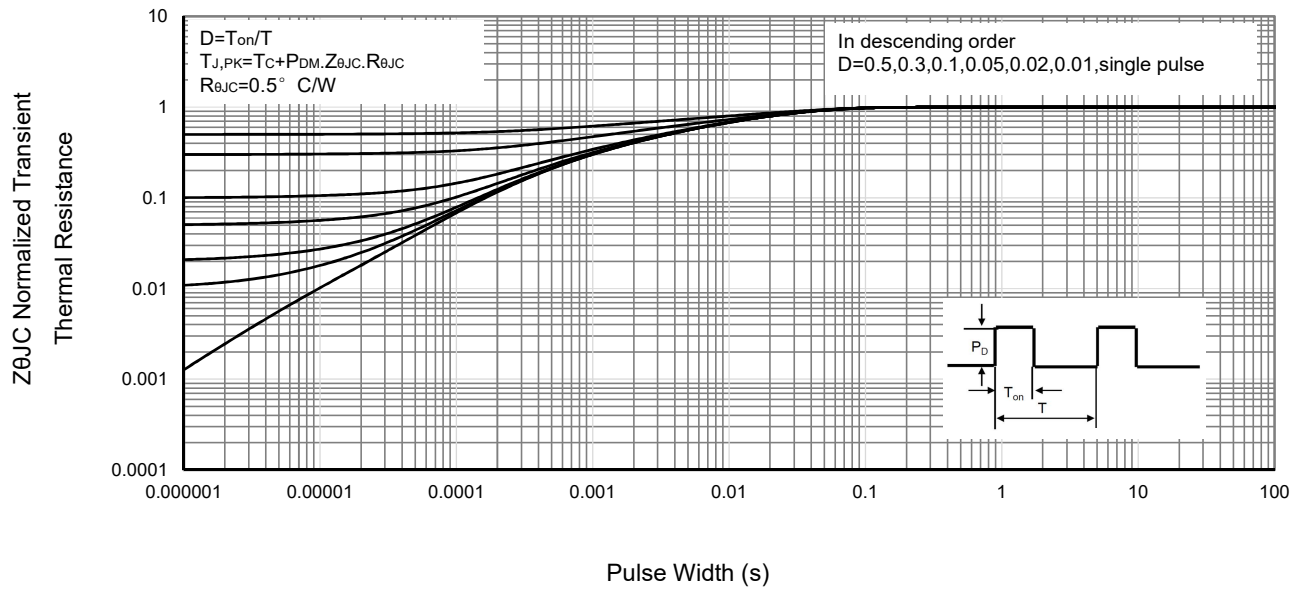


Fig13 . Normalized Maximum Transient Thermal Impedance

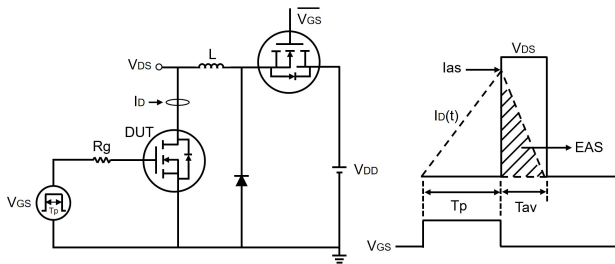


Fig14. Unclamped Inductive Test Circuit and waveforms

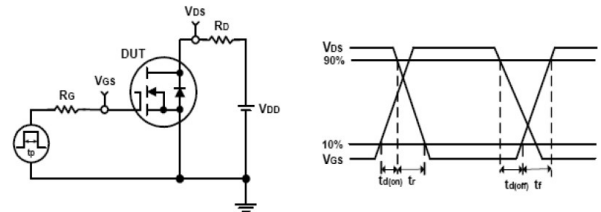
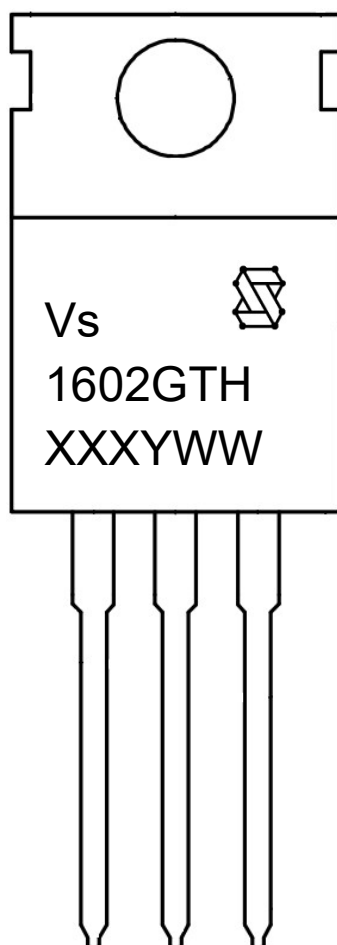


Fig15. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (1602GTH)

3rd line: Date code (XXXYWW)

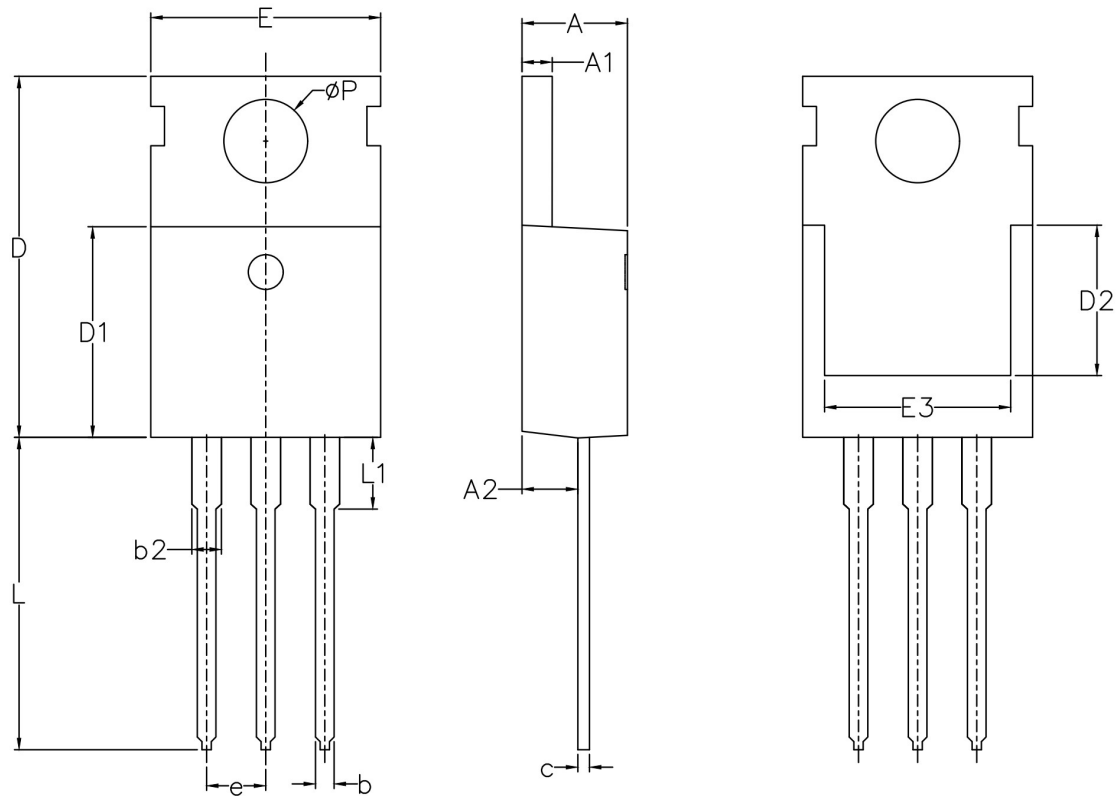
XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.35	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.27	1.47
c	0.45	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	--	--
E	9.70	10.00	10.30
E3	7.00	--	--
e	2.54 BSC		
L	12.75	13.50	13.85
L1	--	3.10	3.40
ϕP	3.40	3.60	3.80

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash.
Mold flash shall not exceed 0.127mm per side.
3. Thermal pad contour optional within dimensions E,H1,D2&E1.
4. Dimension E2&H1 define A zone where stamping and singulation irregularities are allowed.