

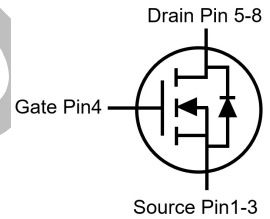
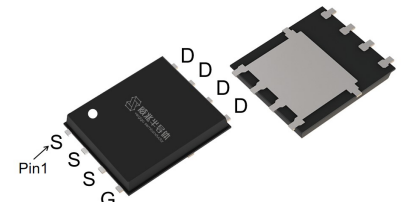
Features

- Enhancement mode
- VitoMOS® II Technology
- Ultra Low RDS(on) to minimize conduction losses
- 100% Avalanche Tested, 100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses



Halogen-Free

Part ID	Package Type	Marking	Packing
VS4896GPHT	PDFN5060X	4896GPHT	3000pcs/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
V(BR)DSS	Drain-source breakdown voltage		40	V
VGS	Gate-source voltage		±20	V
IS	Diode continuous forward current	T _C = 25°C	266	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T _C = 25°C	450	A
ID	Continuous drain current @VGS=10V (Silicon limited)	T _C = 100°C	285	A
IDM	Pulse drain current tested ①	T _C = 25°C	980	A
IDSM	Continuous drain current @VGS=10V	T _A = 25°C	45	A
		T _A = 70°C	36	A
EAS	Avalanche energy, single pulsed ②		1024	mJ
PD	Maximum power dissipation ③	T _C = 25°C	266	W
		T _C = 100°C	106	W
PDSM	Maximum power dissipation ④	T _A = 25°C	2.6	W
		T _A = 70°C	1.7	W
TJ,TSTG	Operating junction and storage temperature range		-55 to 150	°C

Thermal Characteristics

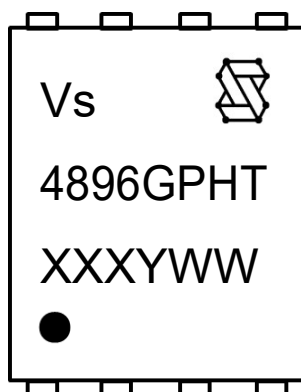
Symbol	Parameter	Typical	Max	Unit
RθJC	Thermal resistance, junction-to-case ⑤	0.39	0.47	°C/W
RθJA	Thermal resistance, junction-to-ambient ⑥	40	48	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250uA	40	--	--	V
I _{DSS}	Zero gate voltage drain current(T _j =25°C)	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _j =125°C)⑦	V _{DS} =40V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-body leakage current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} ,I _D =250μA	2.5	3	3.5	V
R _{DS(on)}	Drain-source on-state resistance ⑧	V _{GS} =10V, I _D =40A	--	0.6	0.8	mΩ
		(T _j =100°C)⑦	--	0.8	--	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	138	--	S
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ⑦	V _{DS} =20V,V _{GS} =0V, f=100kHz	--	8645	--	pF
C _{oss}	Output capacitance ⑦		--	2125	--	pF
C _{rss}	Reverse transfer capacitance ⑦		--	130	--	pF
R _g	Gate resistance	f=1MHz	--	3.1	--	Ω
Q _g	Total gate charge ⑦	V _{DS} =20V,I _D =40A, V _{GS} =10V	--	117	--	nC
Q _{gs}	Gate-source charge ⑦		--	34	--	nC
Q _{gd}	Gate-drain charge ⑦		--	16	--	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =20V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	13	--	ns
T _r	Turn-on rise time		--	73	--	ns
T _{d(off)}	Turn-off delay time		--	93	--	ns
T _f	Turn-off fall time		--	57	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A,V _{GS} =0V	--	0.77	1	V
T _{rr}	Reverse recovery time ⑦	V _{DD} =30V, I _{sd} =40A, V _{GS} =0V	--	54	--	ns
Q _{rr}	Reverse recovery charge ⑦	di/dt=100A/μs	--	52	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This value is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 64A, V_{GS} = 10V; 100% FT tested at L = 0.1mH, I_{AS} = 65A.
- ③ The power dissipation P_d is based on T_j(max), using junction-to-case thermal resistance RθJC.
- ④ The power dissipation P_{dsm} is based on T_j(max), using junction-to-ambient thermal resistance RθJA.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles 2%.

Marking Information


1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (4896GPHT)

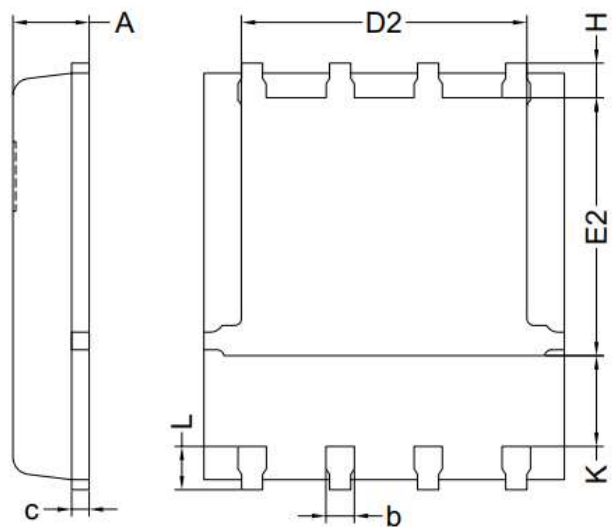
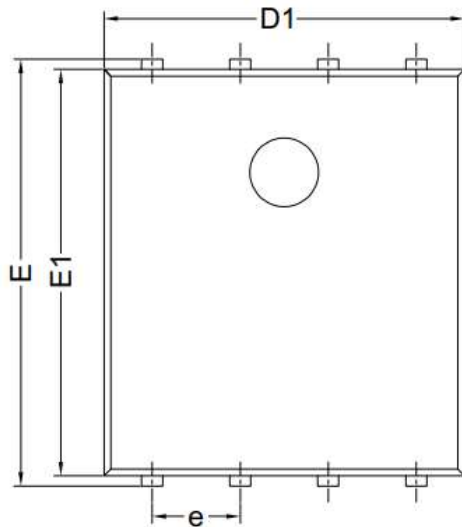
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5060X Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	1.00	1.10	1.20
b	0.33	0.40	0.50
c	0.20	0.25	0.30
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.27 BSC		
E	6.00	6.15	6.30
E1	5.76	5.86	5.96
E2	3.52	3.72	3.92
H	0.40	0.50	0.60
K	1.10	--	--
L	0.50	0.60	0.70

