



PJMG75DN40DN

Dual N-Channel Enhancement Mode Power MOSFET

Product Summary

- $V_{DS} = 40V, I_D = 75A$
- $R_{DS(on)} < 5m\Omega @ V_{GS} = 10V$
- $R_{DS(on)} < 7m\Omega @ V_{GS} = 4.5V$

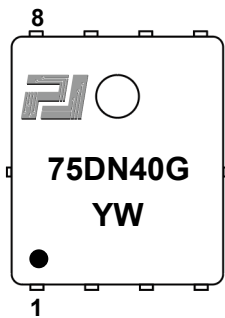
Features

- Advanced Split Gate Trench Technology
- 100% Avalanche Tested
- RoHS Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3

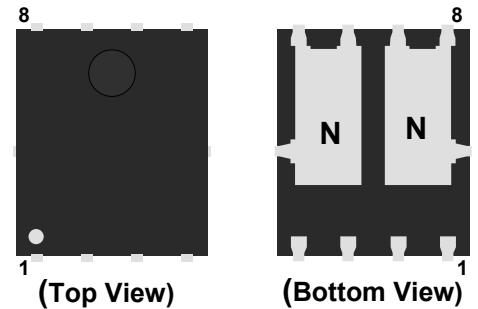
Application

- DC-DC Converter
- Power Switching Application

Marking Code

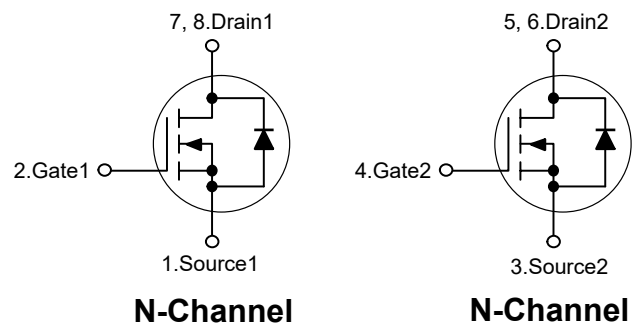


PDFN5x6A-8L



Pin	Description	Pin	Description
1	Source1	4	Gate2
2	Gate1	5,6	Drain2
3	Source2	7,8	Drain1

Schematic Diagram



Absolute Maximum Ratings

Ratings at 25°C case temperature unless otherwise specified.

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous	$T_C = 25^\circ C$	I_D	75	A
	$T_C = 100^\circ C$		48	
Drain Current-Pulsed ^{Note1}		I_{DM}	300	A
Maximum Power Dissipation		P_D	48	W
Single Pulse Avalanche Energy ^{Note2}		E_{AS}	100	mJ
Junction Temperature		T_J	150	$^\circ C$
Storage Temperature Range		T_{STG}	-55 to +150	$^\circ C$

Thermal Characteristics

Thermal Resistance, Junction-to-Case ^{Note3}	$R_{\theta JC}$	2.6	$^\circ C/W$
---	-----------------	-----	--------------



PJMG75DN40DN

Dual N-Channel Enhancement Mode Power MOSFET

Electrical Characteristics

(T_J=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V,I _D =250μA	40	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage ^{Note4}	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.5	2.5	V
Drain-Source On-Resistance ^{Note4}	R _{DS(on)}	V _{GS} =10V,I _D =15A	--	--	5	mΩ
		V _{GS} =4.5V,I _D =10A	--	--	7	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =20V,V _{GS} =0V,f=1MHz	--	1815	--	pF
Output Capacitance	C _{oss}		--	525	--	pF
Reverse Transfer Capacitance	C _{rss}		--	40	--	pF
Total Gate Charge	Q _g	V _{DS} =20V,I _D =20A, V _{GS} =10V	--	24	--	nC
Gate-Source Charge	Q _{gs}		--	3.5	--	nC
Gate-Drain Charge	Q _{gd}		--	4.5	--	nC
Switching Characteristics						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, I _D =20A, V _{GS} =10V, R _{GEN} =6Ω	--	5	--	nS
Turn-on Rise Time	t _r		--	9	--	nS
Turn-off Delay Time	t _{d(off)}		--	23	--	nS
Turn-off Fall Time	t _f		--	15.2	--	nS
Source-Drain Diode Characteristics						
Diode Forward Voltage ^{Note4}	V _{SD}	V _{GS} =0V,I _S =30A	--	--	1.2	V
Diode Forward Current	I _S		--	--	75	A

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. EAS Condition: T_J=25°C, V_{DD}=20V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=20A.

3. Surface mounted on 1inch² FR-4 board with 2OZ copper

4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Characteristic Curves

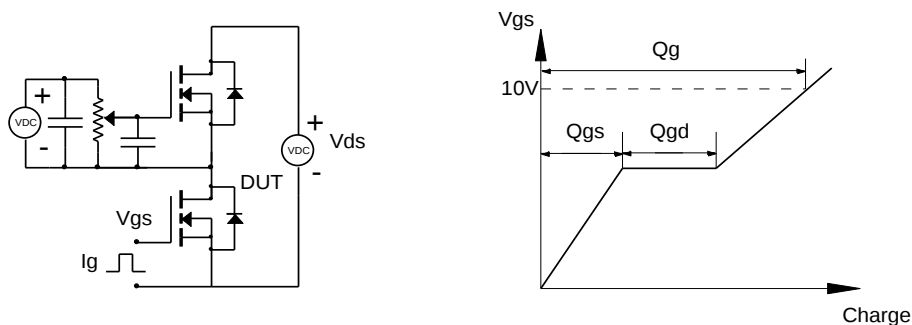


Figure 1: Gate Charge Test Circuit & Waveform

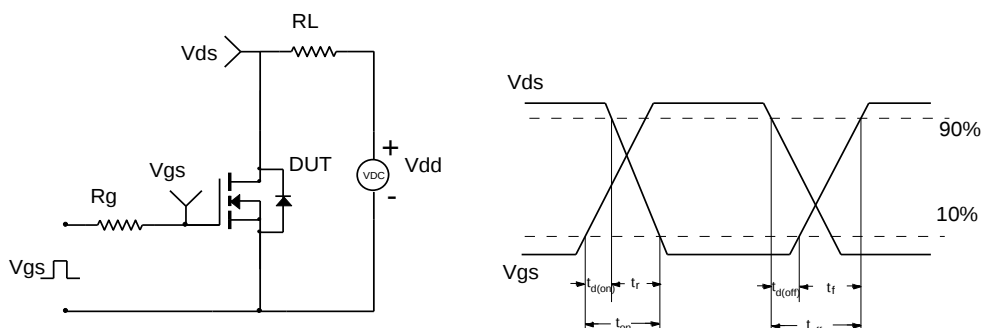


Figure 2: Resistive Switching Test Circuit & Waveform

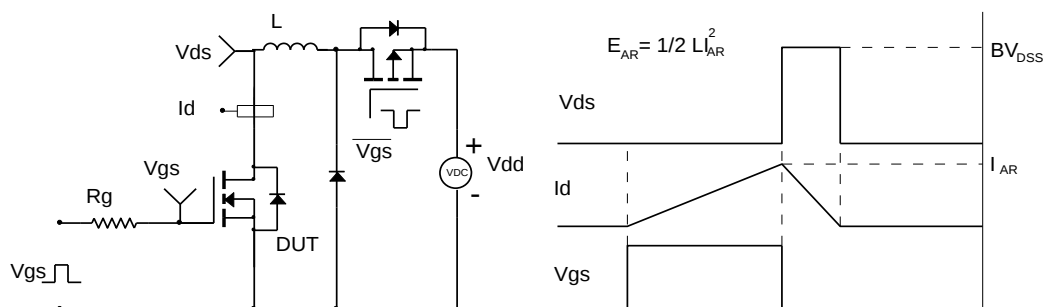


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

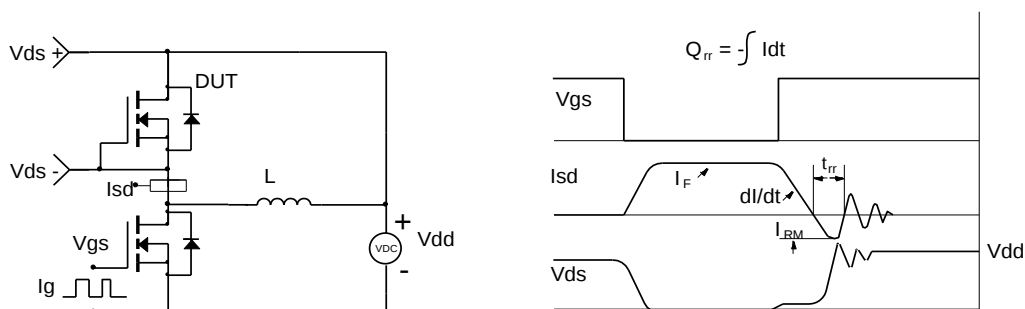


Figure 4: Diode Recovery Test Circuit & Waveform



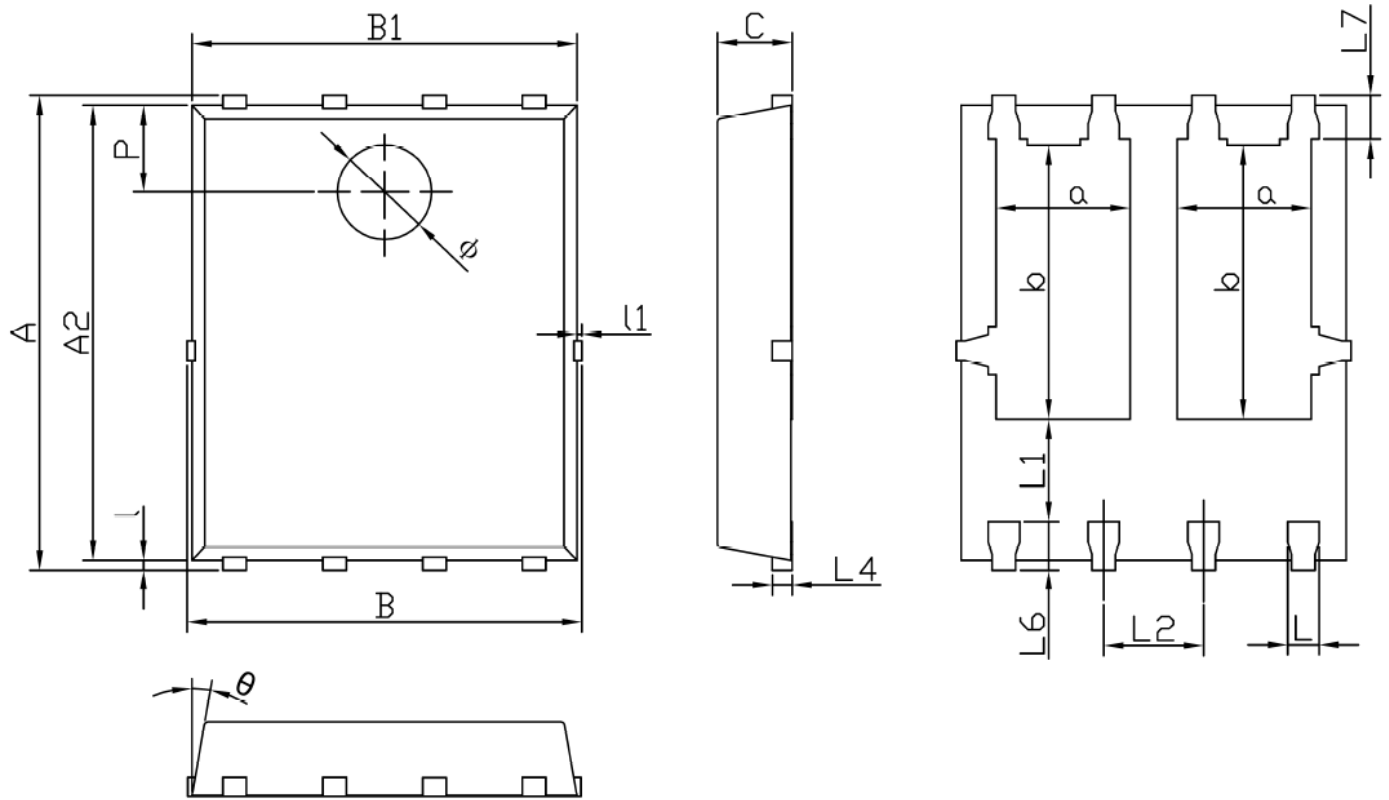
PJMG75DN40DN

Dual N-Channel Enhancement Mode Power MOSFET

Package Outline

PDFN5x6A-8L

Dimensions in mm



Symbol	Dimensions		Symbol	Dimensions	
	Min.	Max.		Min.	Max.
A	5.90	6.10	L1	1.10	-
a	1.605	1.805	l1	-	0.10
A2	5.70	5.80	L2	1.17	1.37
B	4.90	5.10	L4	0.21	0.34
b	3.375	3.575	L6	0.51	0.71
B1	4.80	5.00	L7	0.45	0.65
C	0.90	1.00	P	1.00	1.20
L	0.35	0.45	θ	8°	12°
l	0.06	0.20	Φ	1.10	1.30