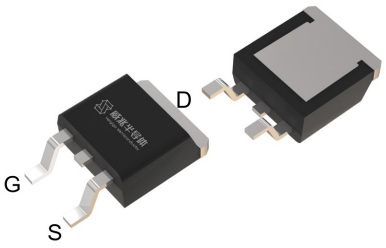
V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	1.8	mΩ
$I_{D(Wire\ bond\ limited)}$	195	A

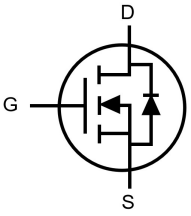
Features

- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® Ⅱ Technology
- 100% Avalanche tested,100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-263



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VS1893GMH	TO-263	1893GMH	800pcs/Reel

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		100	V
V_{GS}	Gate-source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C=25°C	195	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	195	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 100°C	173	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	980	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	23	A
		T_A=70°C	19	A
EAS	Maximum avalanche energy, single pulsed ②		812	mJ
P_D	Maximum power dissipation ③	T_C=25°C	283	W
		T_C=100°C	142	W
P_{DSM}	Maximum power dissipation ④	T_A=25°C	2.5	W
		T_A=70°C	1.8	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.44	0.53	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero gate voltage drain current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3.0	3.5	V
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=10V, I_D=40A	--	1.8	2.3	mΩ
		Tj=100℃ ⑦	--	2.6	--	mΩ
G_{FS}	Forward transconductance	V_{DS}=5V, I_D=40A	--	157	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=100kHz	--	7590	--	pF
Coss	Output capacitance ⑦		--	2795	--	pF
Crss	Reverse transfer capacitance ⑦		--	35	--	pF
Rg	Gate resistance	f=1MHz	--	2	--	Ω
Qg	Total gate charge ⑦	V_{DS}=50V,I_D=40A, V_{GS}=10V	--	111	--	nC
Qgs	Gate-source charge ⑦		--	35	--	nC
Qgd	Gate-drain charge ⑦		--	22	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay Time	V_{DD}=50V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	25	--	ns
Tr	Turn-on rise Time		--	58	--	ns
Td(off)	Turn-off delay Time		--	66	--	ns
Tf	Turn-off fall Time		--	51	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.81	1	V
Trr	Reverse recovery time ⑦	V_{DD}=50V I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	--	111	--	ns
Qrr	Reverse recovery charge ⑦		--	145	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 57A, V_{GS} =10V； 100% FT tested at L = 0.3mH, I_{AS} = 60A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.

⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

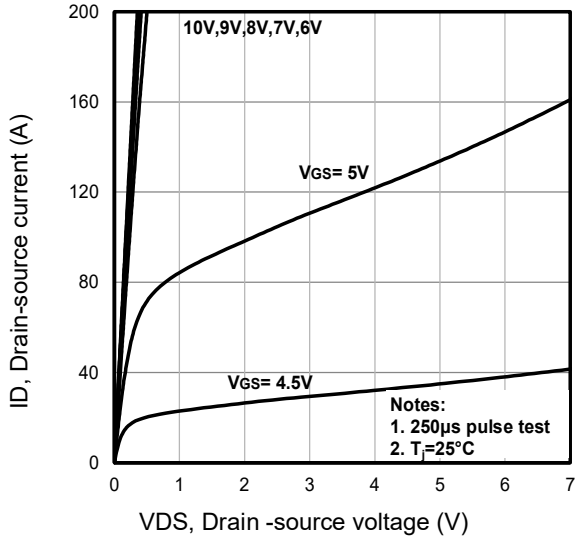


Fig1. Typical output characteristics

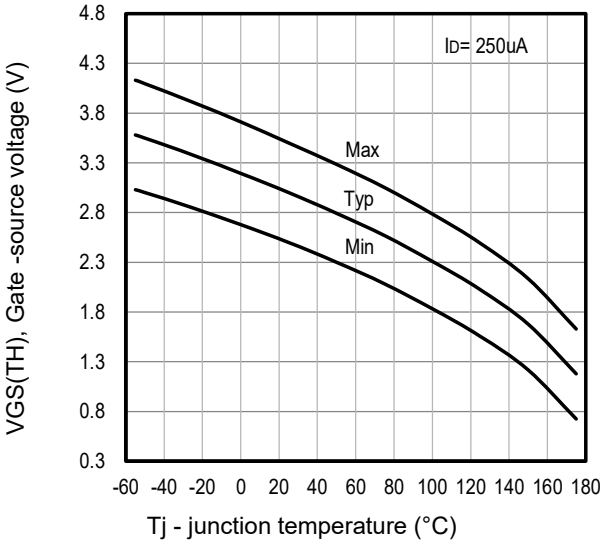


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

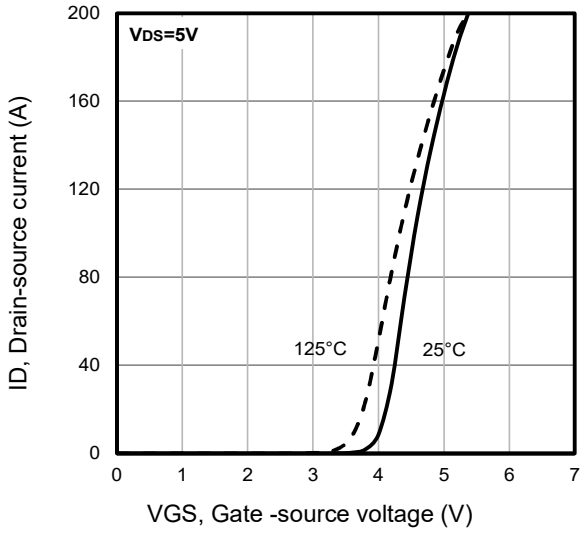


Fig3. Typical transfer characteristics

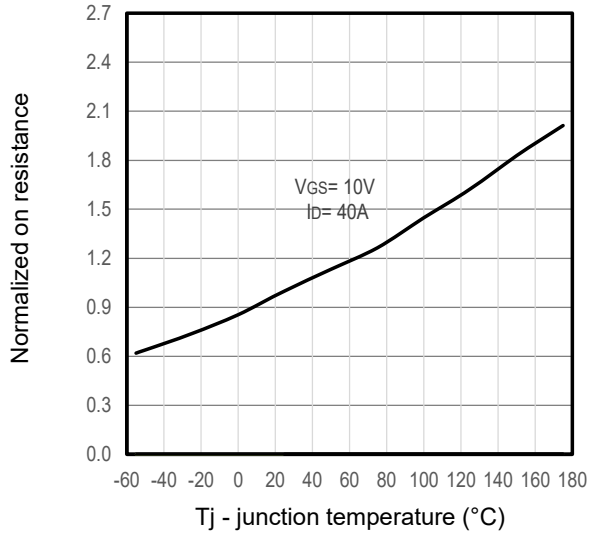


Fig4. Typical normalized on-resistance Vs. Tj

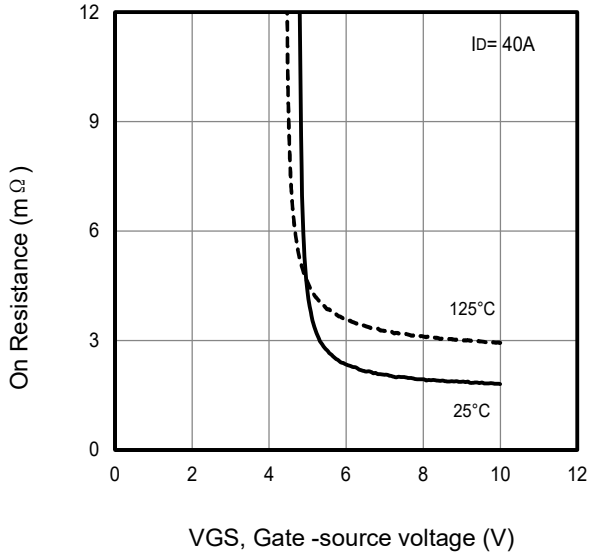


Fig5. Typical on resistance Vs gate -source voltage

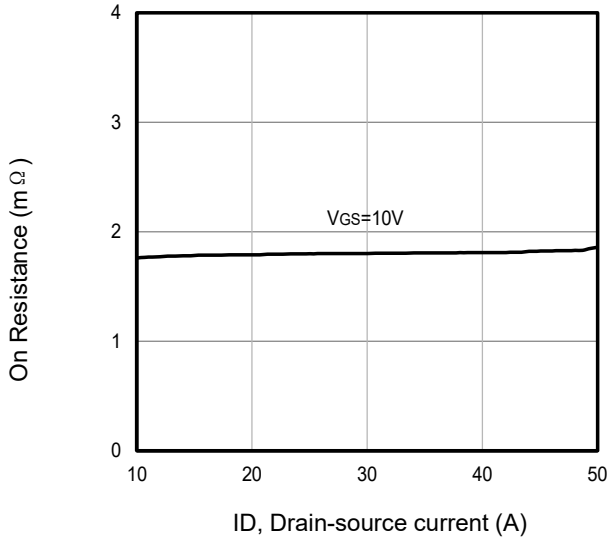


Fig6. Typical on resistance Vs drain current

Typical Characteristics

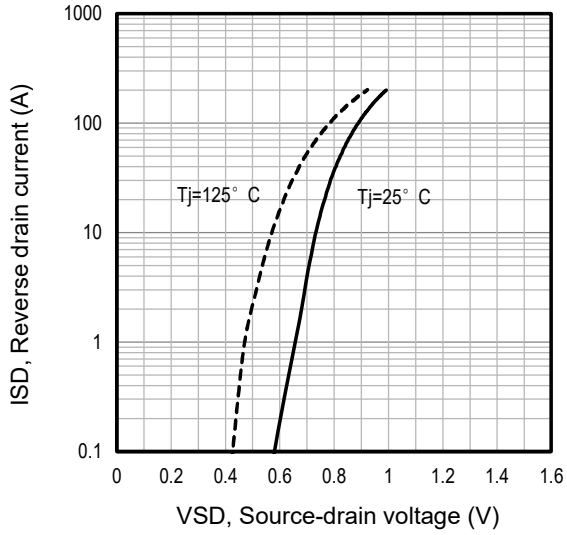


Fig7. Typical source-drain diode forward voltage

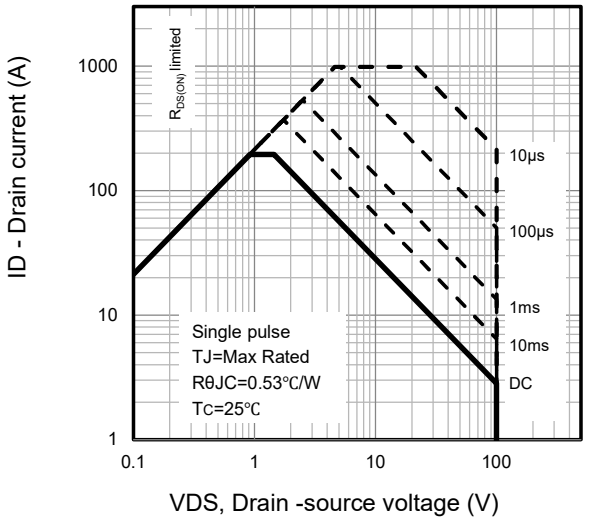


Fig8. Maximum safe operating area

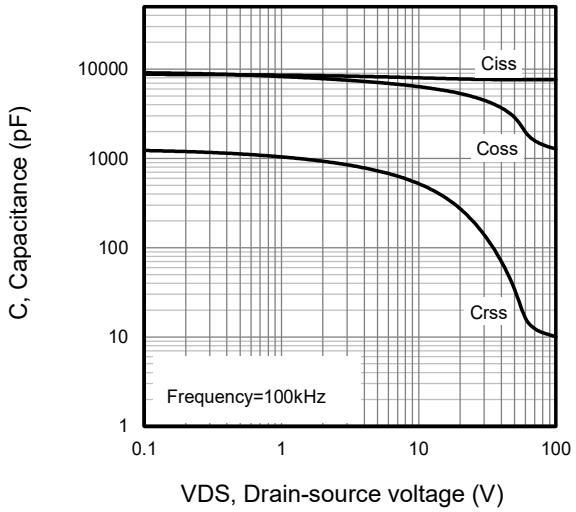


Fig9. Typical capacitance Vs. drain-source voltage

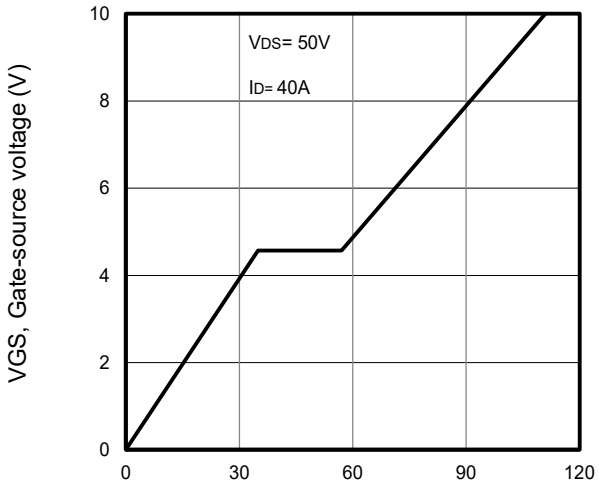


Fig10. Typical gate charge Vs. gate-source voltage

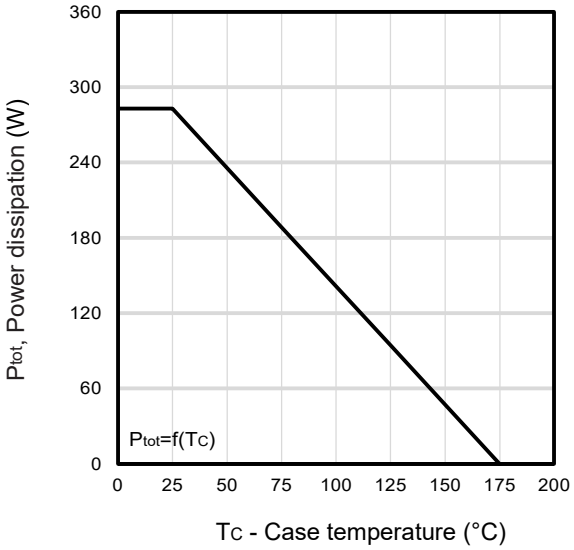


Fig11. Power dissipation Vs. case temperature

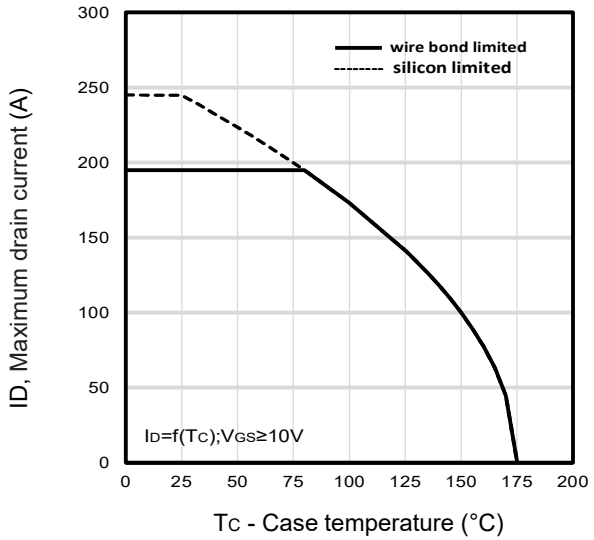


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

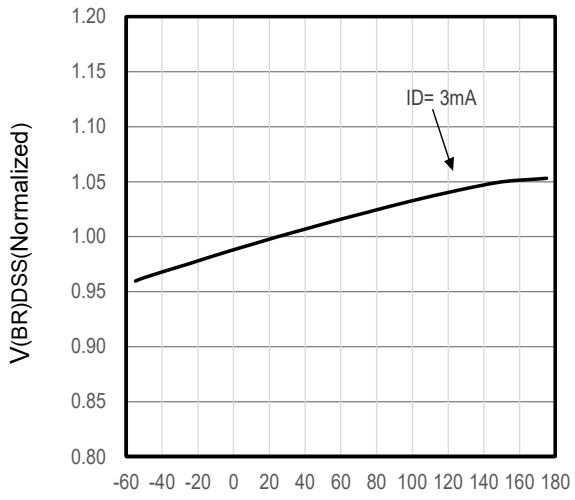


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

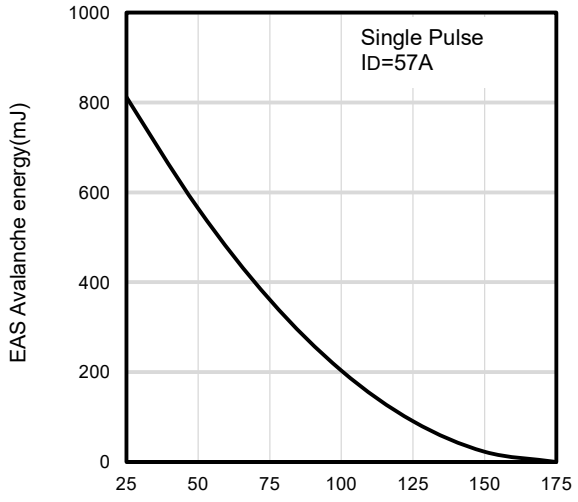


Fig14. Maximum avalanche energy vs temperature (°C)

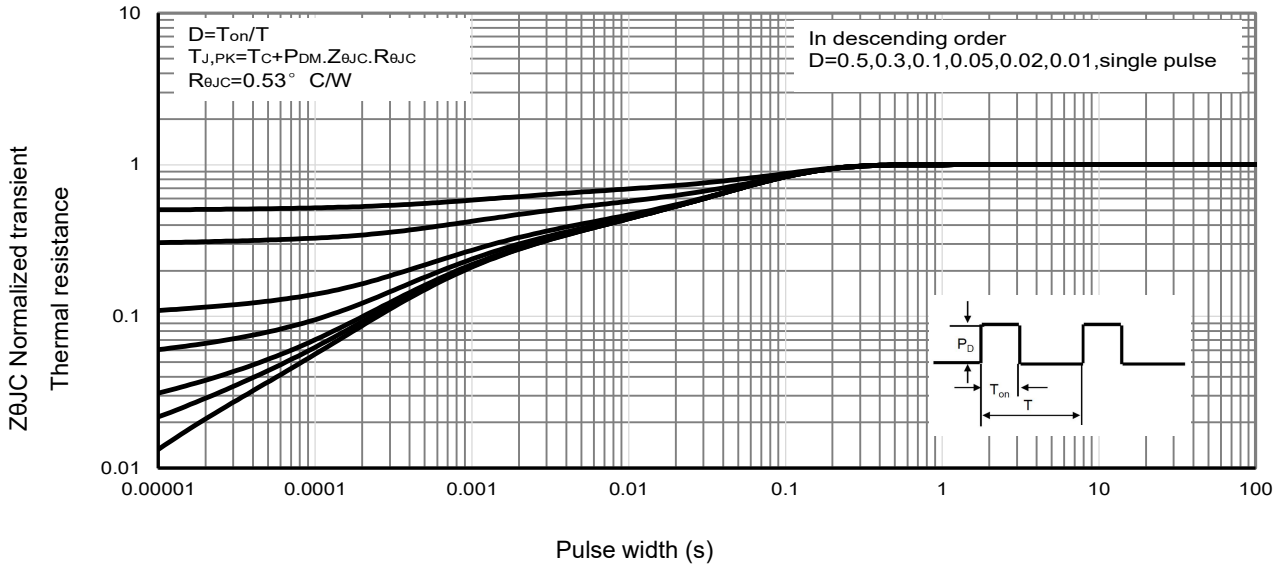


Fig15 . Normalized maximum transient thermal impedance

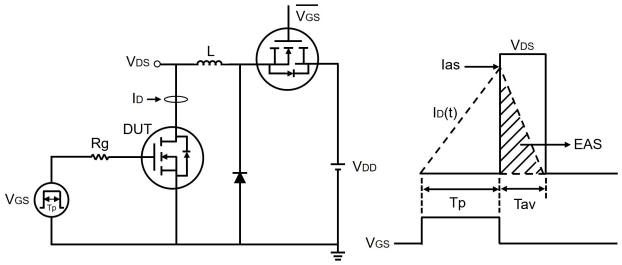


Fig16. Unclamped inductive test circuit and waveforms

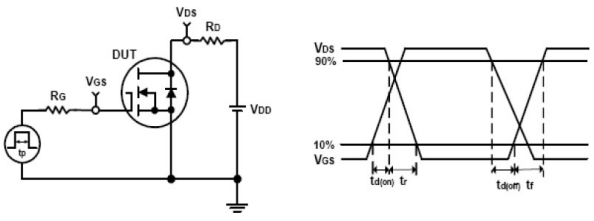
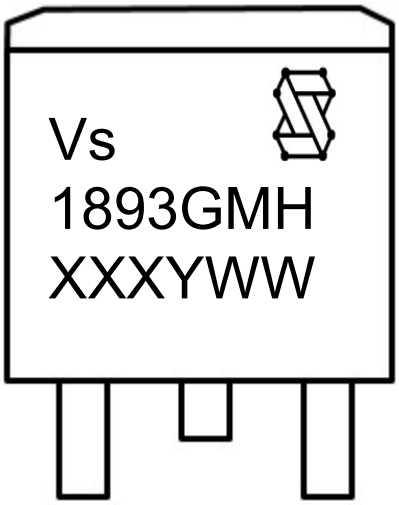


Fig17. Switching time test circuit and waveforms

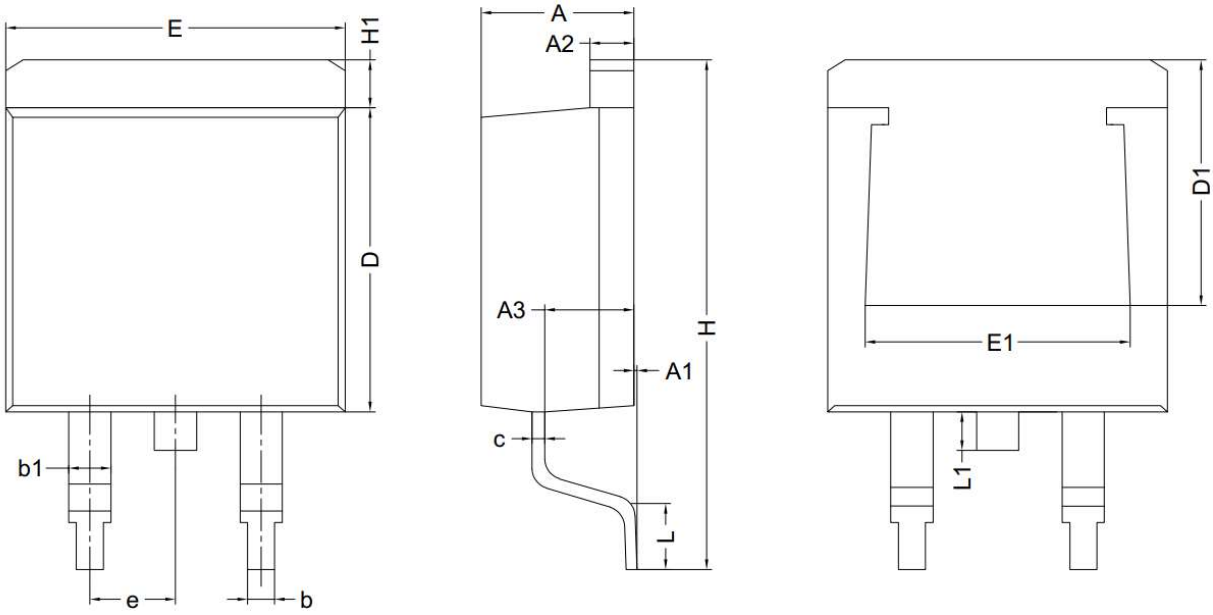
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（1893GMH）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code ， refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.42	4.52	4.62
A1	0.00	0.10	0.20
A2	1.24	1.27	1.32
A3	2.50	2.60	2.70
b	0.75	0.80	0.85
b1	1.20	1.25	1.30
c	0.33	0.38	0.43
D	8.88	9.00	9.12
D1	7.25 REF		
E	9.92	10.07	10.32
E1	7.85	8.00	8.15
e	2.50	2.54	2.58
H	14.80	15.10	15.30
H1	1.12	1.28	1.42
L	2.10	2.23	2.36
L1	1.10	1.30	1.50