

Features

- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® II Technology
- 100% Avalanche Tested, 100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

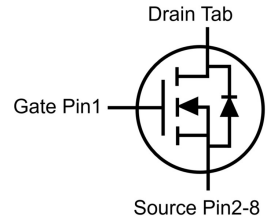
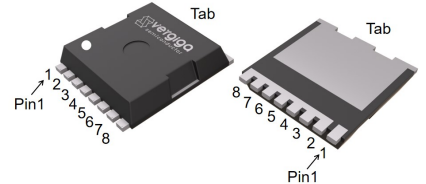


Halogen-Free

Part ID	Package Type	Marking	Packing
VS8801GKH	TOLL	8801GKH	2000PCS/Reel

V_{DS}	85	V
$R_{DS(on), TYP @ V_{GS}=10V}$	1.2	mΩ
I_D (Wire bond limited)	325	A

TOLL



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		85	V
V_{GS}	Gate-source voltage		± 20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$	325	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	325	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$	303	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	1230	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A=25^\circ\text{C}$	33	A
		$T_A=70^\circ\text{C}$	28	A
E_{AS}	Maximum avalanche energy, single pulsed ②		1681	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	577	W
		$T_C = 100^\circ\text{C}$	288	W
P_{DSM}	Maximum power dissipation ④	$T_A=25^\circ\text{C}$	3.5	W
		$T_A=70^\circ\text{C}$	2.4	W
T_J, T_{STG}	Operating junction and storage temperature range		-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.22	0.26	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	36	43	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J =25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250μA	85	95	--	V
I _{DSS}	Zero gate voltage drain current(T _J =25°C)	V _{DS} =85V,V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _J =125°C)⑦	V _{DS} =85V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-body leakage current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} ,I _D =250μA	2.5	3	3.5	V
R _{DS(on)}	Drain-source on-state resistance ⑧	V _{GS} =10V, I _D =80A	--	1.2	1.5	mΩ
		(T _J =100°C) ⑦	--	1.8	--	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	80	--	S
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ⑦	V _{DS} =40V,V _{GS} =0V, f=100kHz	--	11370	--	pF
C _{oss}	Output capacitance ⑦		--	2290	--	pF
C _{rss}	Reverse transfer capacitance ⑦		--	85	--	pF
R _g	Gate resistance	f=1MHz	--	2.4	--	Ω
Q _g	Total gate charge ⑦	V _{DS} =40V,I _D =80A, V _{GS} =10V	--	175	--	nC
Q _{gs}	Gate-source charge ⑦		--	55	--	nC
Q _{gd}	Gate-drain charge ⑦		--	41	--	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =40V, I _D =80A, R _G =3Ω, V _{GS} =10V	--	29	--	ns
T _r	Turn-on rise time		--	107	--	ns
T _{d(off)}	Turn-off delay time		--	90	--	ns
T _f	Turn-off fall time		--	60	--	ns
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =80A,V _{GS} =0V	--	0.83	1	V
T _{rr}	Reverse recovery time ⑦	V _{DD} =60V, I _{sd} =80A, V _{GS} =0V	--	84	--	ns
Q _{rr}	Reverse recovery charge ⑦	di/dt=100A/μs	--	127	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 82A, V_{GS}=10V; 100% FT tested at L = 0.5mH, I_{AS} = 56A.
- ③ The power dissipation P_d is based on T_J(max), using junction-to-case thermal resistance RθJC.
- ④ The power dissipation P_{dsM} is based on T_J(max), using junction-to-ambient thermal resistance RθJA.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

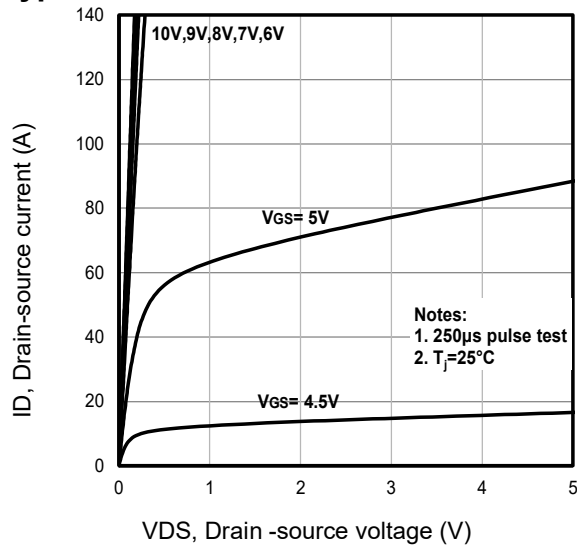


Fig1. Typical output characteristics

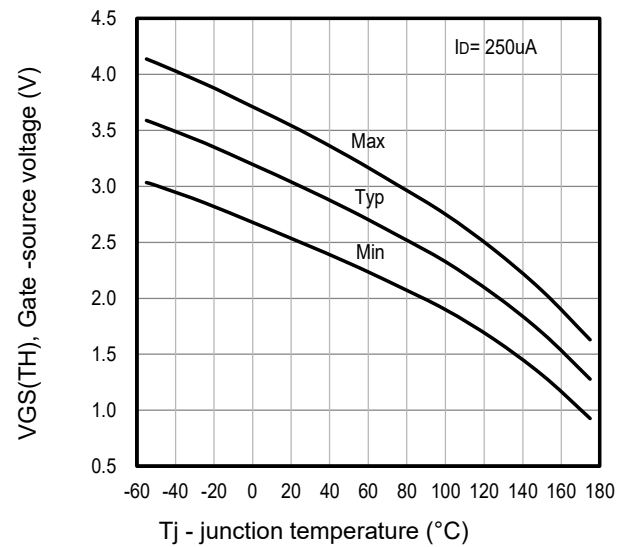


Fig2. Typical $V_{GS(TH)}$ gate-source voltage Vs. T_j

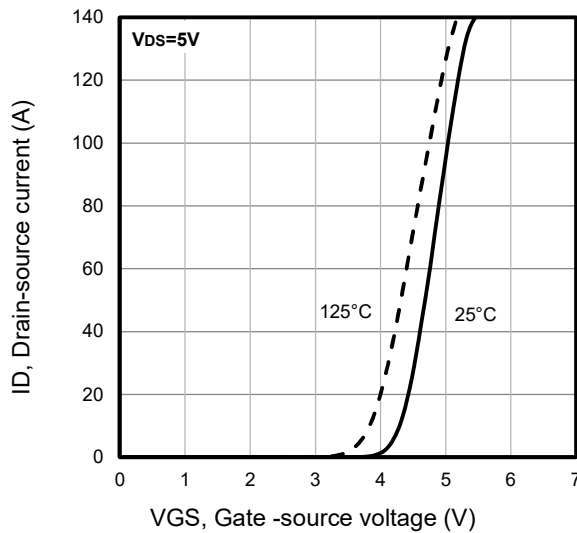


Fig3. Typical transfer characteristics

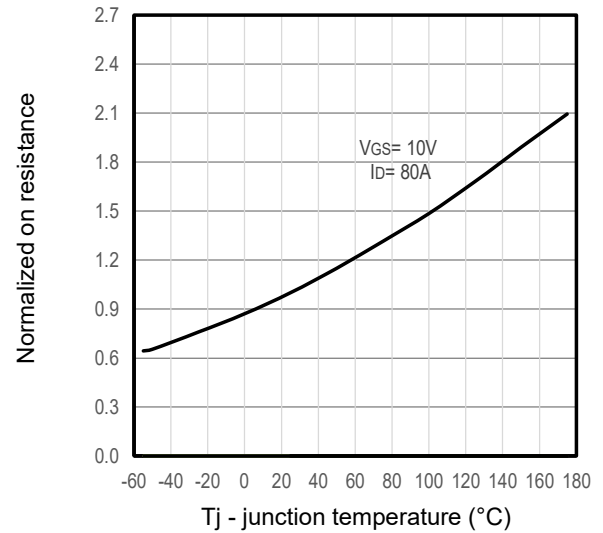


Fig4. Typical normalized on-resistance Vs. T_j

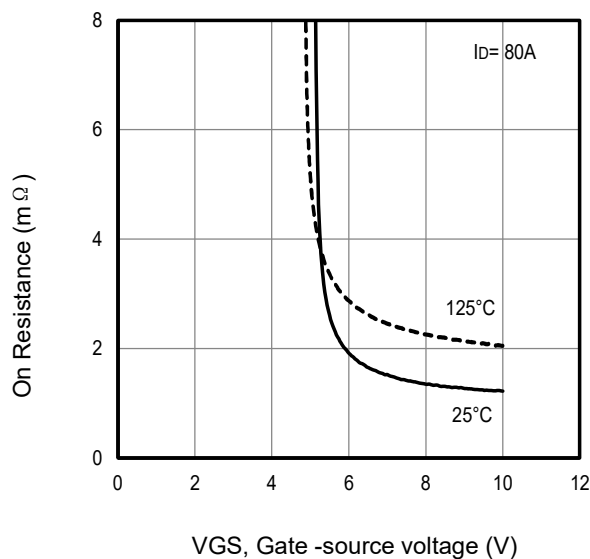


Fig5. Typical on resistance Vs gate-source voltage

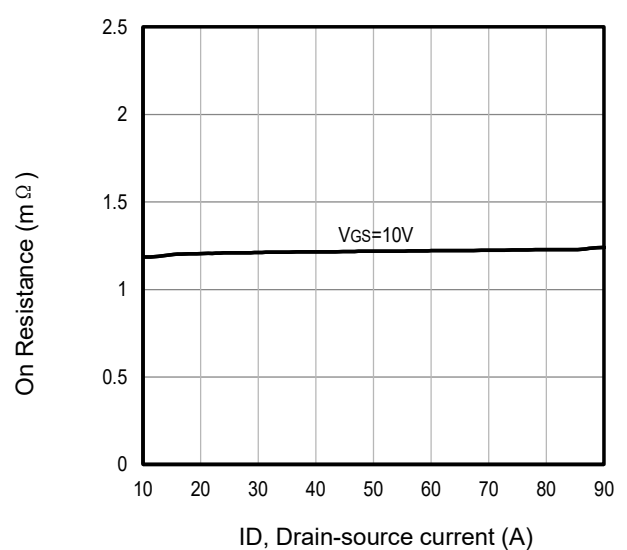


Fig6. Typical on resistance Vs drain current

Typical Characteristics

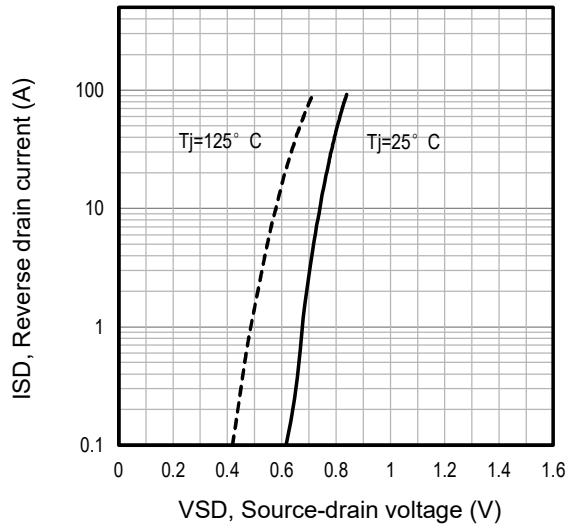


Fig7. Typical source-drain diode forward voltage

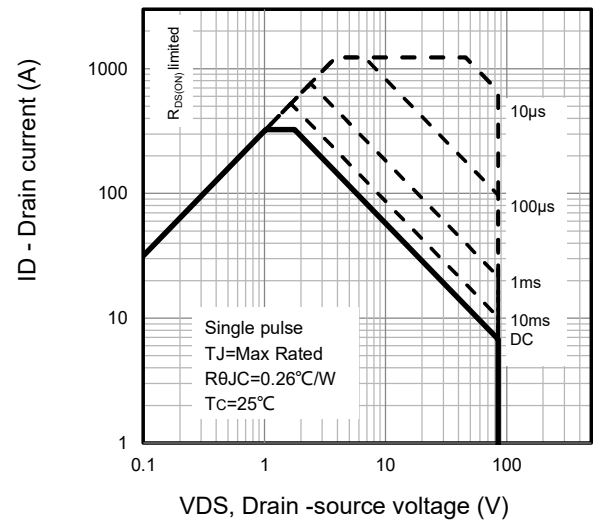


Fig8. Maximum safe operating area

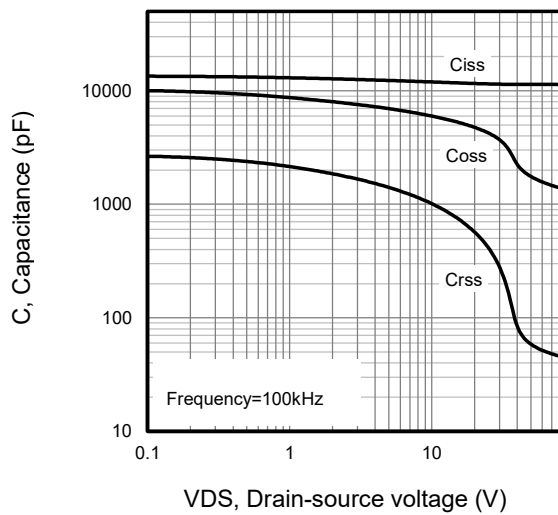


Fig9. Typical capacitance Vs. drain-source voltage

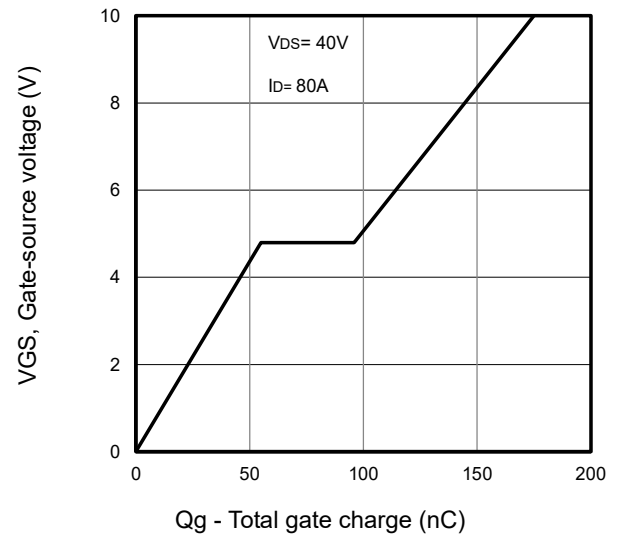


Fig10. Typical gate charge Vs. gate-source voltage

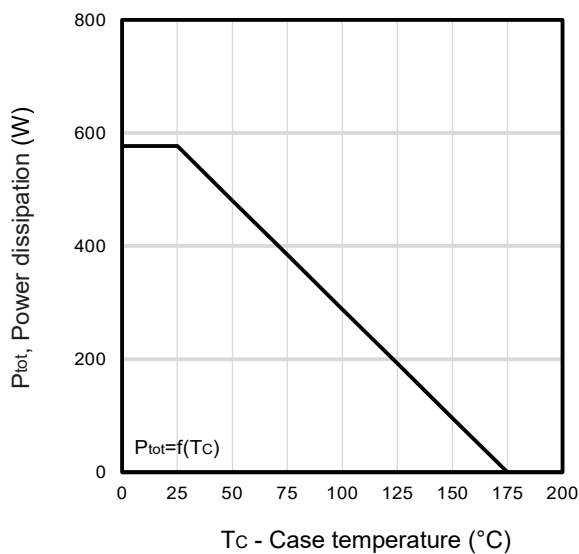


Fig11. Power dissipation Vs. case temperature

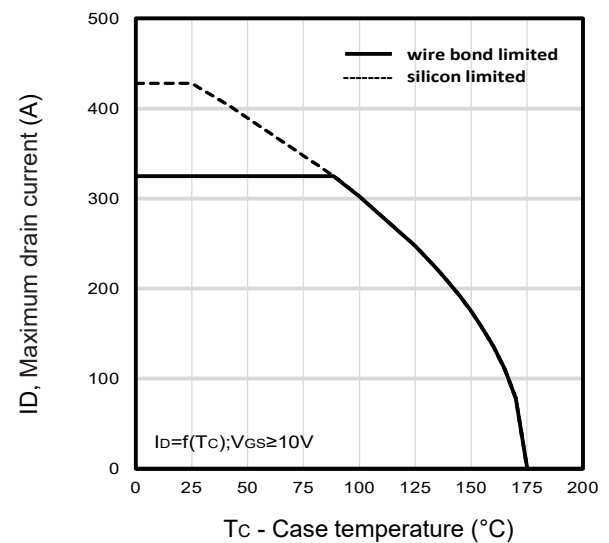
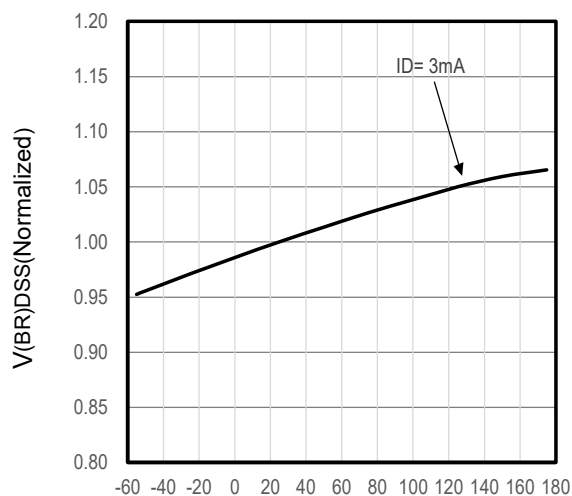


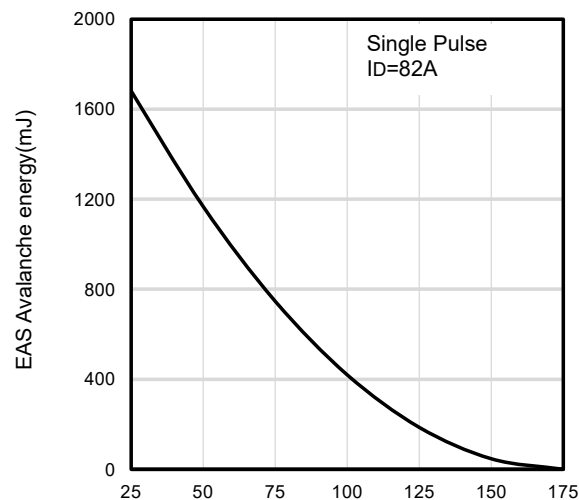
Fig12. Maximum drain current Vs. case temperature

Typical Characteristics



Tj - Junction temperature (°C)

Fig13. Typical V(BR)DSS Vs Tj



Starting Tj junction temperature (°C)

Fig14. Maximum avalanche energy vs temperature (°C)

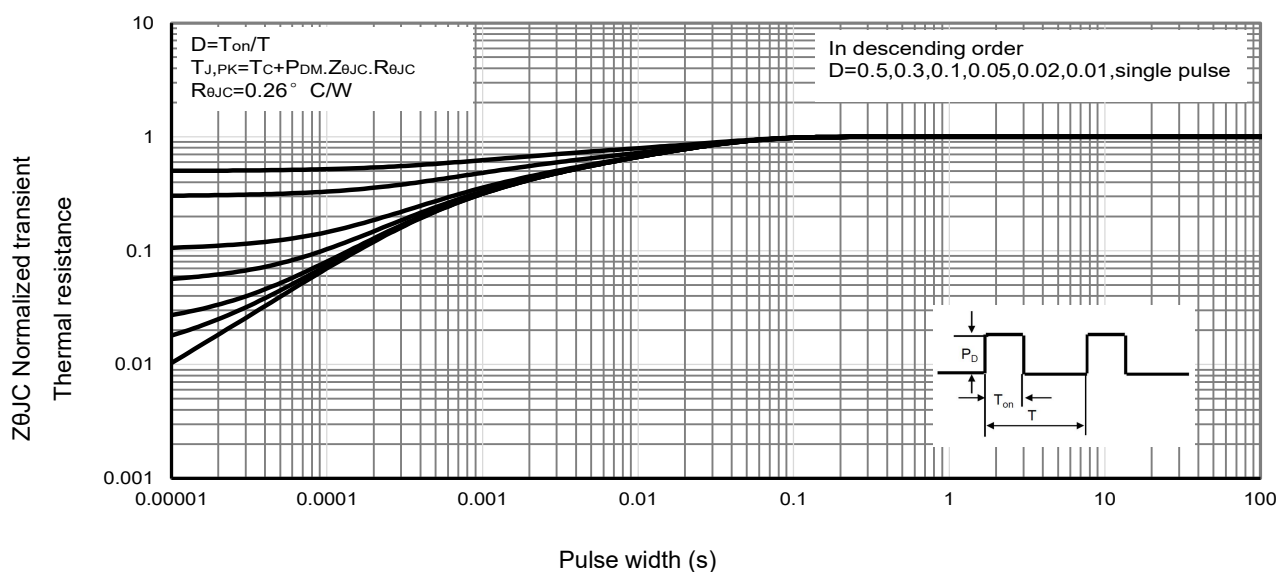


Fig15 . Normalized maximum transient thermal impedance

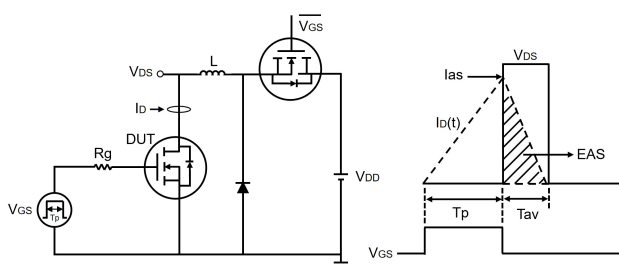


Fig16. Unclamped inductive test circuit and waveforms

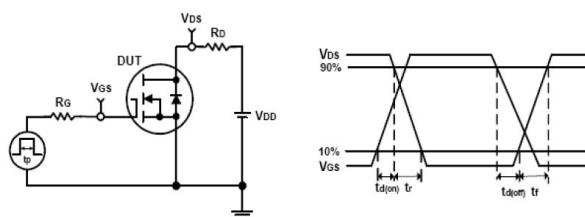
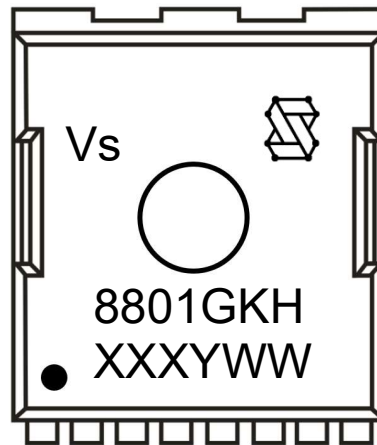


Fig17. Switching time test circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (8801GKH)

3rd line: Date code (XXXYWW)

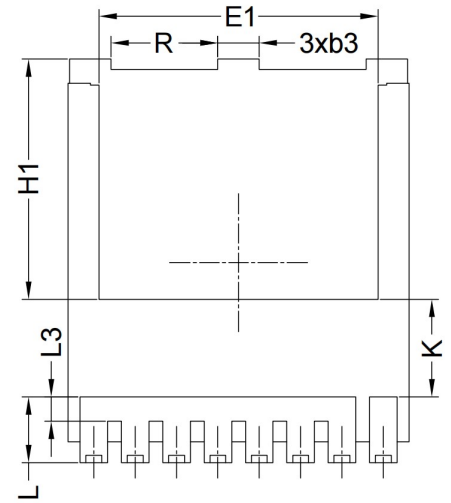
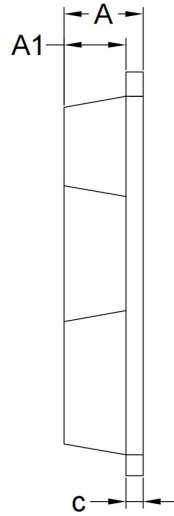
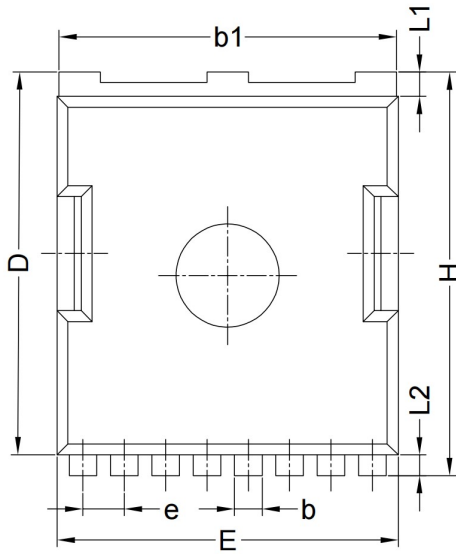
XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

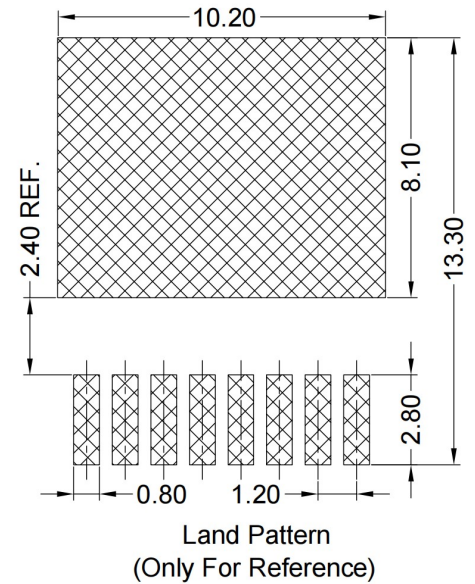
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TOLL Package Outline Data(for M)



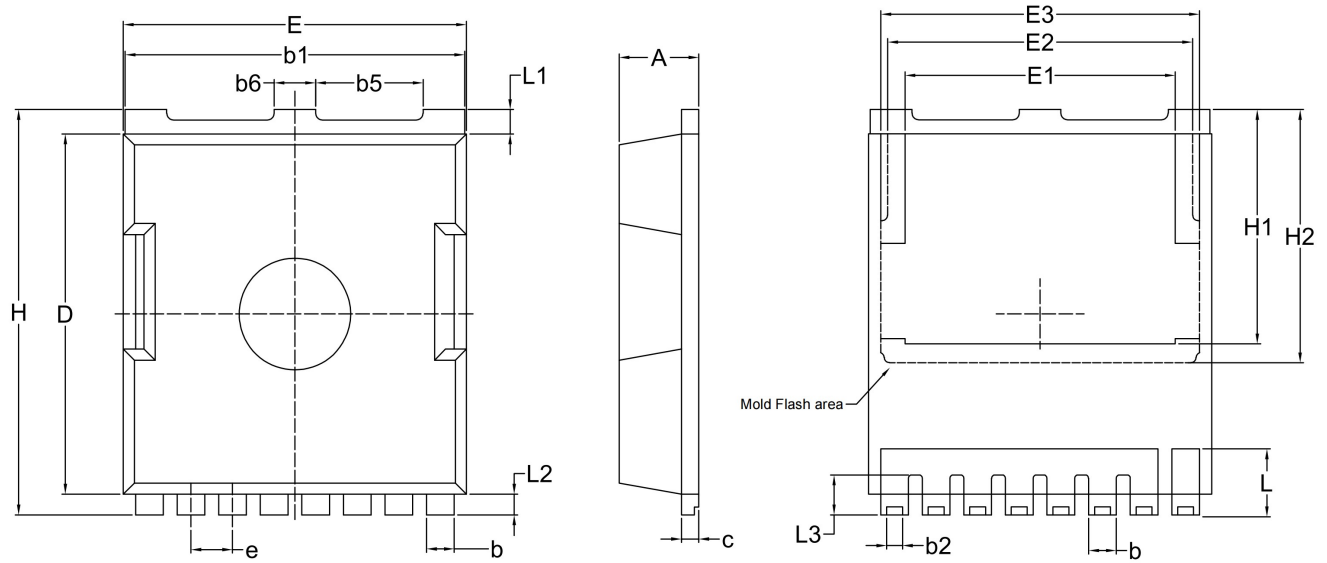
Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
e	1.20BSC		
H	11.58	11.68	11.78
H1	6.95BSC		
K	2.80REF		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
R	3.00	3.10	3.20



Note:

1. Dimensions do NOT include mold flash protrusions or gate burrs.

TOLL Package Outline Data(for JJ)



Note:

1. Dimensions do not include mold flash protrusions or gate burrs.

Symbol	DIMENSIONS (unit : mm)			Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max		Min	Typ	Max
A	2.20	2.30	2.40	E2	--	8.80	--
b	0.70	0.80	0.90	E3	--	9.20	--
b1	9.70	9.80	9.90	e	1.20 BSC		
b2	0.42	0.46	0.50	H	11.58	11.68	11.78
b5	--	3.10	--	H1	6.65	6.75	6.85
b6	--	1.20	--	H2	--	7.30	--
c	0.492	0.500	0.508	L	1.70	1.90	2.10
D	10.28	10.38	10.48	L1	--	0.70	--
E	9.80	9.90	10.00	L2	--	0.60	--
E1	--	7.80	--	L3	1.05	1.15	1.25