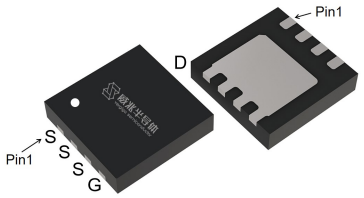
V_{DS}	-100	V
$R_{DS(on),TYP}$@ V_{GS}=-10 V	56	mΩ
$R_{DS(on),TYP}$@ V_{GS}=-4.5 V	61	mΩ
$I_{D(Silicon\ limited)}$	-27	A

Features

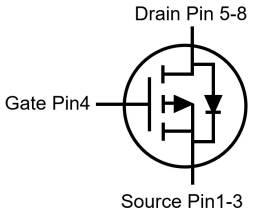
- Enhancement mode
- 100% Avalanche tested,100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TDFN3333



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS1505AB	TDFN3333	1505AB	5000PCS/Reel



Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		-100	V
V_{GS}	Gate-source voltage		±20	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	-27	A
I_D	Continuous drain current @V_{GS}=-10V (Silicon limited)	T_C = 25°C	-27	A
I_D	Continuous drain current @V_{GS}=-10V (Silicon limited)	T_C = 100°C	-17	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	-100	A
I_{DSM}	Continuous drain current @VGS=-10V	T_A = 25°C	-4.1	A
		T_A = 70°C	-3.3	A
EAS	Maximum avalanche energy, single pulsed ②		121	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	96	W
		T_C = 100°C	38	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	2.3	W
		T_A = 70°C	1.5	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	1.1	1.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	46	55	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=-250μA	-100	--	--	V
I_{DSS}	Zero gate voltage drain current	V_{DS}=-100V,V_{GS}=0V	--	--	-1	μA
	Zero gate voltage drain current(Tj=125℃)⑦	V_{DS}=-100V,V_{GS}=0V	--	--	-100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.7	-2.3	V
$R_{DS(on)}$	Drain-Source on-state resistance ⑧	V_{GS}=-10V, I_D=-20A	--	56	70	mΩ
		(Tj=100℃)⑦	--	85	--	mΩ
$R_{DS(on)}$	Drain-Source on-state resistance ⑧	V_{GS}=-4.5V, I_D=-15A	--	61	76	mΩ
G_{FS}	Forward transconductance	V_{DS}=-5V, I_D=-20A	--	30	--	S
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=-50V,V_{GS}=0V, f=100KHz	--	3860	--	pF
Coss	Output capacitance ⑦		--	140	--	pF
Crss	Reverse transfer capacitance ⑦		--	80	--	pF
Rg	Gate resistance	f=1MHz	--	17	--	Ω
Qg(-10V)	Total gate charge ⑦	V_{DS}=-50V,I_D=-20A, V_{GS}=-10V	--	60	--	nC
Qg(-4.5V)	Total gate charge ⑦		--	28	--	nC
Qgs	Gate-source charge ⑦		--	12	--	nC
Qgd	Gate-drain charge ⑦		--	8	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay time	V_{DD}=-50V, I_D=-20A, R_G=2.7Ω, V_{GS}=-10V	--	6.6	--	ns
Tr	Turn-on rise time		--	24	--	ns
Td(off)	Turn-off delay time		--	199	--	ns
Tf	Turn-off fall time		--	95	--	ns
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-20A,V_{GS}=0V	--	-0.88	-1	V
Trr	Reverse recovery time ⑦	V_{DD}=-50V I_{sd}=-20A, V_{GS}=0V di/dt=-100A/μs	--	25	--	ns
Qrr	Reverse recovery charge ⑦		--	30	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -22A, V_{GS} =-10V；100% FT tested at L = 0.1mH, I_{AS} = -30A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

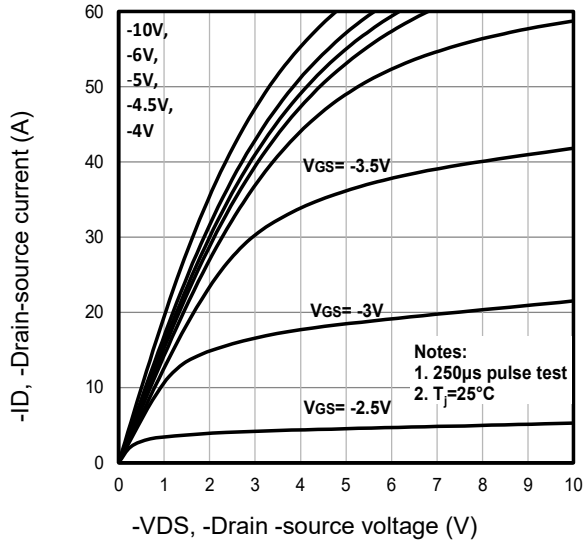


Fig1. Typical output characteristics

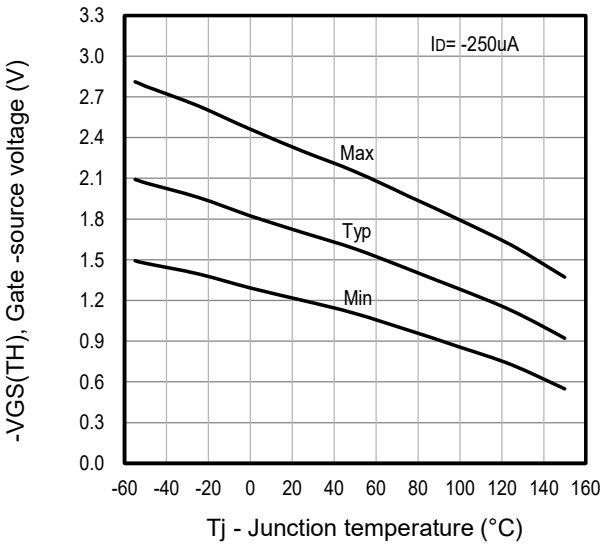


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs Tj

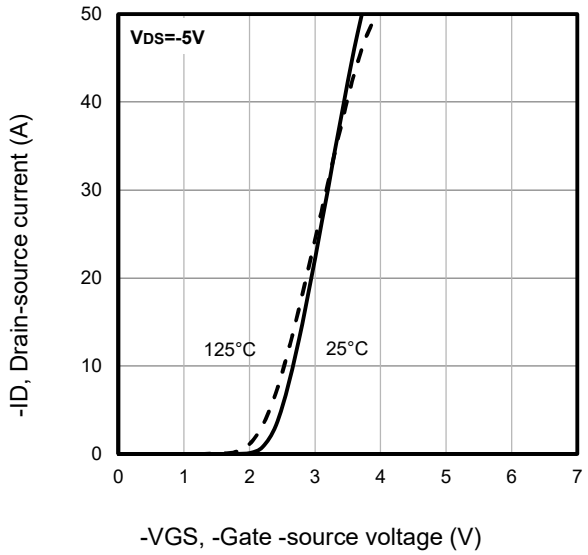


Fig3. Typical transfer characteristics

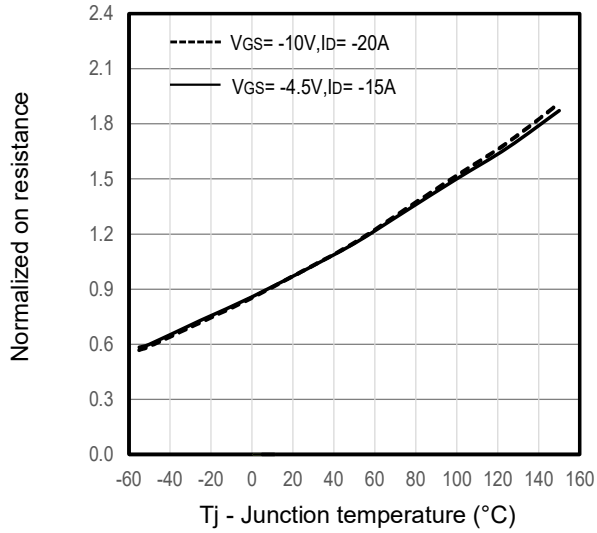


Fig4. Typical normalized on-resistance Vs. Tj

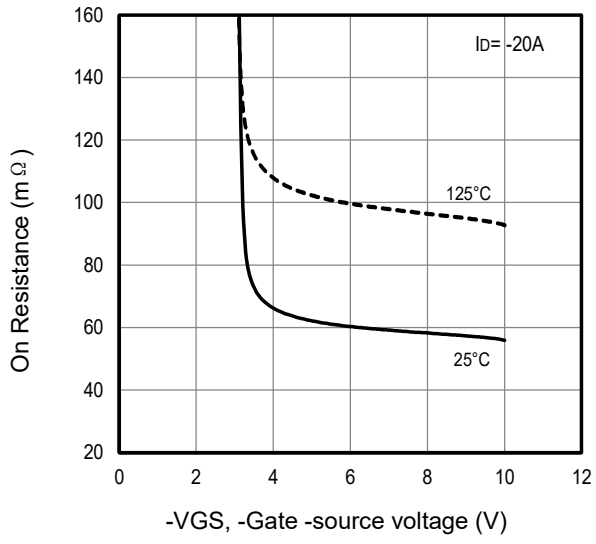


Fig5. Typical on resistance Vs gate -source voltage

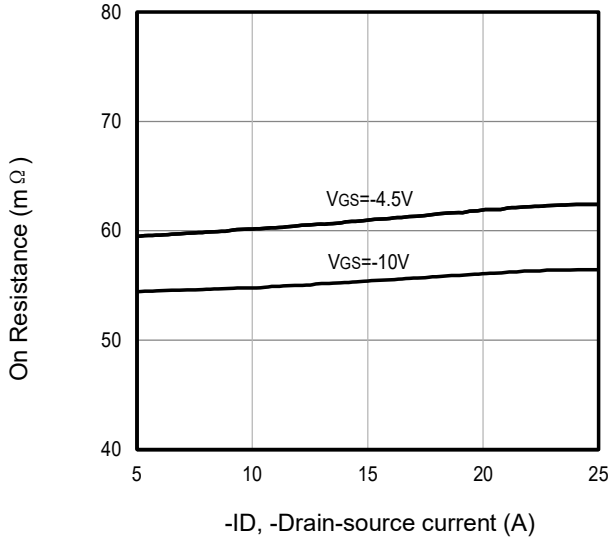


Fig6. Typical on resistance Vs drain current

Typical Characteristics

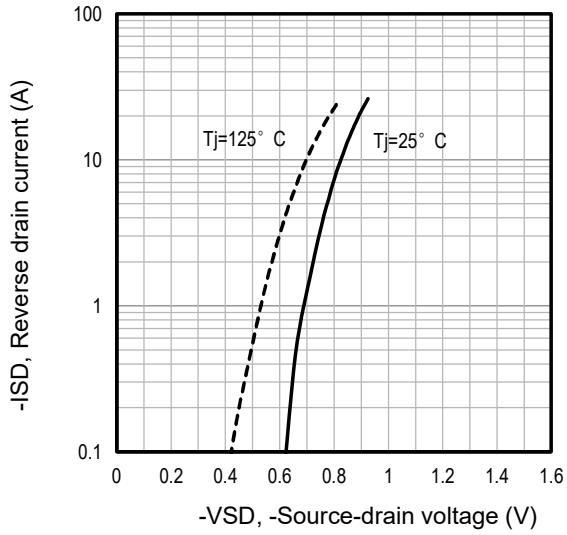


Fig7. Typical source-drain diode forward voltage

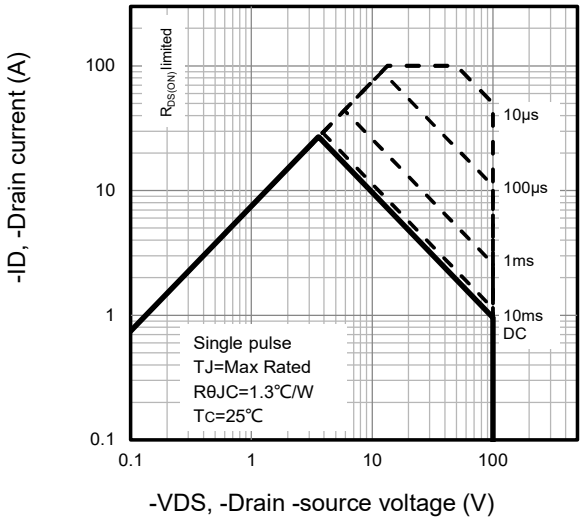


Fig8. Maximum safe operating area

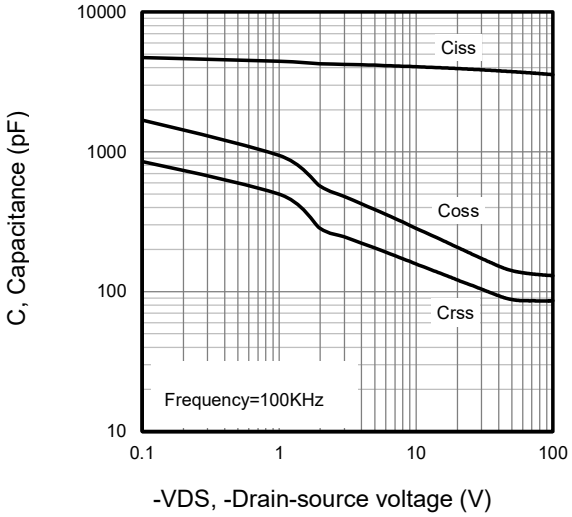


Fig9. Typical capacitance Vs drain-source voltage

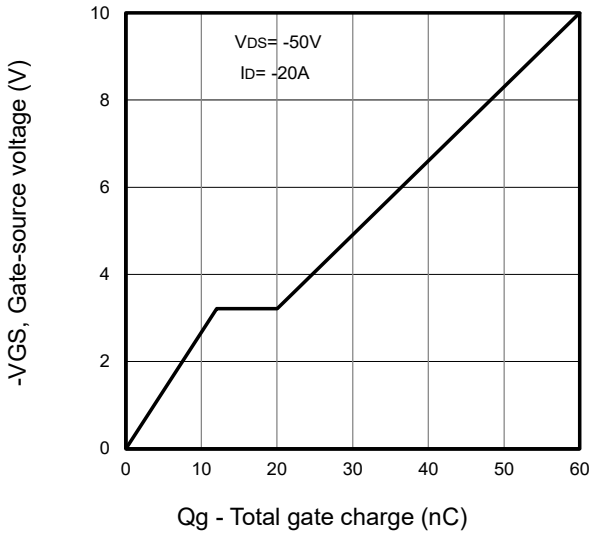


Fig10. Typical gate charge Vs gate-source voltage

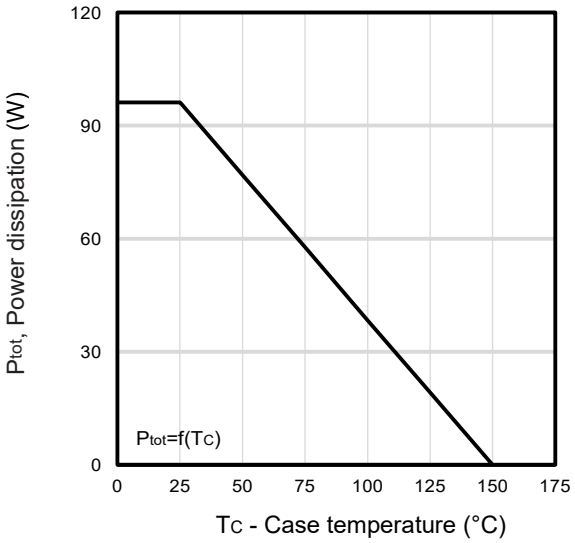


Fig11. Power dissipation Vs. case temperature

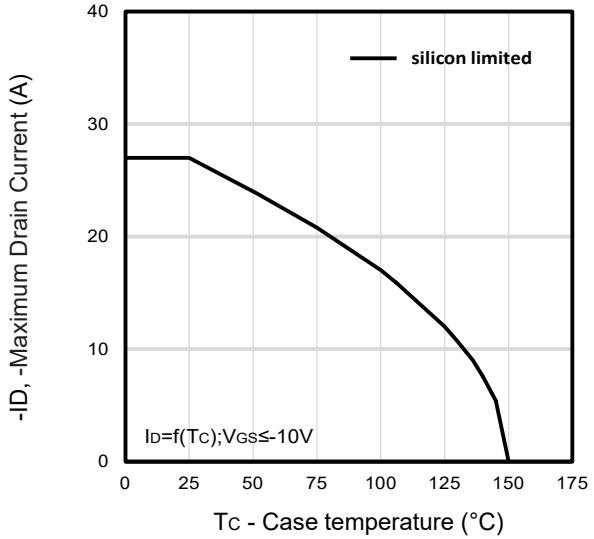


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

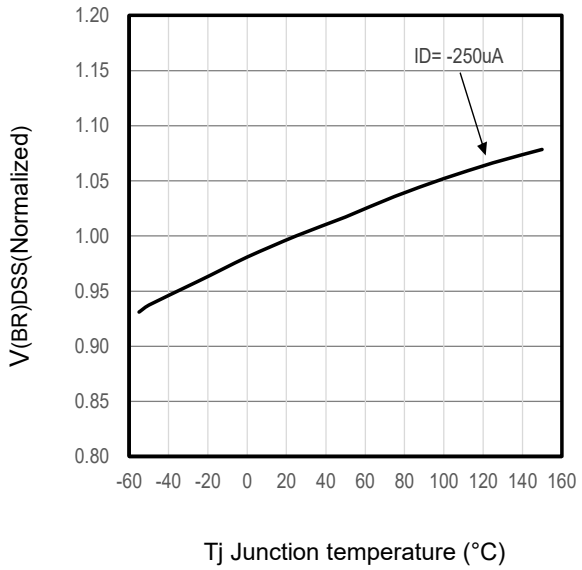


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

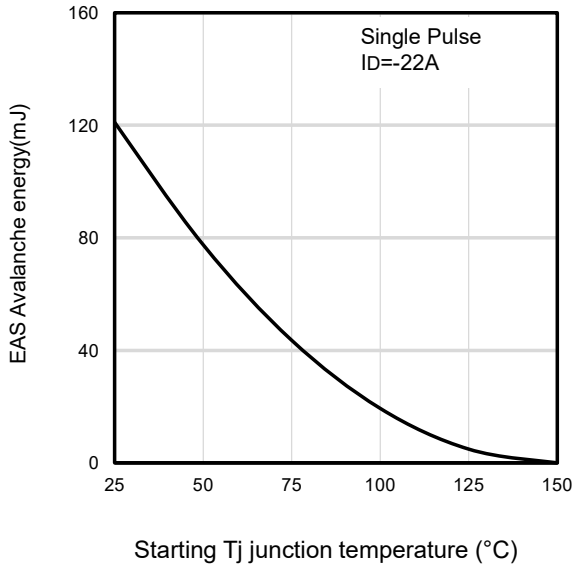


Fig14. Maximum avalanche energy vs temperature (°C)

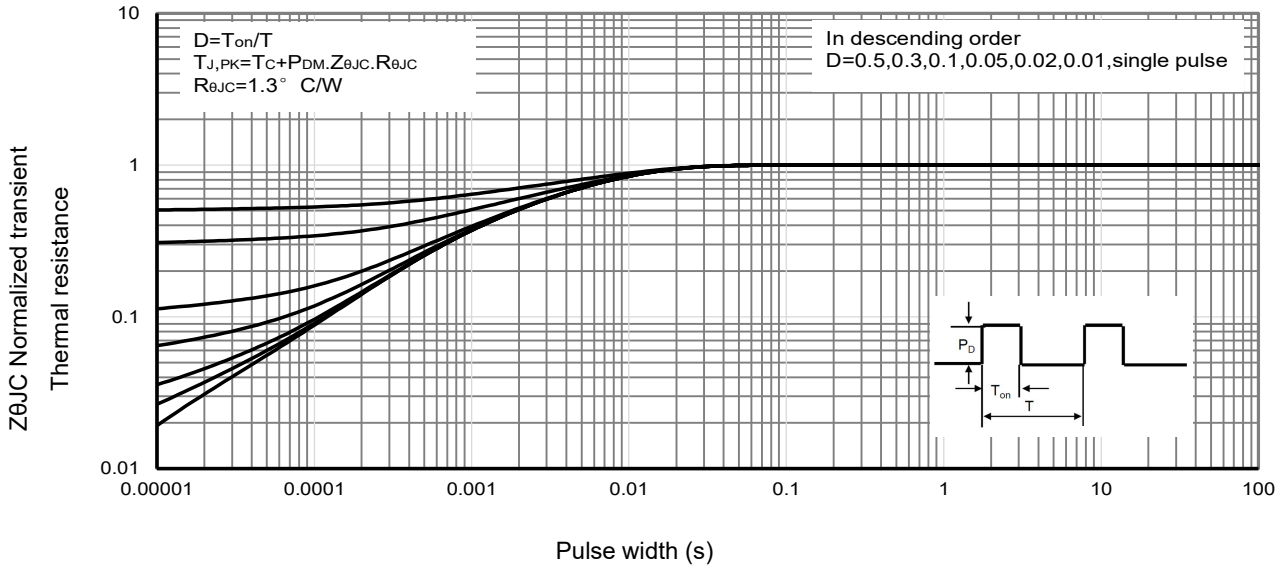


Fig15 . Normalized maximum transient thermal impedance

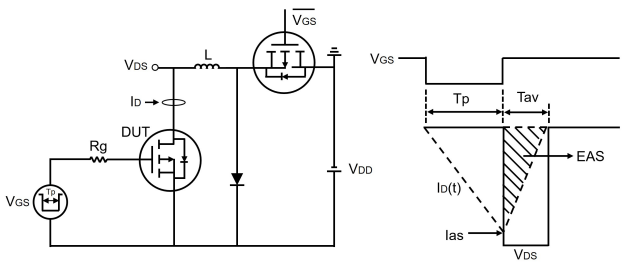


Fig16. Unclamped Inductive Test Circuit and waveforms

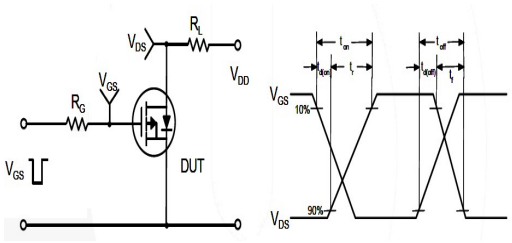
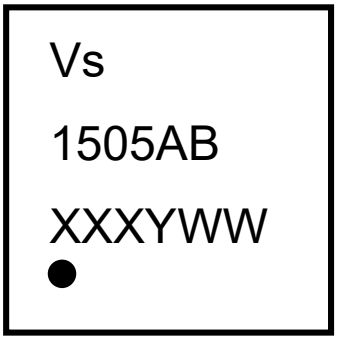


Fig17. Switching Time Test Circuit and waveforms

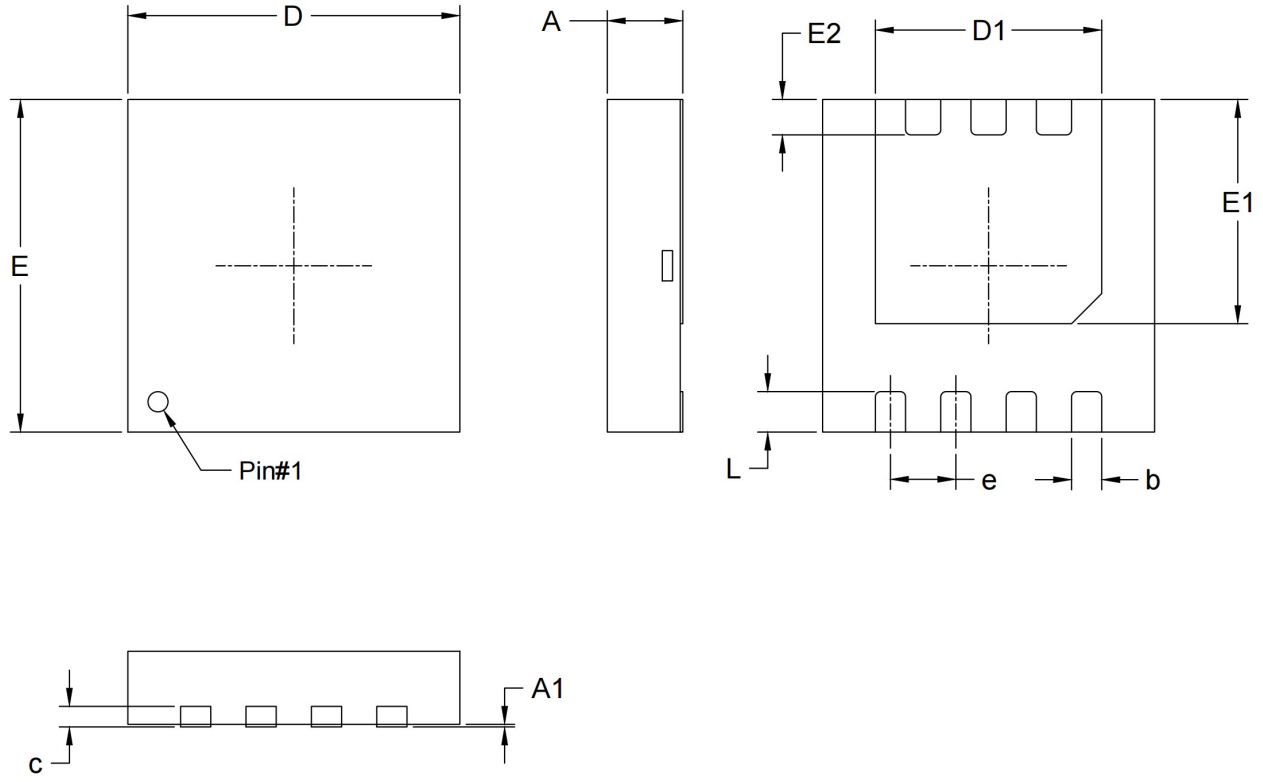
Marking Information



1st line: Vergiga Code（Vs）
2nd line: Part Number（1505AB）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TDFN3333 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	--	0.05
b	0.24	0.30	0.35
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.15	2.25	2.35
E	3.20	3.30	3.40
E1	2.13	2.23	2.33
E2	0.25	0.35	0.45
e	0.65 BSC		
L	0.30	0.40	0.50