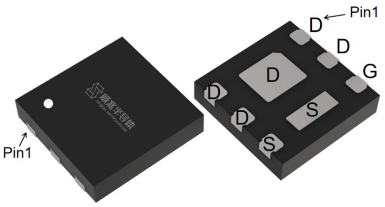
Features

- P-Channel
- Enhancement mode
- Fast Switching and High efficiency

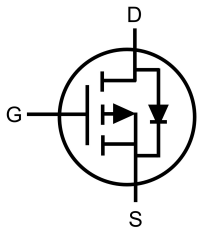
V_{DS}	-30	V
$R_{DS(on),TYP}$@ V_{GS}=-10 V	17.5	mΩ
$R_{DS(on),TYP}$@ V_{GS}=-4.5 V	25	mΩ
$I_{D(Silicon\ Limited)}$	-8.6	A

DFN2x2x0.5-6L



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS3522AA4	DFN2x2x0.5-6L	3522	3000PCS/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-30	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_A = 25°C	-2.6	A
I_D	Continuous drain current @VGS=-10V (Silicon limited)	T_A = 25°C	-8.6	A
I_D	Continuous drain current @VGS=-10V (Silicon limited)	T_A = 70°C	-6.9	A
I_{DM}	Pulse drain current tested ①	T_A = 25°C	-28	A
P_D	Maximum power dissipation ②	T_A = 25°C	2.6	W
		T_A = 70°C	1.7	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter		Typical	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient③	t≤10s	40	48	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient③	Steady State	66	79	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=-30V,V_{GS}=0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)④	V_{DS}=-30V,V_{GS}=0V	--	--	-100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1	-1.5	-2.1	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑤	V_{GS}=-10V, I_D=-4.5A	--	17.5	22	mΩ
		(T_j=100℃)④	--	24	--	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ⑤	V_{GS}=-4.5V, I_D=-4A	--	25	32	mΩ
G_{FS}	Forward transconductance	V_{DS}=-5V, I_D=-4.5A	--	9.3	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ④	V_{DS}=-15V,V_{GS}=0V, f=1MHz	--	1040	--	pF
Coss	Output Capacitance ④		--	150	--	pF
Crss	Reverse Transfer Capacitance ④		--	130	--	pF
Rg	Gate Resistance ④	f=1MHz	--	13	--	Ω
Qg(-10V)	Total Gate Charge ④	V_{DS}=-15V,I_D=-4.5A, V_{GS}=-10V	--	22	--	nC
Qg(-4.5V)	Total Gate Charge ④		--	11	--	nC
Qgs	Gate-Source Charge ④		--	2.7	--	nC
Qgd	Gate-Drain Charge ④		--	4.6	--	nC
Switching Characteristics ④						
Td(on)	Turn-on Delay Time	V_{DD}=-15V, I_D=-4.5A, R_G=2.7Ω, V_{GS}=-10V	--	5.6	--	ns
Tr	Turn-on Rise Time		--	14	--	ns
Td(off)	Turn-Off Delay Time		--	50	--	ns
Tf	Turn-Off Fall Time		--	25	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-4.5A,V_{GS}=0V	--	-0.77	-1	V
Trr	Reverse Recovery Time ④	V_{DD}=-15V I_{sd}=-4.5A, V_{GS}=0V di/dt=-100A/μs	--	15	--	ns
Qrr	Reverse Recovery Charge ④		--	5.3	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA t≤10s value.

③ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

④ Guaranteed by design, not subject to production testing.

⑤ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

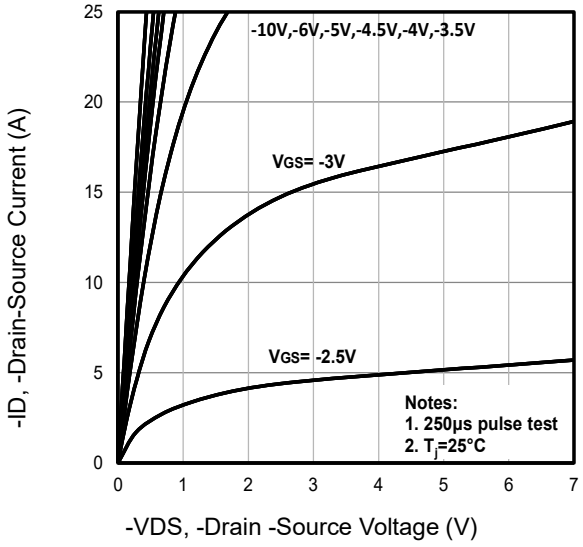


Fig1. Typical Output Characteristics

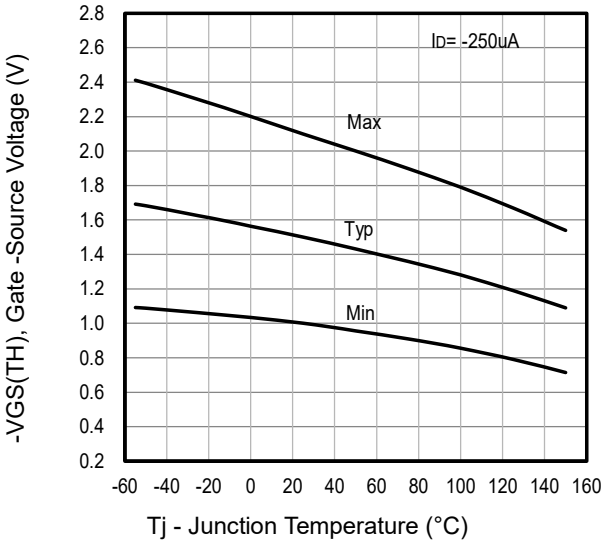


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

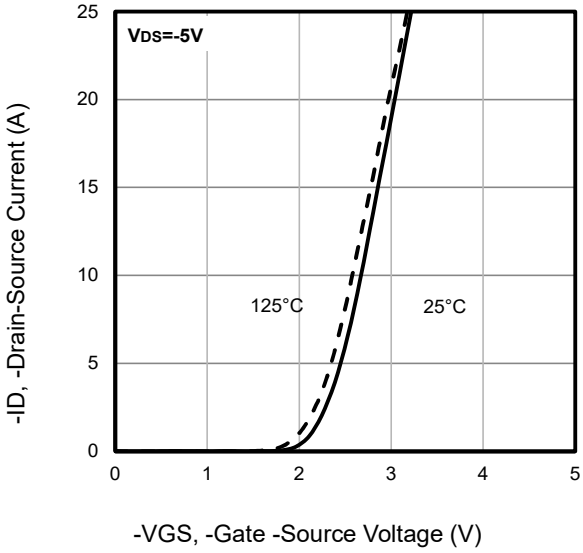


Fig3. Typical Transfer Characteristics

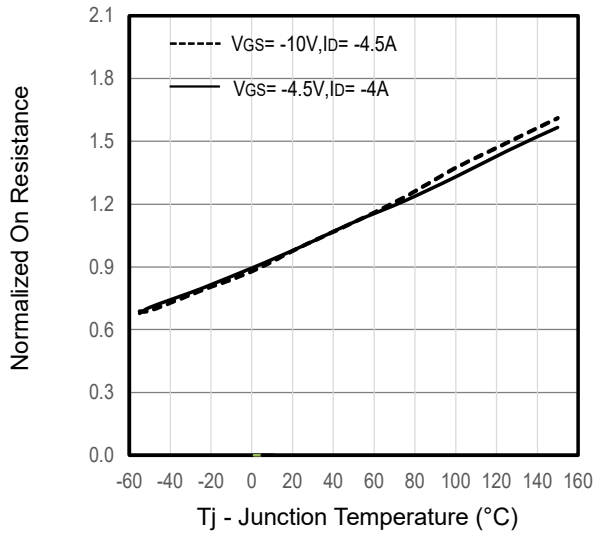


Fig4. Typical Normalized On-Resistance Vs. Tj

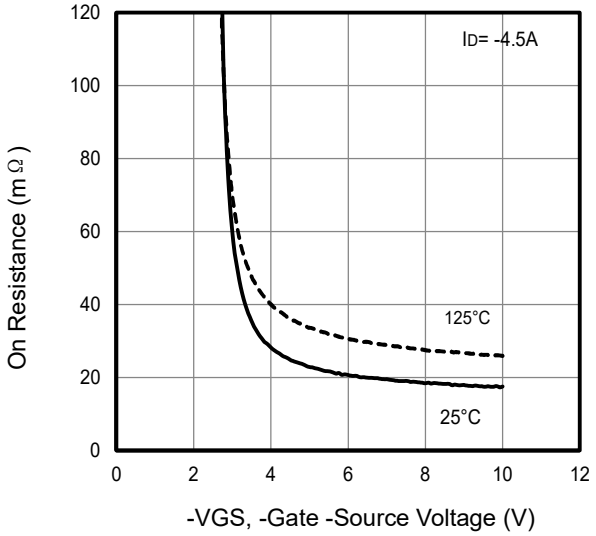


Fig5. Typical On Resistance Vs Gate -Source Voltage

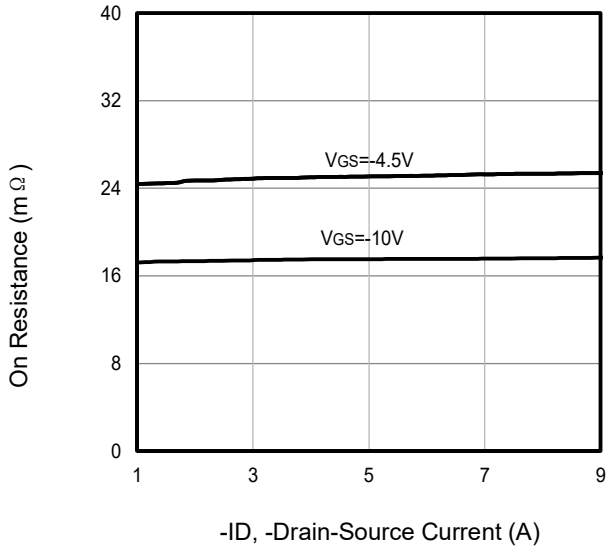


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

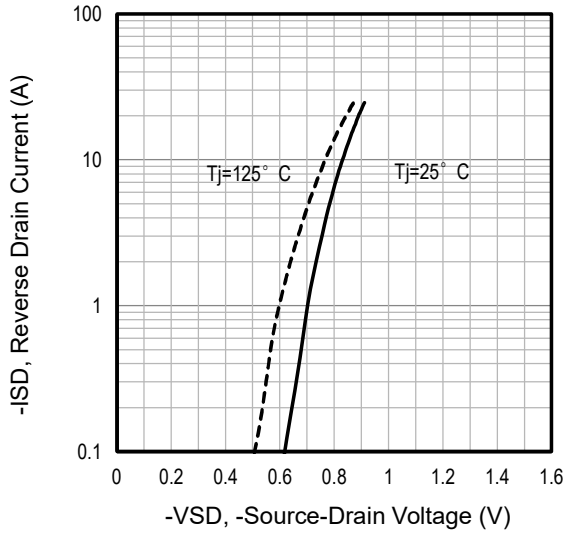


Fig7. Typical Source-Drain Diode Forward Voltage

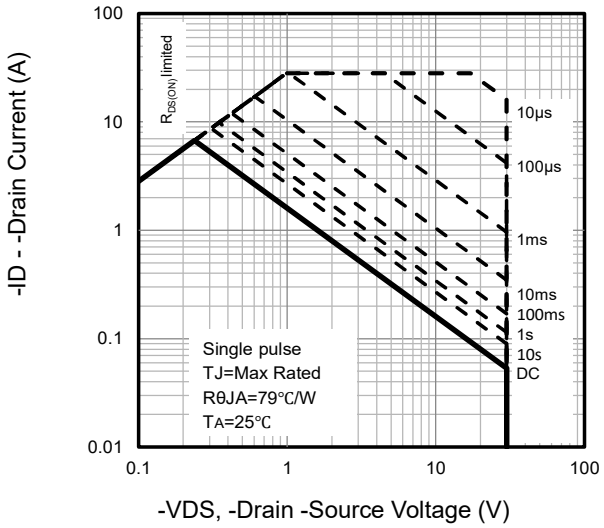


Fig8. Maximum Safe Operating Area

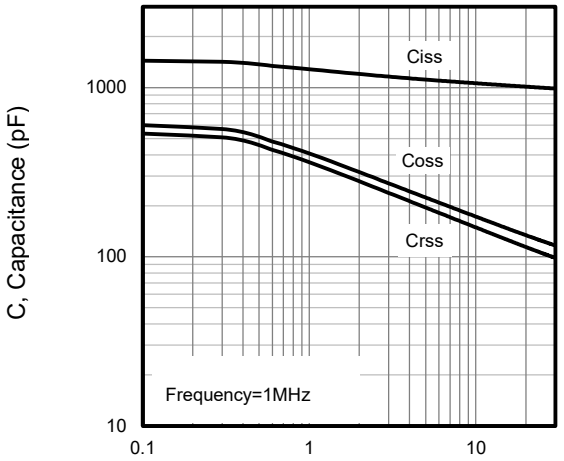


Fig9. Typical Capacitance Vs. Drain-Source Voltage

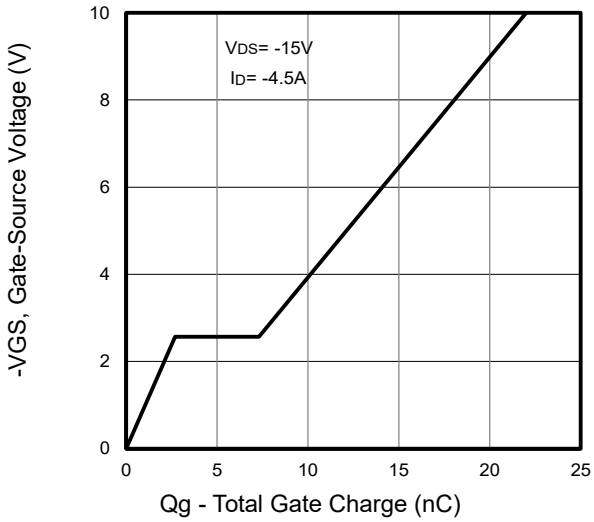


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

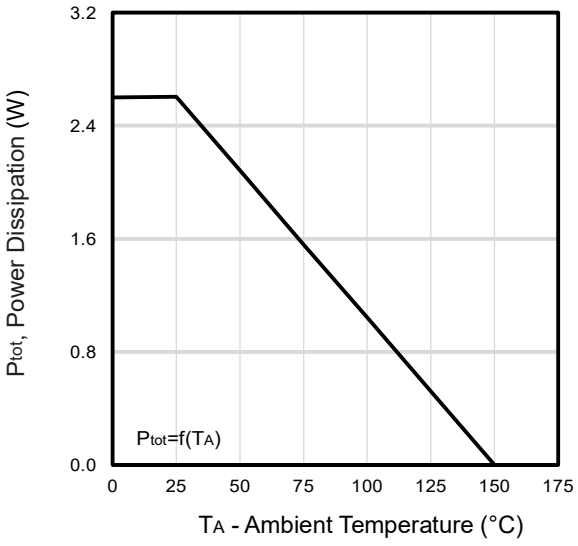


Fig11. Power Dissipation Vs. ambient Temperature

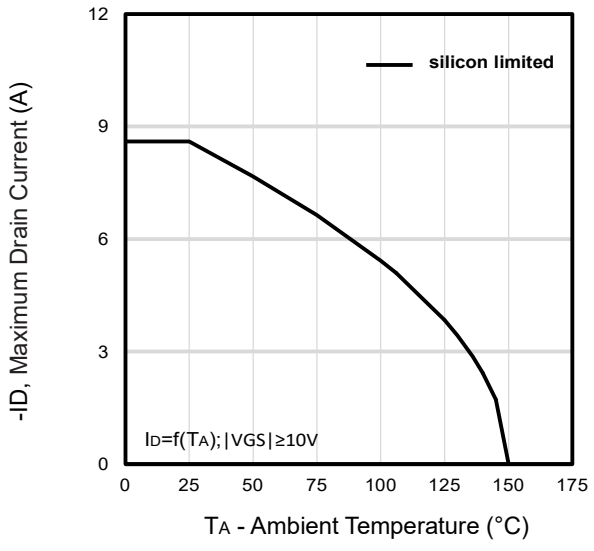


Fig12. Maximum Drain Current Vs.ambient Temperature

Typical Characteristics

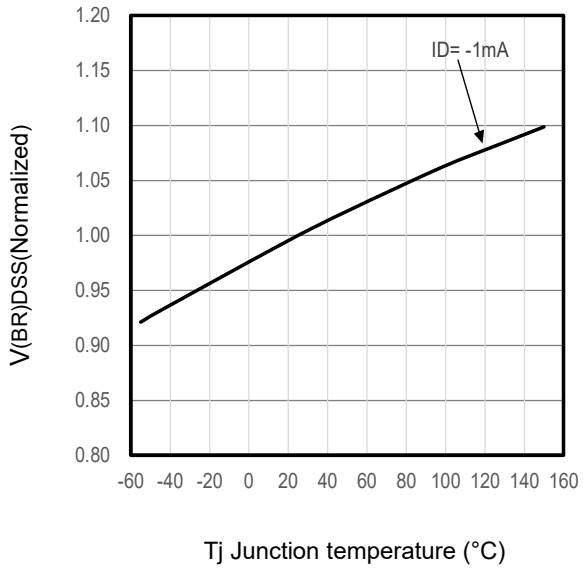


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

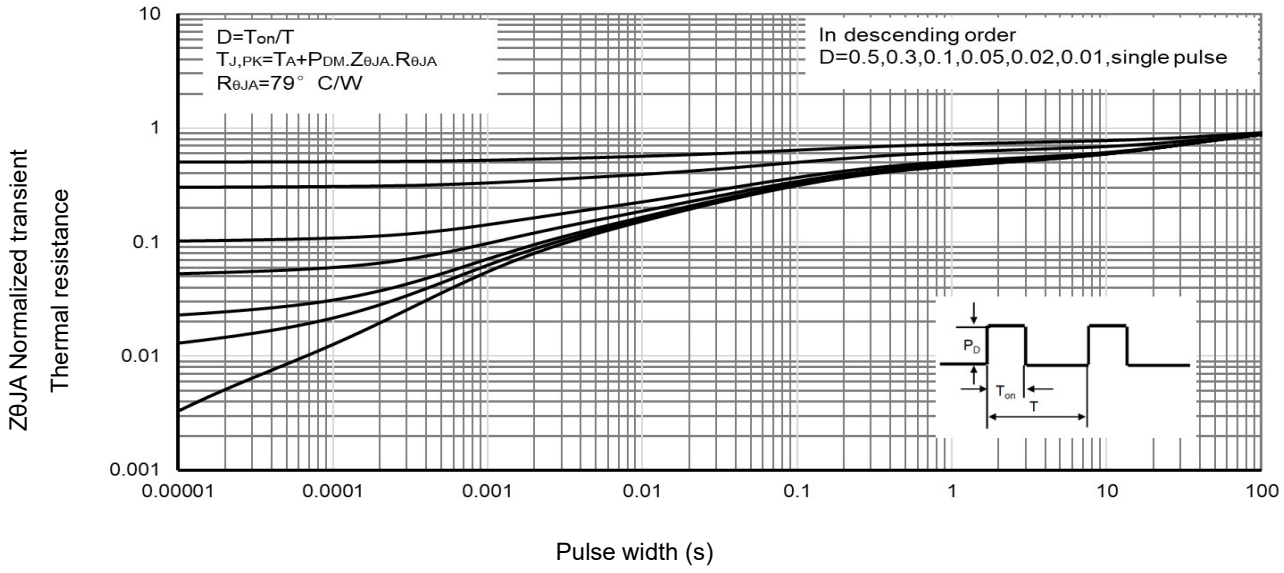


Fig14 . Normalized maximum transient thermal impedance

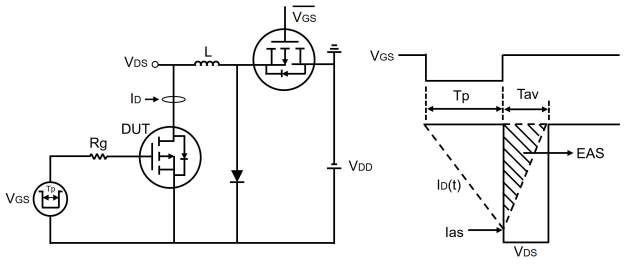


Fig15. Unclamped Inductive Test Circuit and waveforms

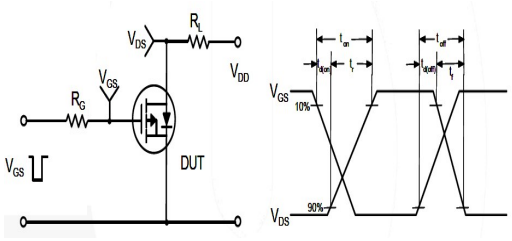


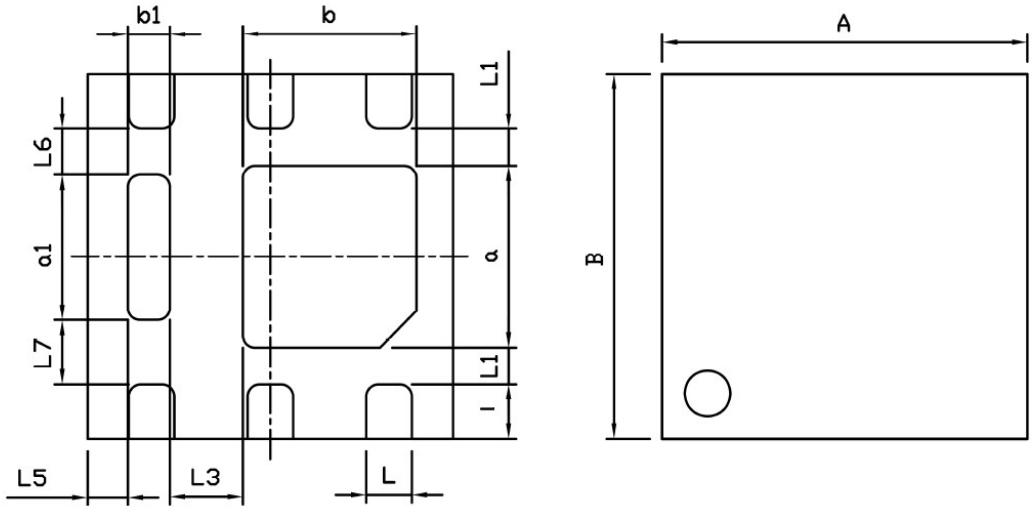
Fig16. Switching Time Test Circuit and waveforms

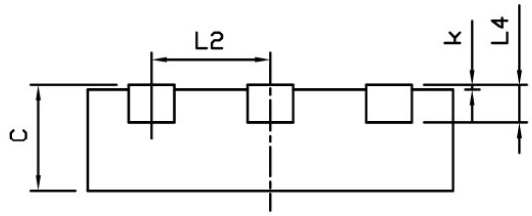
Marking Information

3522： Part Number
AA： Part Number
YM： Y：Year Code，refer to table below
M：Month Code，(e.g. 9=September, O=October, N=November, D=December, etc)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

DFN2x2x0.5-6L Package Outline Data





Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	1.95	2.00	2.05
B	1.95	2.00	2.05
C	0.45	0.50	0.55
L	0.25	0.30	0.35
L1	0.10	0.20	0.30
L2	--	0.65	--
L3	0.30	0.40	0.50
L4	--	0.152	--
L5	0.12	0.22	0.32
L6	0.15	0.25	0.35
L7	0.23	0.33	0.43
a	0.90	1.00	1.10
a1	0.72	0.82	0.92
b	0.85	0.95	1.05
b1	0.13	0.23	0.33
I	0.25	0.30	0.35
k	0.00	--	0.05