1. 特性

- 静态电流：3.9μA
- 低失调电压：±10μV (max)
- 失调电压漂移：
  - ±0.2μV/°C (max) at –40°C to 125°C
- 0.1Hz 至 10Hz 噪声：3.1μV_{PP}
- 输入偏置电流：±1.4pA
- 增益带宽：83kHz
- 电源电压：1.7V 至 5.5V
- 轨到轨输入/输出
- 抗 EMI 干扰
- 1 或者 2 通道

2. 应用

- 电池供电仪器仪表
- 气体检测
- 温度测量
  - 高阻抗热敏电阻
  - RTD、热电偶
- 故障监控
- 电流检测
  - 分流电阻
  - 电流变压器
- 电子秤

3. 说明

OPZ503/4 是一款高精度、零漂移 5V 运算放大器，尤其适用于高精度、低压传感器应用。OPZ503/4 在具备低零漂移和超低初始失调电压(±10μV，max)的基础上进一步实现了超低功耗，其典型功耗仅为 3.9μA。这使得设计者在保证功耗和保持精度的同时，能够有效解除电池供电场景的功耗担忧。

此外，OPZ503/4 器件具有 83kHz 带宽和皮安偏置电流，可有效减少放大器本身引入的误差，这使得 OPZ503/4 运算放大器非常适合电流检测、气体检测和温度传感等应用。零漂移功能使一些需要保持常开的设备不会因为环境变化损失太多的精度。

OPZ503/4 运算放大器采用 SOT23-5、SOT23-6 和 SOIC-8 封装，此外 OPZ5032 为 2 通道运放，封装为 SOIC-8。所有版本的额定温度范围为–40°C 至 125°C。有关订购信息，请参见 Table 1。

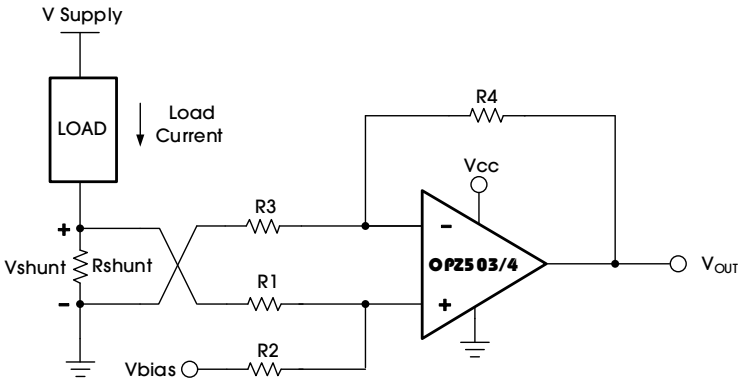


Table 1 lists the order information.

Table 1. Order Information

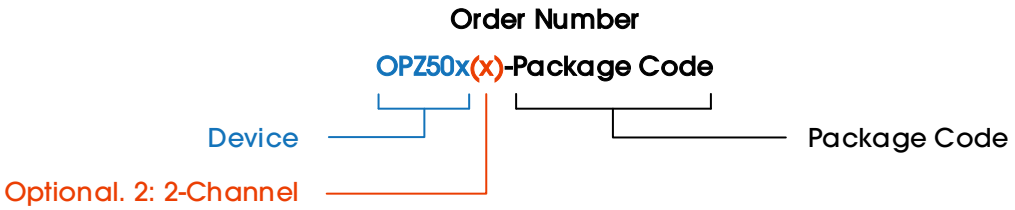
ORDER NUMBER[1]	CH (#)	PACKAGE	MARK	EN PIN	I_Q PER CH (TYP) (μA)	GBW (kHz)	SLEW RATE (TYP) (V/ms)	NOISE nV/√Hz (100Hz)	OPERATING TEMP (°C)	PACKAGE OPTION
OPZ503ASOT235	1	SOT23-5	OPZ503	No	3.9	83	30	93	-40-125	T/R-4000
OPZ503ASOIC8[2]	1	SOIC-8	OPZ503	No	3.9	83	30	93	-40-125	T/R-4000
OPZ5032ASOIC8[2]	2	SOIC-8	OPZ5032	No	3.9	83	30	93	-40-125	T/R-4000
OPZ504ASOT236	1	SOT23-6	OPZ504	Yes	3.9	83	30	93	-40-125	T/R-4000
OPZ504ASOIC8[2]	1	SOIC-8	OPZ504	Yes	3.9	83	30	93	-40-125	T/R-4000

Table 2. Family Selection Guide

ORDER NUMBER[1]	CH (#)	PACKAGE	MARK	EN PIN	I_Q PER CH (TYP) (μA)	GBW (kHz)	SLEW RATE (TYP) (V/ms)	NOISE nV/√Hz (100Hz)	OPERATING TEMP (°C)	PACKAGE OPTION
OPZ501ASOT235	1	SOT23-5	OPZ501	No	0.68	15	3	257	-40-125	T/R-4000
OPZ501ASOIC8[2]	1	SOIC-8	OPZ501	No	0.68	15	3	257	-40-125	T/R-4000
OPZ502ASOT236	1	SOT23-6	OPZ502	Yes	0.68	15	3	257	-40-125	T/R-4000
OPZ502ASOIC8[2]	1	SOIC-8	OPZ502	Yes	0.68	15	3	257	-40-125	T/R-4000
OPZ5012ASOIC8[2]	2	SOIC-8	OPZ5012	No	0.68	15	3	257	-40-125	T/R-4000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration (SOT23-5 and SOT23-6 packages).

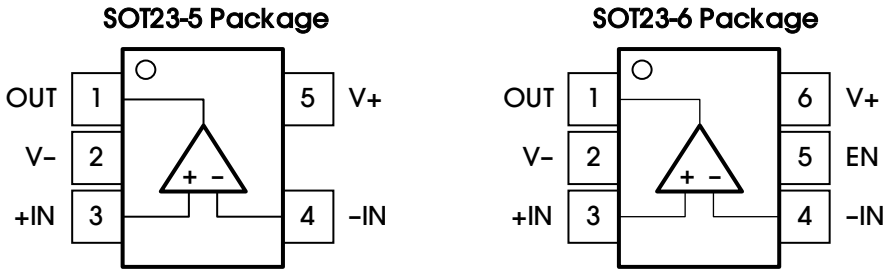


Figure 1. Pin Configuration (SOT23-5 and SOT23-6 Packages)

Table 3 lists the pin functions (SOT23-5 and SOT23-6 packages).

Table 3. Pin Functions (SOT23-5 and SOT23-6 Packages)

POSITION		NAME	TYPE	DESCRIPTION
SOT23-5	SOT23-6			
1	1	OUT	Ouput	Output
2	2	V–	Power	Negative (lowest) power supply
3	3	+IN	Input	Positive (non-inverting) input
4	4	–IN	Input	Negative (inverting) input
5	6	V+	Power	Positive (highest) power supply
—	5	EN	Input	Enable pin

Figure 2 illustrates the pin configuration (SOIC-8 package).

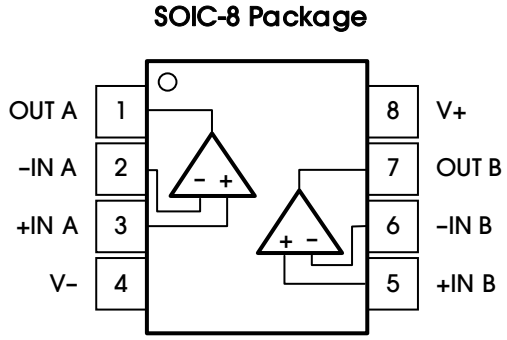


Figure 2. Pin Configuration (SOIC-8 Package)

Table 4 lists the pin functions (SOIC-8 package).

Table 4. Pin Functions (SOIC-8 Package)

POSITION	NAME	TYPE	DESCRIPTION
1	OUT A	Ouput	Output, channel A
2	–IN A	Input	Inverting input, channel A
3	+IN A	Input	Non-inverting input, channel A
4	V–	Power	Negative (lowest) power supply
5	+IN B	Input	Non-inverting input, channel B
6	–IN B	Input	Inverting input, channel B
7	OUT B	Output	Output, channel B
8	V+	Power	Positive (highest) power supply

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the OPZ503/4.

Table 5. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply		–0.3	6	V
	Signal input pins(2)(3)	Common-mode	(V–) – 0.3	(V+) + 0.3	
		Differential	–0.3	0.3	
Current	Signal input pins		–10	10	mA
	Output short-circuit(4)		Continuous		
Temperature	Operating, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

Note 1: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
Note 3: Not to exceed –0.3V or +4.0V on ANY pin, referred to V–.
Note 4: Short-circuit to ground, one amplifier per package.

5.2 ESD RATINGS

Table 6 lists the ESD ratings of the OPZ503/4.

Table 6. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the OPZ503/4.

Table 7. Recommended Operating Conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage Range	1.7		5.5	V
Specified Temperature Range	–40		125	°C

5.4 THERMAL INFORMATION

Table 8 lists the thermal information for the OPZ503/4.

Table 8. Thermal Information

PARAMETER	SYMBOL	SOT23-5	SOT23-6	SOIC-8	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	168	169	90.6	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	103	109	35	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	39	28	47.6	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	10	11	3.6	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	36	28	47	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	66	59	50.8	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 9 lists the electrical characteristics of OPZ503/4. T_A = 25°C, V_S = 1.7V to 5.5V, V_{CM} = V_{OUT} = V_S / 2, and R_L ≥ 10MΩ to V_S / 2, unless otherwise noted.

Table 9. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OFFSET VOLTAGE							
Input Offset Voltage	V_{OS}	V_S = 5V			±1.5	±10	μV
Input Offset Voltage Drift	dV_{OS}/dT	T_A = –40°C to 125°C, V_S = 5V			±0.03	±0.2	μV/°C
Power-Supply Rejection Ratio	PSRR	V_S = 1.7V to 5.5V			0.6	2.5	μV/V
INPUT BIAS CURRENT							
Input Bias Current	I_B	+IN	T_A = 25°C		4		pA
			T_A = 125°C		340		
		–IN	T_A = 25°C		–2		
			T_A = 125°C		–378		
Input Offset Current	I_{OS}				6		pA
NOISE							
Input Voltage Noise	E_n	f = 0.1Hz to 10Hz			3.1		μV_{pp}
Input Voltage Noise Density	e_n	f = 100Hz			93		$nV/\sqrt{Hz}$
Input Current Noise Density	i_n	f = 100Hz			0.4		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
Common-Mode Voltage Range	V_{CM}			V–		V+	V
Common-Mode Rejection Ratio	CMRR	(V–) ≤ V_{CM} ≤ (V+), V_S = 5.5V		108	133		dB
INPUT CAPACITANCE							
Differential					3.3		pF
Common-Mode					3.7		pF
OPEN-LOOP GAIN							
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.1V ≤ V_O ≤ (V+) – 0.1V, R_L = 100kΩ to V_S / 2			140		dB
FREQUENCY RESPONSE							
Gain-Bandwidth Product	GBW	C_L = 20pF, R_L = 10MΩ			83		kHz
Slew Rate	SR	G = 1, C_L = 20pF			30		V/ms
OUTPUT							
Voltage Output Swing from Positive Rail	V_{OH}	R_L = 100kΩ to (V+) / 2, V_S = 5.5V				5	mV
Voltage Output Swing from Negative Rail	V_{OL}	R_L = 100kΩ to (V+) / 2, V_S = 5.5V				5	
Short-Circuit Current	I_{SC}	Sourcing, V_O to (V–), $V_{IN\ (diff)}$ = 100mV, V_S = 5.5V			20		mA
		Sinking, V_O to (V+), $V_{IN\ (diff)}$ = –100mV, V_S = 5.5V			20		
Capacitive Load Drive	C_L			See Table 10			
Open-Loop Output Impedance	Z_O	f = 100Hz, I_O = 0A			80		kΩ
POWER SUPPLY							
Quiescent Current per Channel	I_Q	V_{CM} = V_S / 2, I_O = 0, V_S = 3.3V			3.9	4.8	uA

6. TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 3.3V, V_{CM} = V_{OUT} = V_S / 2, C_L = 20pF, and R_L ≥ 10MΩ, unless otherwise noted.

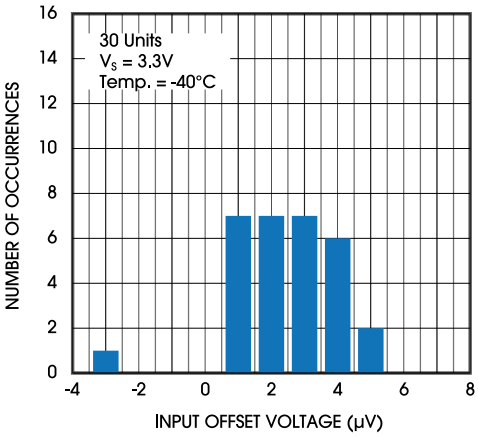


Figure 3. Offset Voltage Distribution, V_S = 3.3V

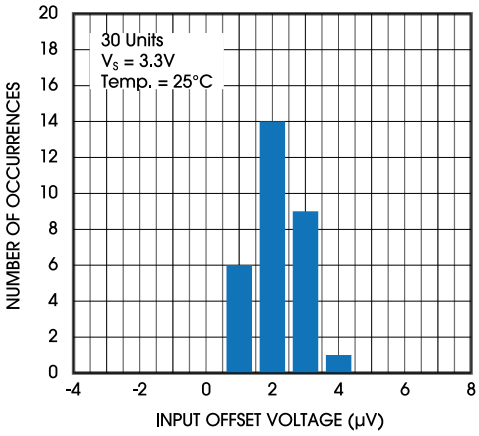


Figure 4. Offset Voltage Distribution, V_S = 3.3V

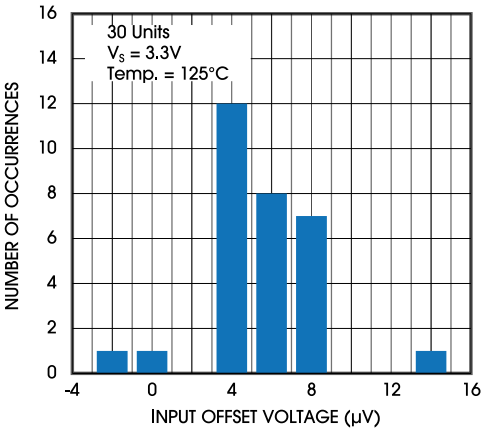


Figure 5. Offset Voltage Distribution, V_S = 3.3V

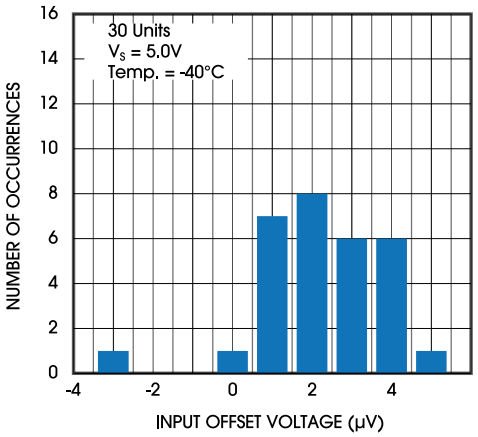


Figure 6. Offset Voltage Distribution, V_S = 5V

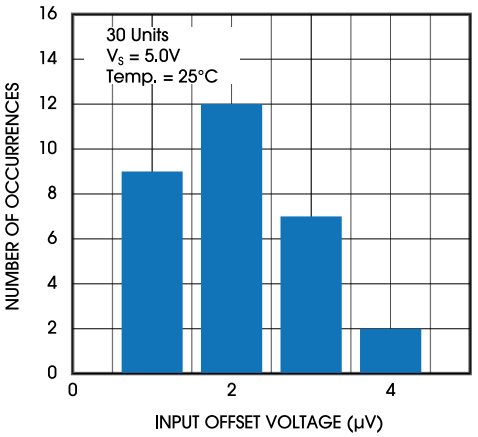


Figure 7. Offset Voltage Distribution, V_S = 5V

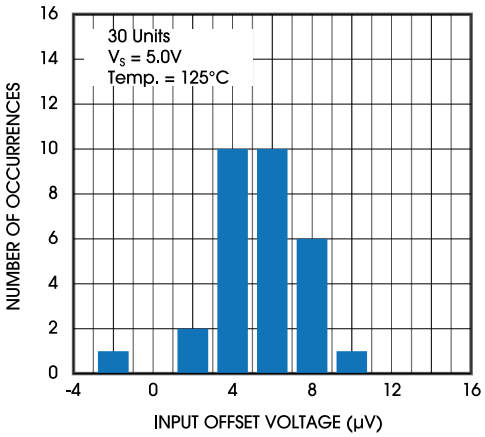


Figure 8. Offset Voltage Distribution, V_S = 5V

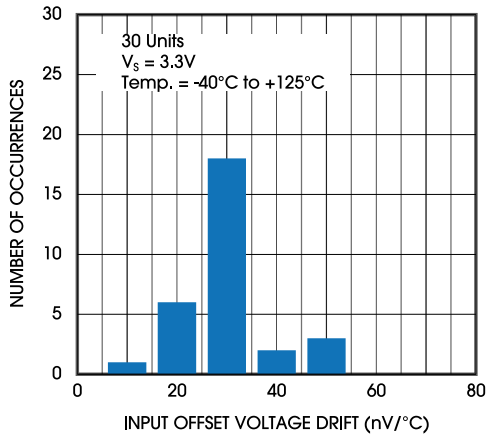


Figure 9. Offset Voltage Drift Distribution, V_S = 3.3V

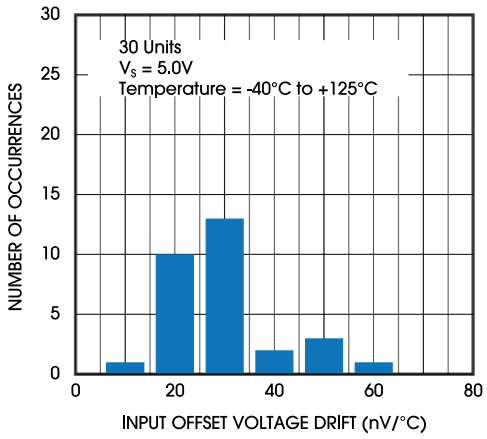


Figure 10. Offset Voltage Drift Distribution, V_S = 5V

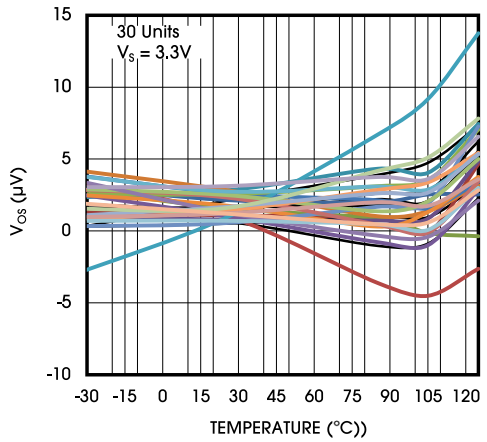


Figure 11. Offset Voltage vs. Temperature, V_S = 3.3V

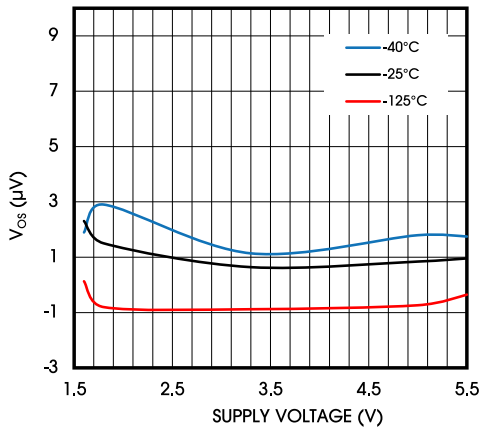


Figure 12. Offset Voltage vs. Supply Voltage

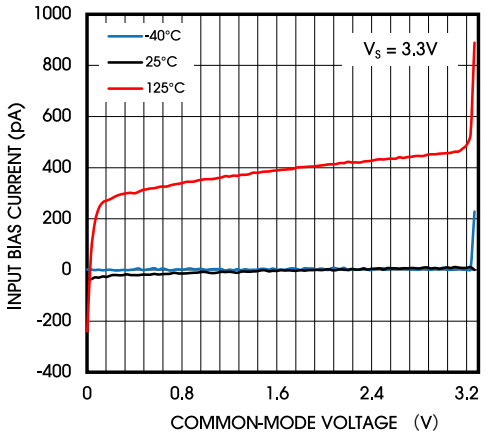


Figure 13. Input Bias Current on +IN Input Pin vs. Common-Mode Voltage

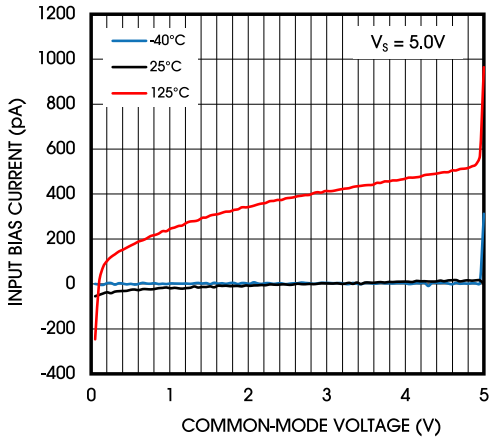


Figure 14. Input Bias Current on +IN Input Pin vs. Common-Mode Voltage

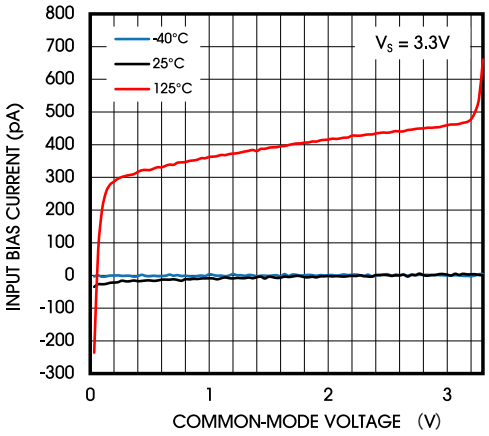


Figure 15. Input Bias Current on –IN Pin vs. Common-Mode Voltage

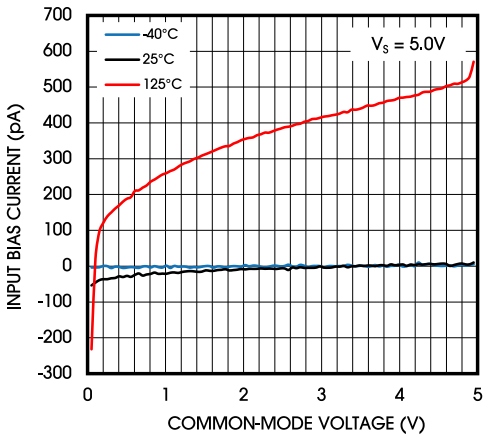


Figure 16. Input Bias Current on –IN Pin vs. Common-Mode Voltage

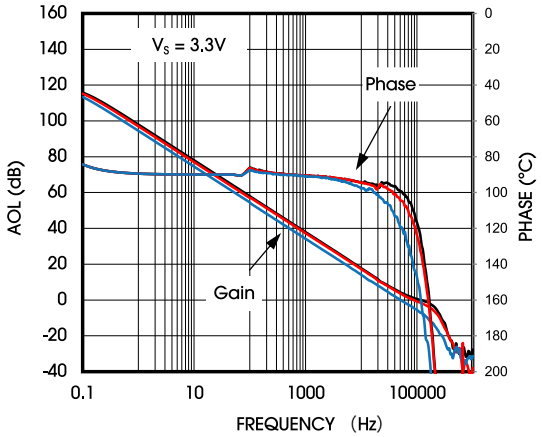


Figure 17. Open-Loop Gain and Phase vs. Frequency

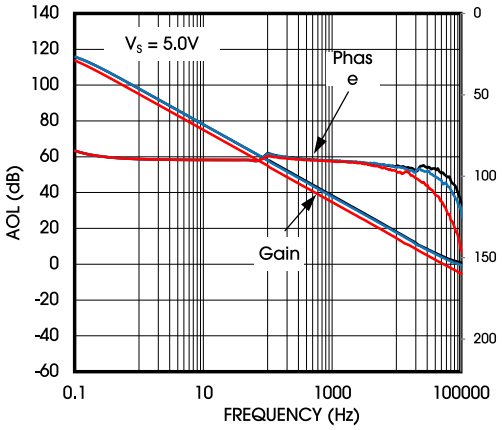


Figure 18. Open-Loop Gain and Phase vs. Frequency

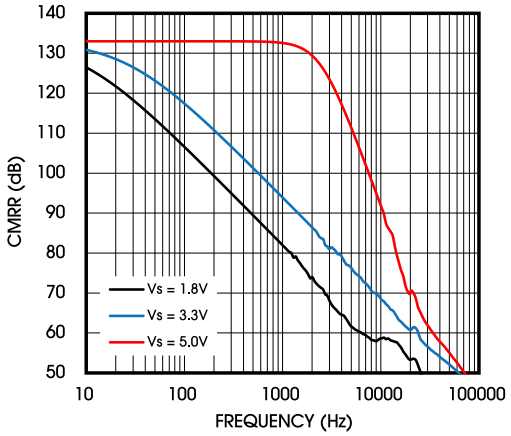


Figure 19. CMRR vs. Frequency

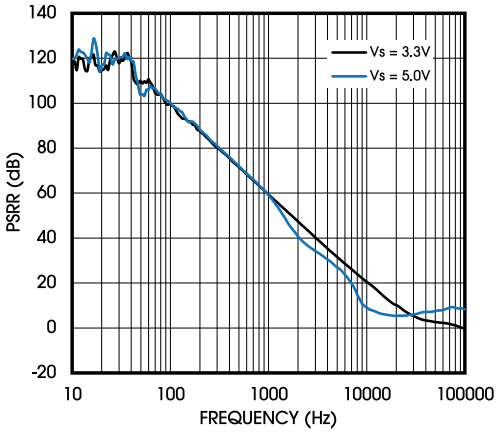


Figure 20. PSRR vs. Frequency

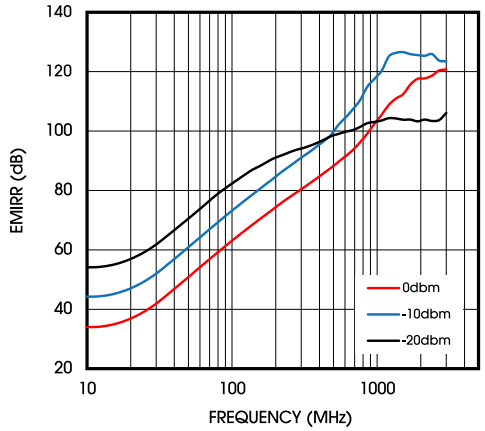


Figure 21. EMIRR Performance

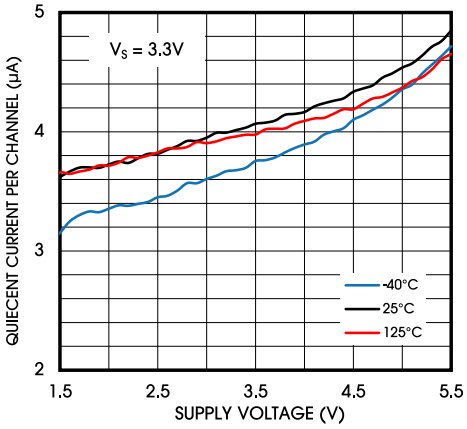


Figure 22. Per Channel Quiescent Current vs. Supply Voltage

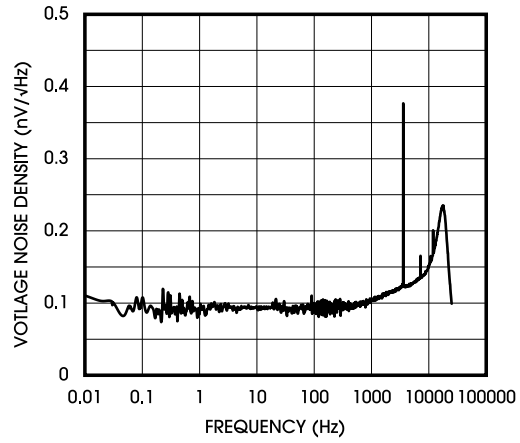


Figure 23. Voltage Noise Spectral Density vs. Frequency

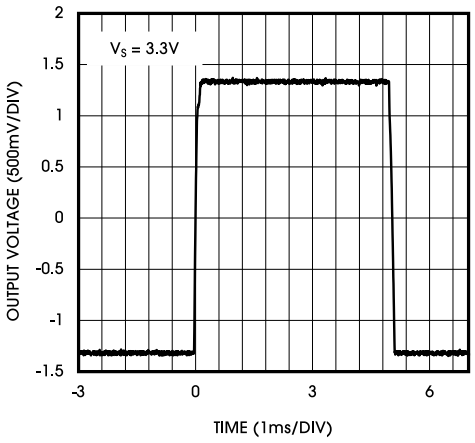


Figure 24. Large-Signal Response, 3.3V

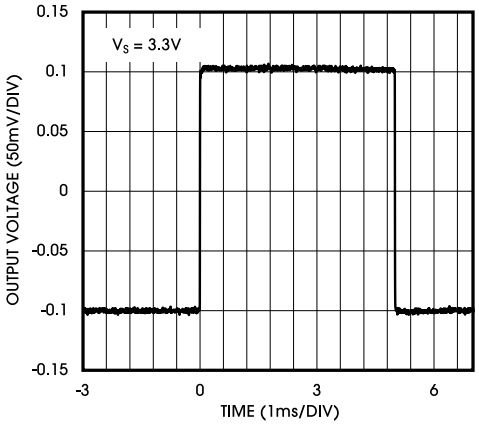


Figure 25. Small Signal Response, 3.3V

7. 详细描述

7.1 概述

OPZ503/4 是一款零漂移、超低功耗、轨到轨输入和输出运算放大器，可提供超低失调电压和接近零的失调电压漂移。OPZ503/4 的工作电压范围为 1.7V 至 5.5V，单位增益稳定，适用于范围广泛的通用应用。

7.2 功能模块框图

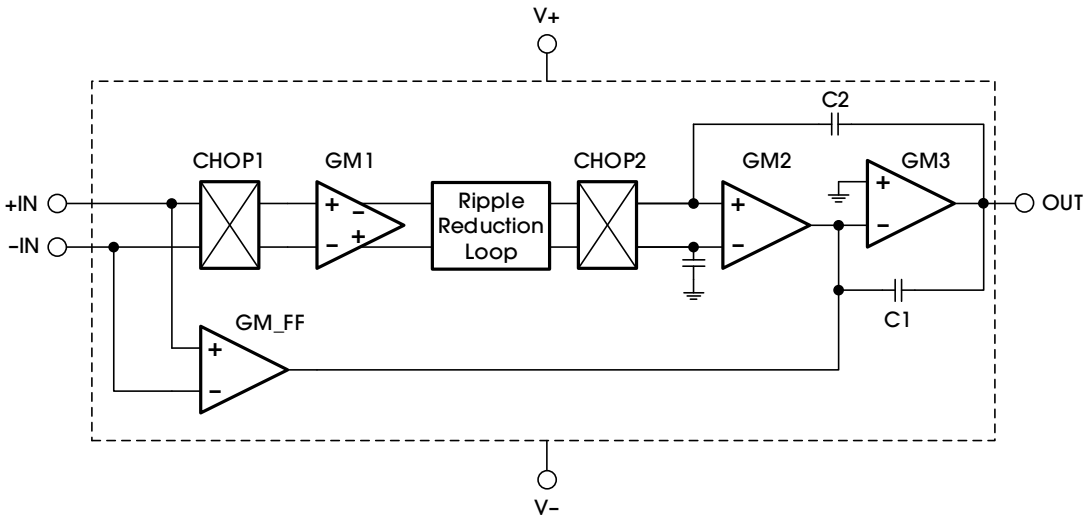


Figure 26. Functional Block Diagram

7.3 特性描述

OPZ503/4 单位增益稳定，并使用自动校准技术实现低失调电压以及极低漂移(随时间和温度变化)。为了获得更好的精度性能，建议在设计中避免温度梯度、异种金属和直接气流。

7.3.1 工作电压

OPZ503/4 运算放大器的工作电源电压范围为 1.7V 至 5.5V(±0.85V 至±2.75V)。随电源电压或温度变化的参数请参考 TYPICAL CHARACTERISTICS 部分。

警告：高于 6V(绝对最大值)的电源电压可能会永久损坏设备。

7.3.2 输入

对于输入电路设计，输入共模电压范围建议在推荐范围内。如果瞬时输入电压超过电源电压，则将输入电流限制在 10mA 以内。这种限制很容易通过添加一个与输入串联的电阻器来实现，如 Figure 27 所示。

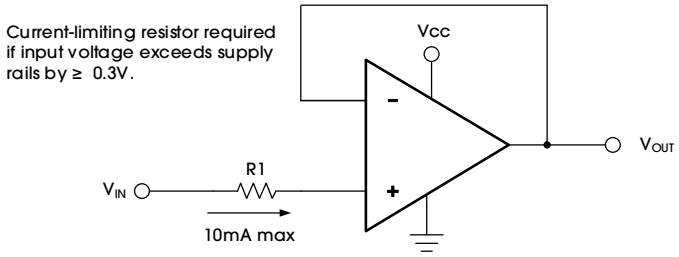


Figure 27. Input Current Protection

OPZ503/4 运算放大器包含一个内部输入低通滤波器，可降低放大器受到外部 EMI 的干扰。输入滤波器包括共模和差模滤波。

7.3.3 驱动容性负载

单位增益跟随器是驱动容性负载时最灵敏的配置，因为它会降低放大器的相位裕度。为保证足够的相位裕度，避免潜在的震荡，建议在大(> 50pF)场景下加隔离电阻 R_{ISO}，如 Figure 28 所示。

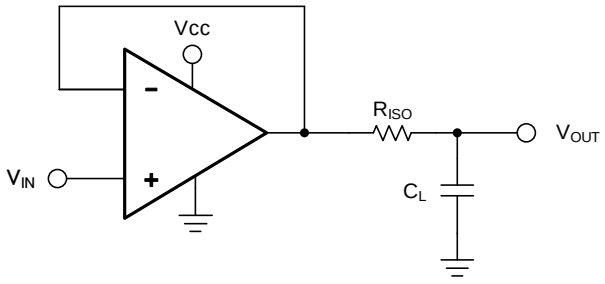


Figure 28. Resistive Isolation of Capacitive Load

应根据 C_L 的大小和所需的性能水平来决定要使用的 R_{ISO} 值。对于 3.3V 电源，下表给出了 R_{ISO} 的推荐最小值。

Table 10. Capacitive Loads vs. Needed Isolation Resistors

C_L	R_{ISO}
0–20pF	Not needed
50pF	15kΩ
100pF	15kΩ
500pF	15kΩ
1nF	15kΩ
5nF	15kΩ
10nF	15kΩ

8. 布局

8.1 布局指南

建议保持尽可能短的走线，尽可能使用 PCB 接地层，并将表面贴装元件放置在尽可能靠近器件引脚的位置。建议在电源引脚之间放置一个 0.1μF 电容。在整个模拟电路中应用这些指南以提高性能，例如降低电磁干扰(EMI)敏感性。

运算放大器对射频干扰(RFI)的敏感性各不相同。RFI 通常可以识别为偏移电压或 DC 信号电平随干扰 RF 信号的变化而变化。OPZ503/4 专为最大限度地降低对 RFI 的敏感性而设计，与上一代设备相比，灵敏度显着降低。强 RF 场仍可能导致不同的偏移水平。

8.2 布局示例

请参考 EVM 或者咨询 AnalogySemi 销售支持。

9. PACKAGE INFORMATION

The OPZ503/4 family is available in the SOT23-5, SOT23-6 and SOIC-8 packages.

9.1 SOT23-5 PACKAGE

Figure 29 shows the SOT23-5 package view.

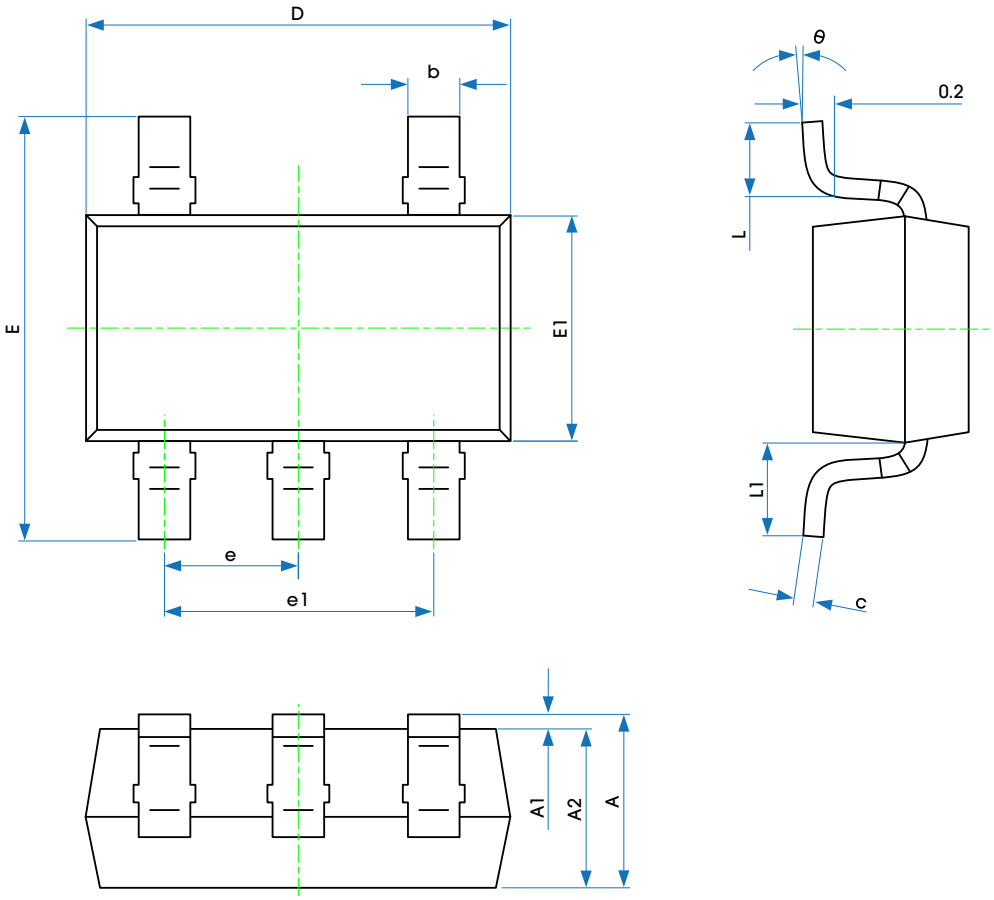


Figure 29. SOT23-5 Package View

Table 11 provides detailed information about the dimensions of the SOT23-5 package.

Table 11. Dimensions of the SOT23-5 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600 REF.		0.024 REF.	
θ	0°	8°	0°	8°

9.2 SOT23-6 PACKAGE

Figure 30 shows the SOT23-6 package view.

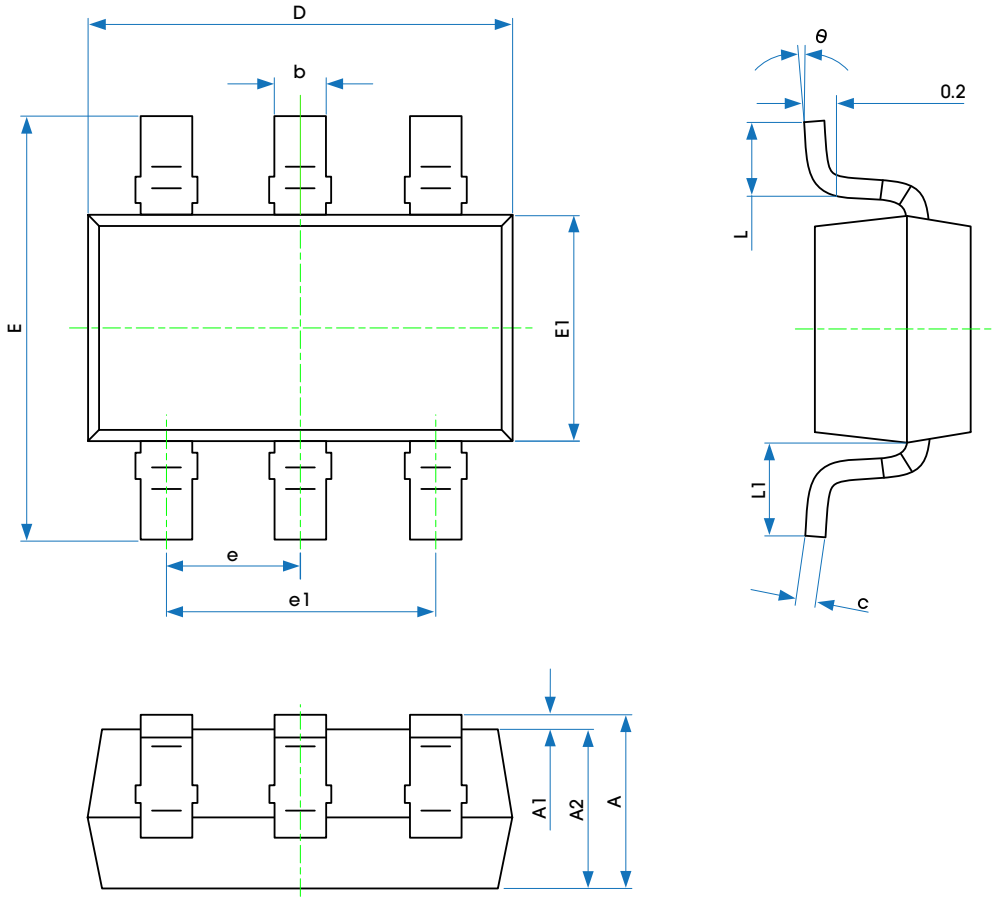


Figure 30. SOT23-6 Package View

Table 12 provides detailed information about the dimensions of the SOT23-6 package.

Table 12. Dimensions of the SOT23-6 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600 REF.		0.024 REF.	
θ	0°	8°	0°	8°

9.3 SOIC-8 PACKAGE

Figure 31 shows the SOIC-8 package view.

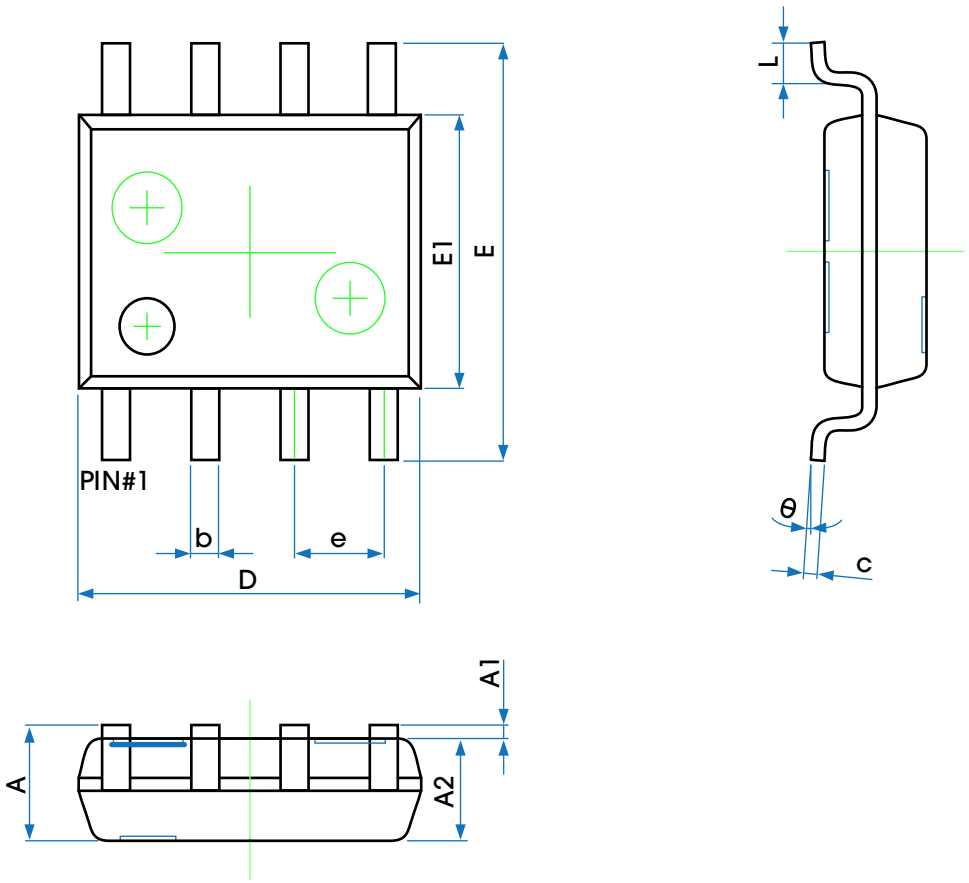


Figure 31. SOIC-8 Package View

Table 13 provides detailed information about the dimensions of the SOIC-8 package.

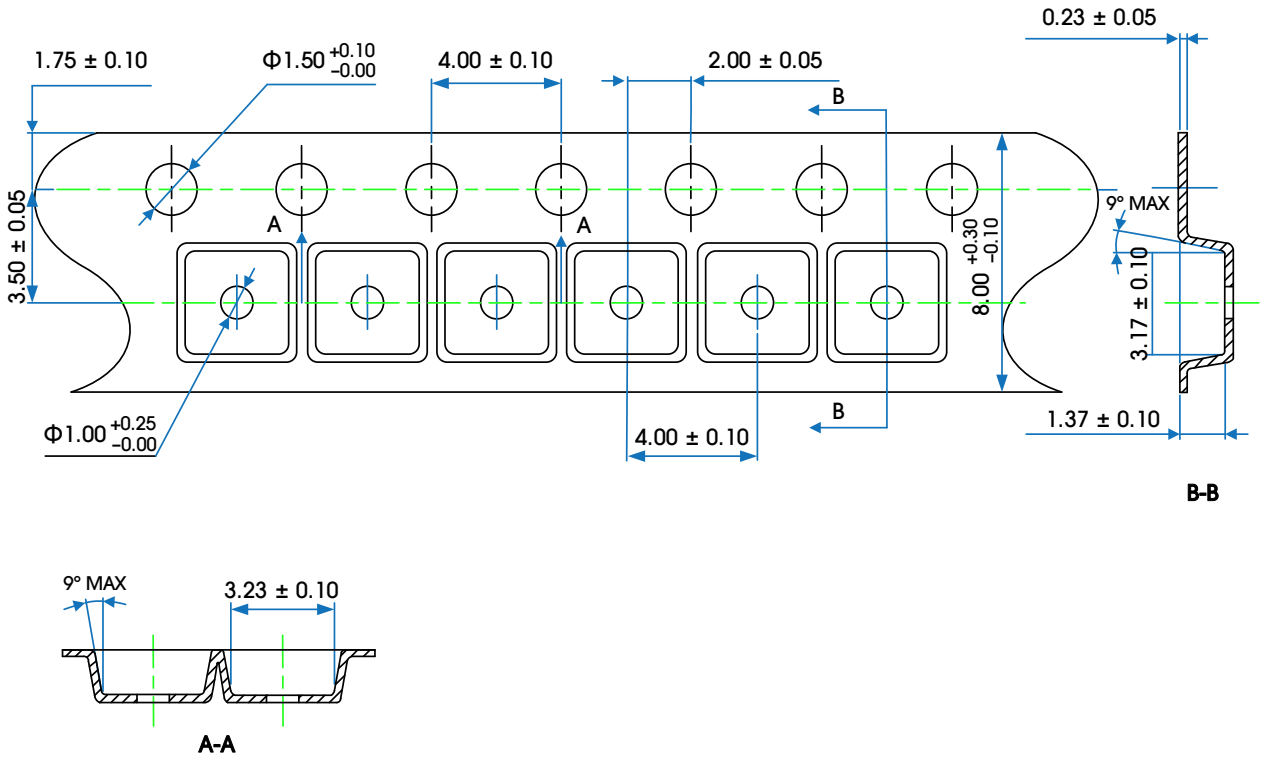
Table 13. Dimensions of the SOIC-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

10. TAPE AND REEL INFORMATION

10.1 SOT23-5/SOT23-6 PACKAGE

Figure 32 illustrates the carrier tape.



Notes:
1. Cover tape width: 5.50 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 2mm in 250mm.
4. Mold#: SOT23-5/SOT23-6.
5. All dimensions: mm.
6. Direction of view:

Figure 32. Carrier Tape Drawing

Table 14 provides information about tape and reel.

Table 14. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOT23-5/ SOT23-6	7''	3000	10	4	120000	210*208*203	440*440*230

Figure 33 shows the product loading orientation—pin 1 is assigned at Q3.

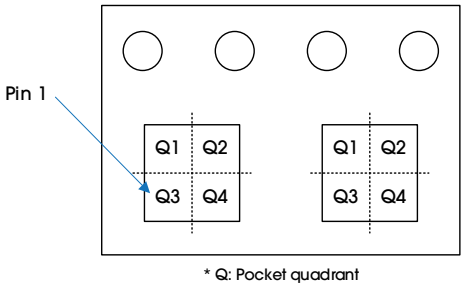
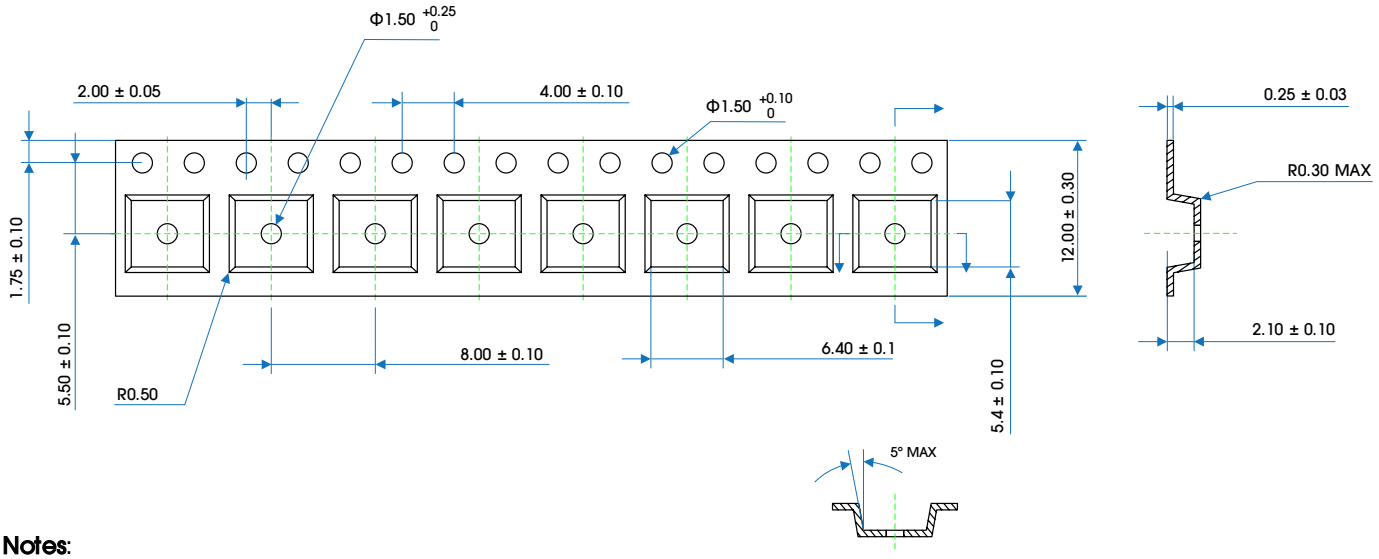


Figure 33. Product Loading Orientation

10.2 SOIC-8 PACKAGE

Figure 34 illustrates the carrier tape.



Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: SOIC-8.
5. All dimensions: mm.
6. Direction of view:

Figure 34. Carrier Tape Drawing

Table 15 provides information about tape and reel.

Table 15. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
SOIC-8	13''	4000	1	8	32000	358*340*50	430*380*390

Figure 35 shows the product loading orientation—pin 1 is assigned at Q1.

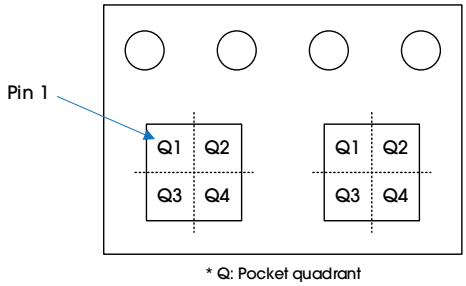


Figure 35. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	24 February 2023	Rev A release.