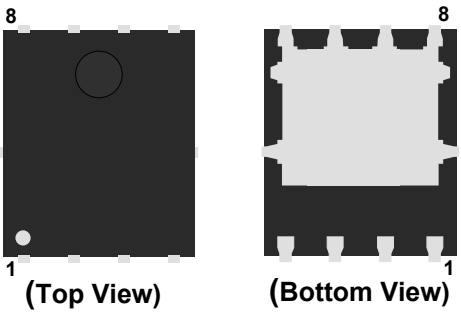
PJMG10H35PDN
P-Channel Enhancement Mode Power MOSFET

Product Summary

- V_{DS}= -100V,I_D= -35A
- $R_{DS(on)}$<46.3mΩ @V_{GS}= -10V
- $R_{DS(on)}$<58.3mΩ @V_{GS}= -4.5V

PDFN5x6-8L



Features

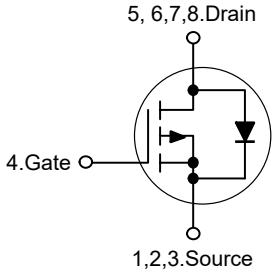
- Advanced Split Gate Trench Technology
- 100% Avalanche Tested
- RoHS Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3

Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain

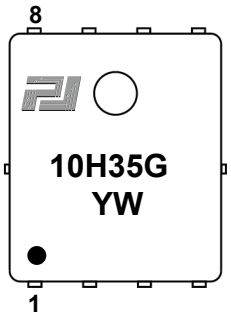
Application

- Load Switch
- PWM Application
- Power Management

Schematic Diagram



Marking Code



Absolute Maximum Ratings

Ratings at 25℃ case temperature unless otherwise specified.

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$-V_{DS}$	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	T_C=25°C	$-I_D$	35	A
	T_C=100°C		21	
Drain Current-Pulsed Note1		$-I_{DM}$	140	A
Single Pulse Avalanche Energy Note2		E_{AS}	110	mJ
Maximum Power Dissipation		P_D	97	W
Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Thermal Characteristics

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.28	°C/W

Electrical Characteristics

(T_J=25℃ unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$-V_{(BR)DSS}$	V_{GS}=0V,I_D=-250μA	100	--	--	V
Zero Gate Voltage Drain Current	$-I_{DSS}$	V_{DS}=-80V,V_{GS}=0V	--	--	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage Note3	$-V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	1.4	2	2.6	V
Drain-Source On-Resistance Note3	$R_{DS(on)}$	V_{GS}=-10V,I_D=-12A	--	35.6	46.3	mΩ
		V_{GS}=-4.5V,I_D=-8A	--	45	58.5	mΩ
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=-25V,V_{GS}=0V, f=1MHz	--	1230	--	pF
Output Capacitance	C_{oss}		--	620	--	pF
Reverse Transfer Capacitance	C_{rss}		--	44	--	pF
Total Gate Charge	Q_g	V_{DS}=-50V,I_D=-15A, V_{GS}=-10V	--	19	--	nC
Gate-Source Charge	Q_{gs}		--	7	--	nC
Gate-Drain Charge	Q_{gd}		--	4	--	nC
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-50V, I_D=-15A, V_{GS}=-10V, R_{GEN}=6Ω	--	12	--	nS
Turn-on Rise Time	t_r		--	55	--	nS
Turn-off Delay Time	$t_{d(off)}$		--	40	--	nS
Turn-off Fall Time	t_f		--	75	--	nS
Source-Drain Diode Characteristics						
Diode Forward Voltage Note3	$-V_{SD}$	V_{GS}=0V,I_S=-12A	--	--	1.2	V
Diode Forward Current	$-I_S$		--	--	35	A
Body Diode Reverse Recovery Time	t_{rr}	I_F=-15A,di/dt=100A/us	--	50	--	ns
Body Diode Reverse Recovery Charge	Q_{rr}		--	125	--	nC

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. EAS Condition: Tj=25℃,V_{DD}=-50V,V_G=-10V,R_G=25Ω,L=0.5mH,I_{AS}=-21A.
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Test Circuit

P-MOS

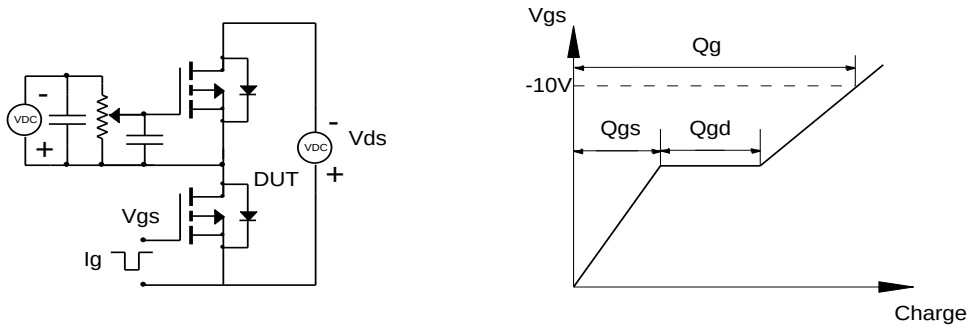


Figure 1: Gate Charge Test Circuit & Waveform

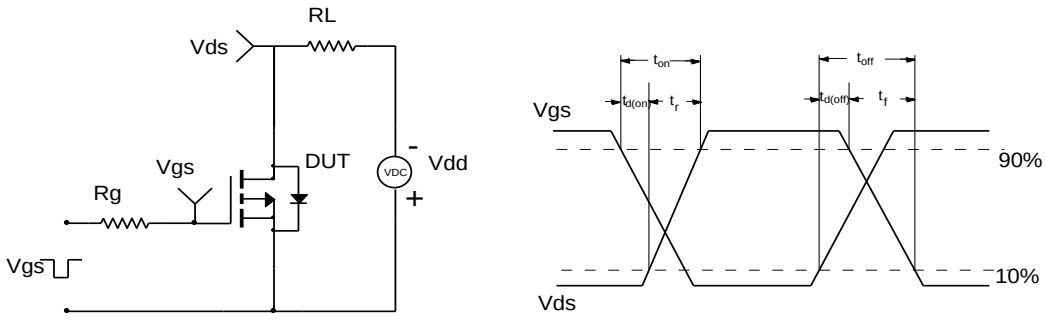


Figure 2: Resistive Switching Test Circuit & Waveform

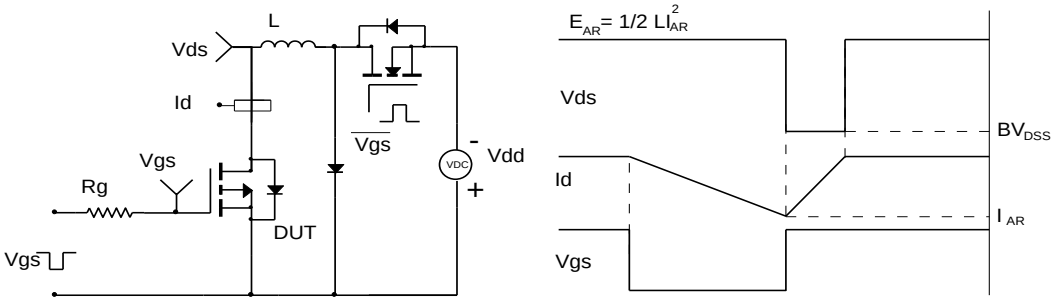


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

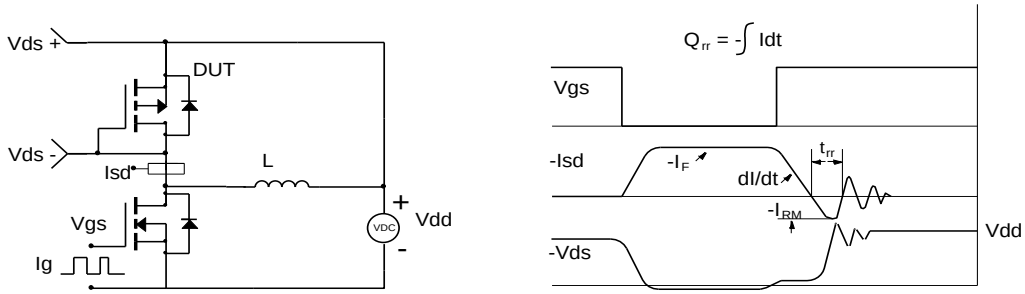
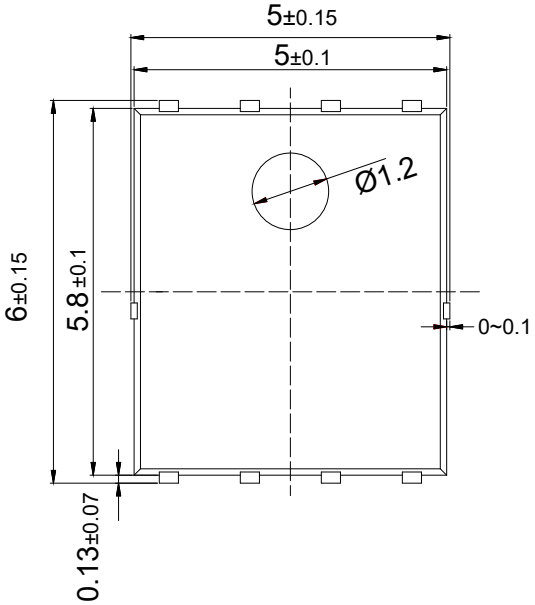


Figure 4: Diode Recovery Test Circuit & Waveform

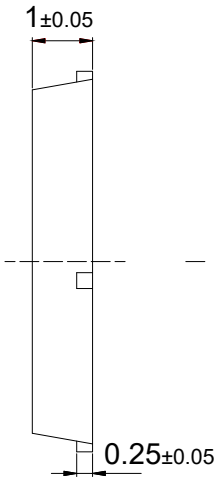
Package Outline

PDFN5x6-8L

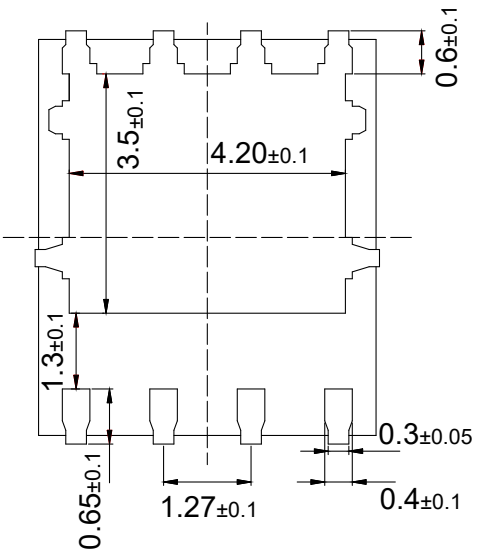
Dimensions in mm



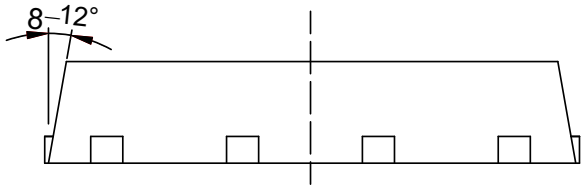
TOP VIEW



RIGHT VIEW



BOTTOM VIEW



SIDE VIEW