

Features

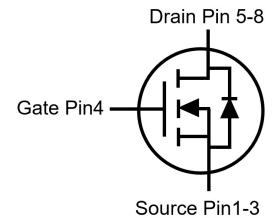
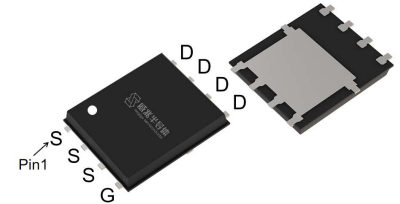
- Enhancement mode
- Ultra Low RDS(on) to minimize conduction losses
- VitoMOS® II Technology
- 100% Avalanche tested, 100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses
- AEC-Q101 Compliant



Part ID	Package Type	Marking	Packing
VS4802GPHT-IG	PDFN5x6	4802GPH	3000PCS/Reel

V_{DS}	40	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	0.7	mΩ
$I_D(\text{Silicon limited})$	355	A

PDFN5x6



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		40	V
V_{GS}	Gate-source voltage		± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	205	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$	355	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	251	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	1000	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	44	A
		$T_A = 70^\circ\text{C}$	37	A
E_{AS}	Avalanche energy, single pulsed ②		961	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	205	W
		$T_C = 100^\circ\text{C}$	103	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 70^\circ\text{C}$	2.2	W
T_J, T_{STG}	Operating junction and storage temperature range		-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.61	0.73	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	40	48	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250uA	40	--	--	V
I _{DSS}	Zero gate voltage drain current(T _j =25°C)	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _j =125°C)⑦	V _{DS} =40V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-body leakage current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} ,I _D =250μA	2.4	3.0	3.6	V
R _{DS(on)}	Drain-source on-state resistance ⑧	V _{GS} =10V, I _D =40A	--	0.7	0.9	mΩ
		(T _j =100°C)⑦	--	1	--	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	120	--	S
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ⑦	V _{DS} =20V,V _{GS} =0V, f=100kHz	--	5945	--	pF
C _{oss}	Output capacitance ⑦		--	1515	--	pF
C _{rss}	Reverse transfer capacitance ⑦		--	95	--	pF
R _g	Gate resistance	f=1MHz	--	2.6	--	Ω
Q _g	Total gate charge ⑦	V _{DS} =20V,I _D =40A, V _{GS} =10V	--	82	--	nC
Q _{gs}	Gate-source charge ⑦		--	24	--	nC
Q _{gd}	Gate-drain charge ⑦		--	12	--	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =20V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	12	--	ns
T _r	Turn-on rise time		--	69	--	ns
T _{d(off)}	Turn-off delay time		--	63	--	ns
T _f	Turn-off fall time		--	39	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A,V _{GS} =0V	--	0.78	1	V
T _{rr}	Reverse recovery time ⑦	V _{DD} =30V, I _{sd} =40A, V _{GS} =0V	--	42	--	ns
Q _{rr}	Reverse recovery charge ⑦	di/dt=100A/μs	--	30	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This value is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 62A, V_{GS} = 10V; 100% FT tested at L = 0.1mH, I_{AS} = 65A.
- ③ The power dissipation Pd is based on T_j(max), using junction-to-case thermal resistance RθJC.
- ④ The power dissipation Pdsm is based on T_j(max), using junction-to-ambient thermal resistance RθJA.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles 2%.

Typical Characteristics

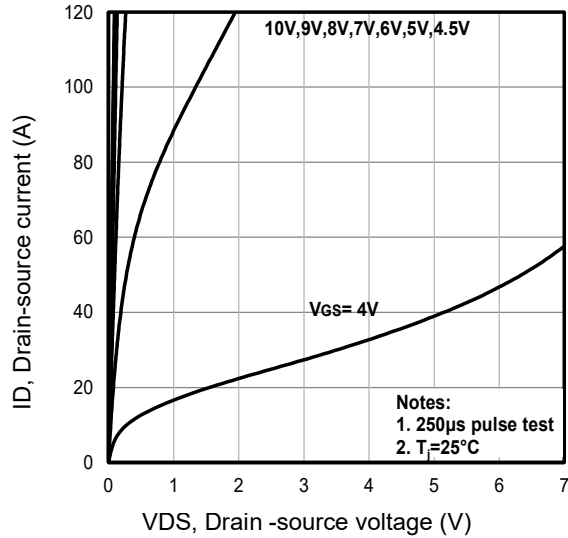


Fig1. Typical output characteristics

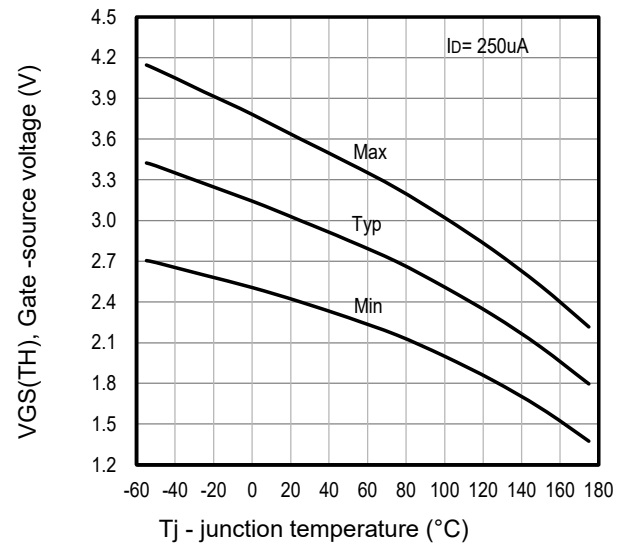


Fig2. Typical $V_{GS(TH)}$ gate-source voltage Vs. T_j

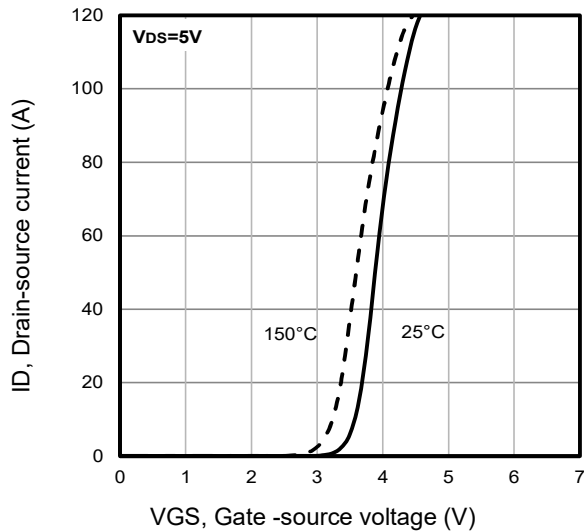


Fig3. Typical transfer characteristics

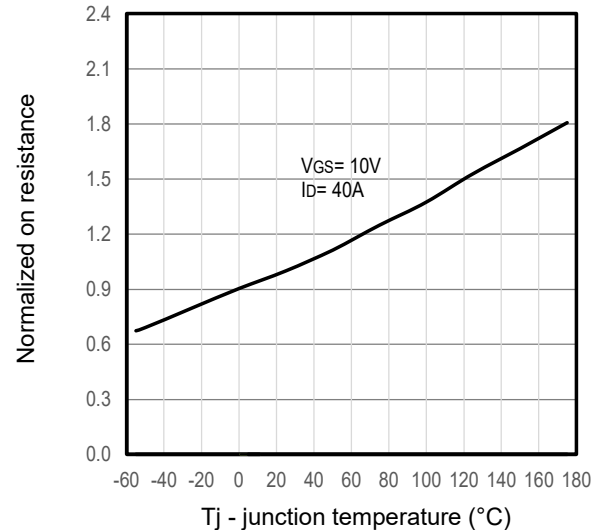


Fig4. Typical normalized on-resistance Vs. T_j

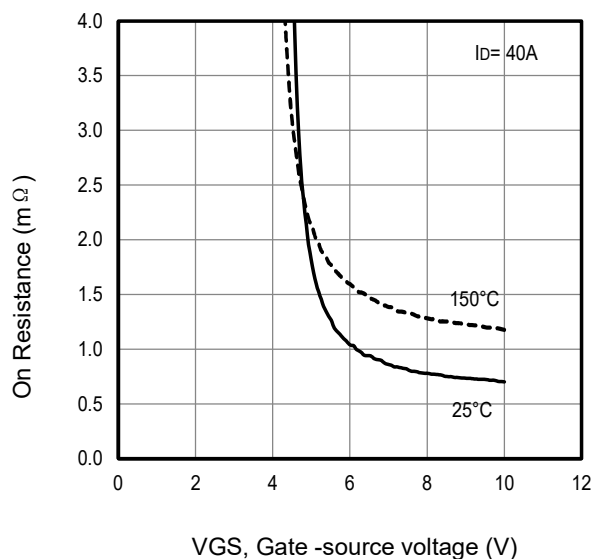


Fig5. Typical on resistance Vs gate-source voltage

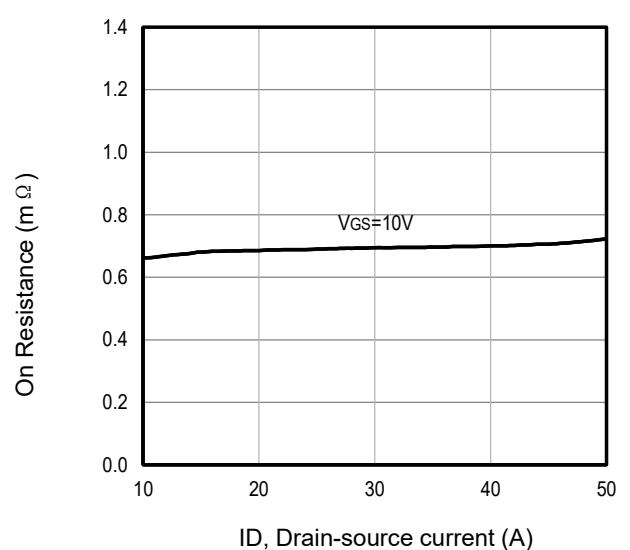


Fig6. Typical on resistance Vs drain current

Typical Characteristics

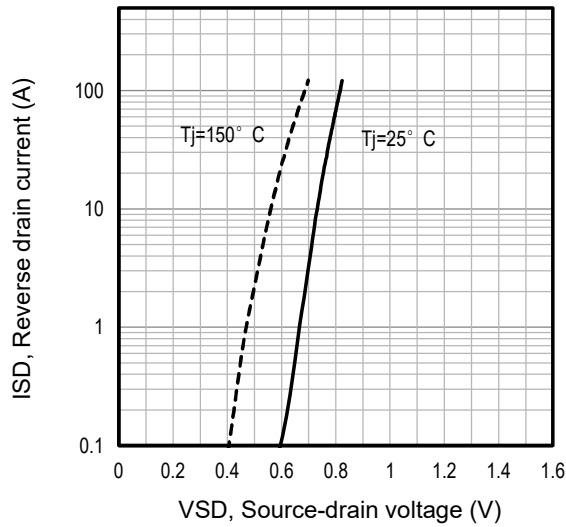


Fig7. Typical source-drain diode forward voltage

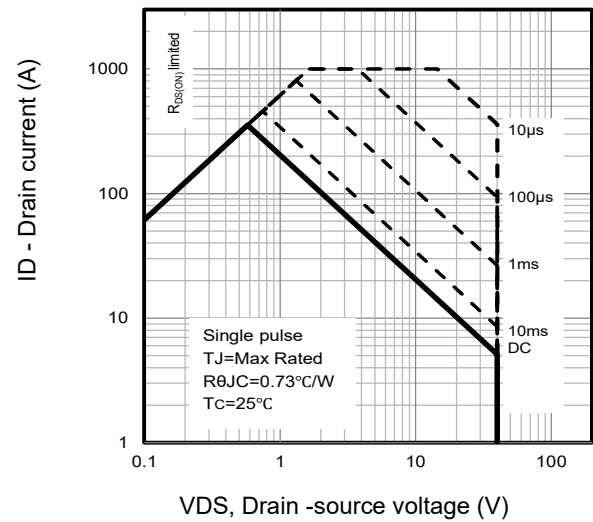


Fig8. Maximum safe operating area

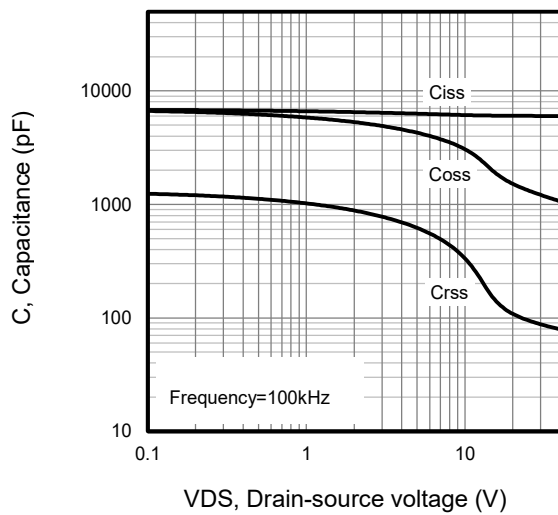


Fig9. Typical capacitance Vs. drain-source voltage

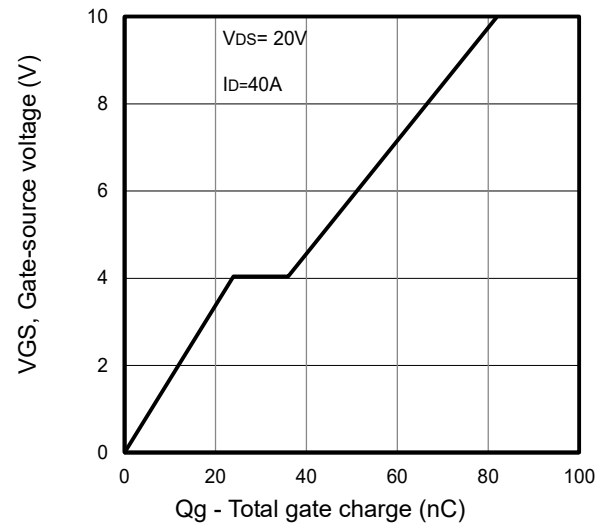


Fig10. Typical gate charge Vs. gate-source voltage

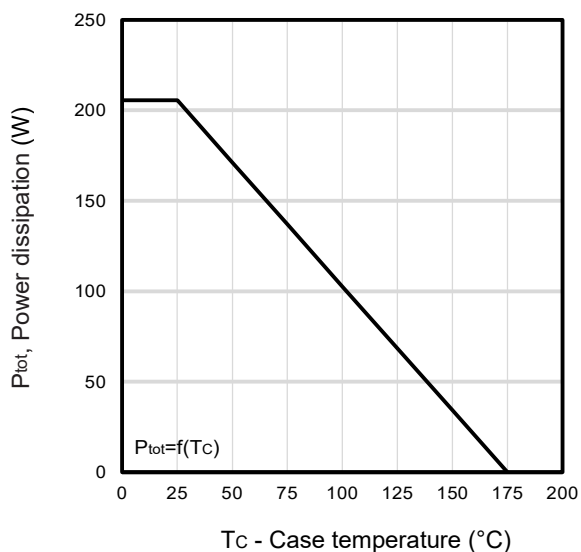


Fig11. Power dissipation Vs. case temperature

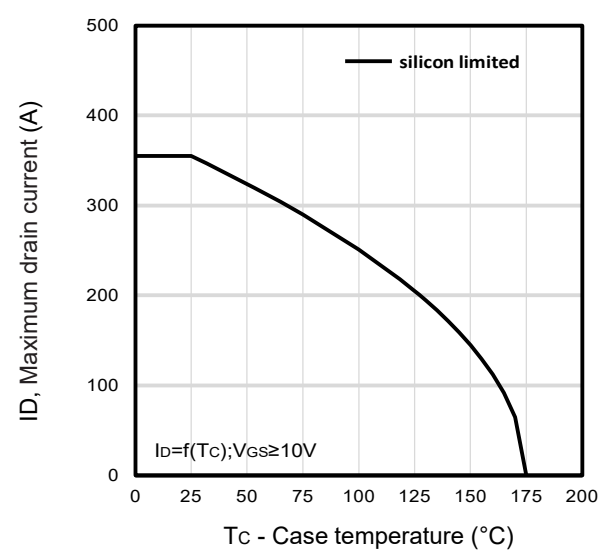


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

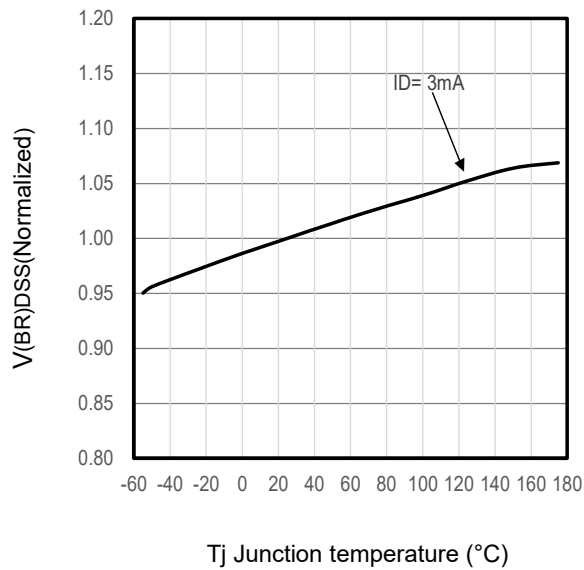


Fig13. Typical $V(BR)DSS$ Vs T_j

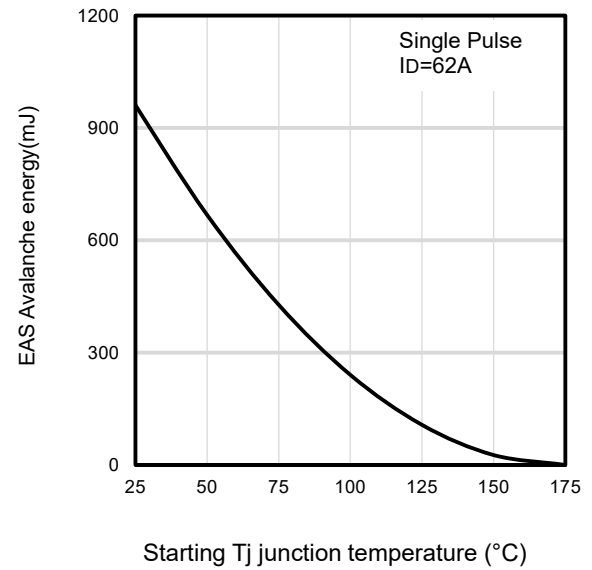


Fig14. Maximum avalanche energy vs temperature ($^{\circ}C$)

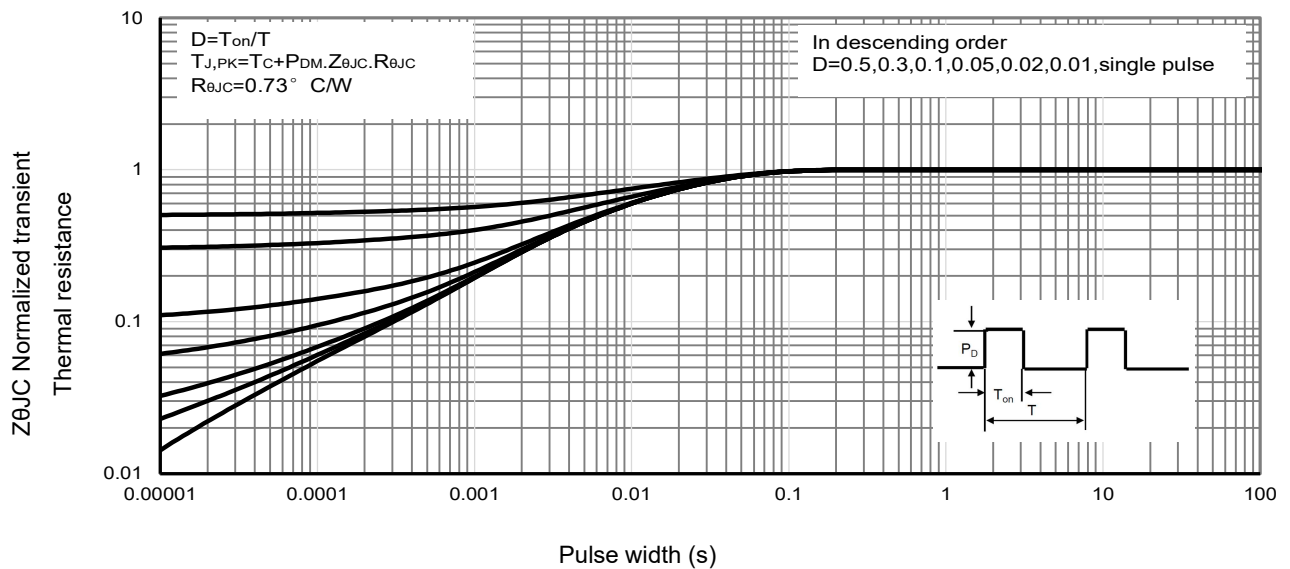


Fig15 . Normalized maximum transient thermal impedance

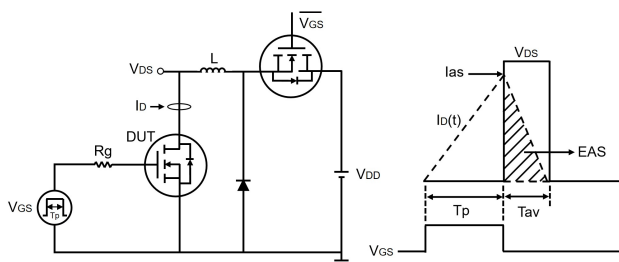


Fig16. Unclamped Inductive Test Circuit and waveforms

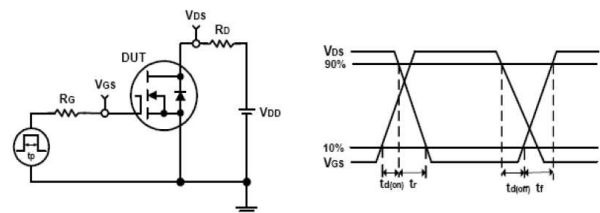
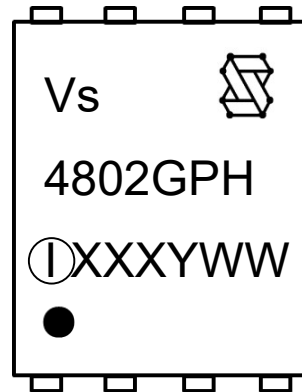


Fig17. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (4802GPH)

3rd line: Date code (ⓈXXXYYWW)

Ⓢ: Fixed printing

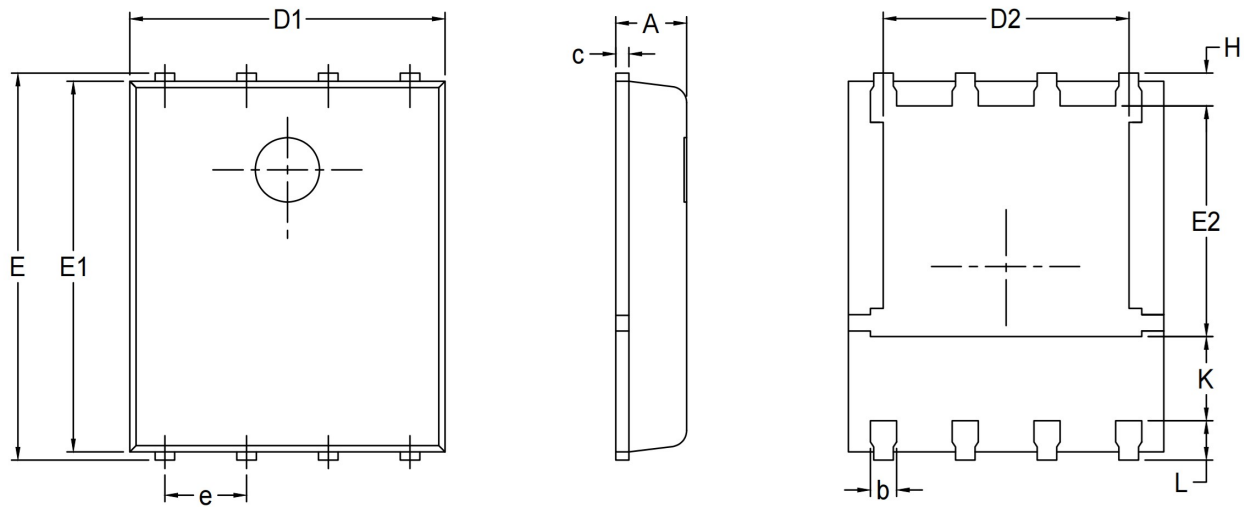
XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71

Notes:

- 1.Refer to JEDEC MO-240 variation AA.
- 2.Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
- 3.Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.