24C32

DATASHEET

Specification Revision History：

Version	Date	Description
V1.0	2019/05	New
V1.1	2021/01	Modify Ordering Information
V1.2	2025/02	Modify Ordering Information
V1.3	2025/03	Add application precautions and overall typesetting.

General Description

FEATURES

The 24C32 is a 32-Kbit I2C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 4096 × 8bits, which is organized in 32-byte per page. 24C32 provides the following devices for different application.

■Single Supply Voltage and High Speed
○ Minimum operating voltage down to 1.7V
○ 1 MHz clock from 2.5V to 5.5V
○ 400kHz clock from 1.7V to 2.5V
■Low power CMOS technology
○ Read current 400uA, maximum
○ Write current 1.6mA, maximum
■Schmitt Trigger, Filtered Inputs for Noise Suppression
■Sequential & Random Read Features
■32 byte Page Write Modes, Partial Page Writes Allowed
■Write protect of the whole memory array
■Additional Write Lockable Page
■Additional 128-bit Serial Number
■Self-timed Write Cycle (5ms maximum)
■High Reliability
○ESD(HBM): 6KV
○ Endurance: 1 Million Write Cycles
○ Data Retention: 100 Years
○ LATCH UP Capability: +/- 200mA
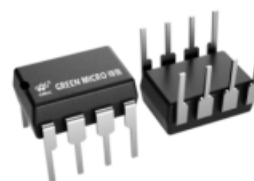■Package: PDIP, SOP, TSSOP, DFN, SOT23-5 and WLCSP

## The appearance of the product

TSSOP-8
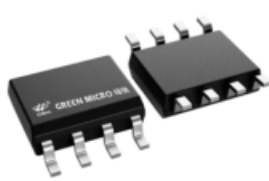
SOP-8

DIP-8

SOT-23-5

MSOP-8

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
AT24C32CDR165	SOP-8	24C32 A65或165	REEL	4000PCS/REEL
AT24C32CP165	DIP-8	24C32 165	TUBE	2000PCS/BOX
AT24C32S5165	SOT-23-5	24C32 A65	REEL	3000PCS/REEL
AT24C32T165	TSSOP-8	24C32 A65	REEL	3000PCS/REEL
AT24C32MDR165	MSOP-8	24C32 A65	REEL	3000PCS/REEL
GM24C32DR	SOP-8	24C32 S165	REEL	4000PCS/REEL
GM24C32P	DIP-8	24C32 D165	TUBE	2000PCS/BOX
GM24C32S5	SOT-23-5	24C32 O165	REEL	3000PCS/REEL
GM24C32T	TSSOP-8	24C32 T165	REEL	3000PCS/REEL
GM24C32MDR	MSOP-8	24C32 M165	REEL	3000PCS/REEL

1.Pin Configuration

1.1 Figure 1-1 Pin Configuration

PDIP/SOP/TSSOP/DFN

SOT23-5

(BOTTOM VIEW)

6-BALL WLCSP
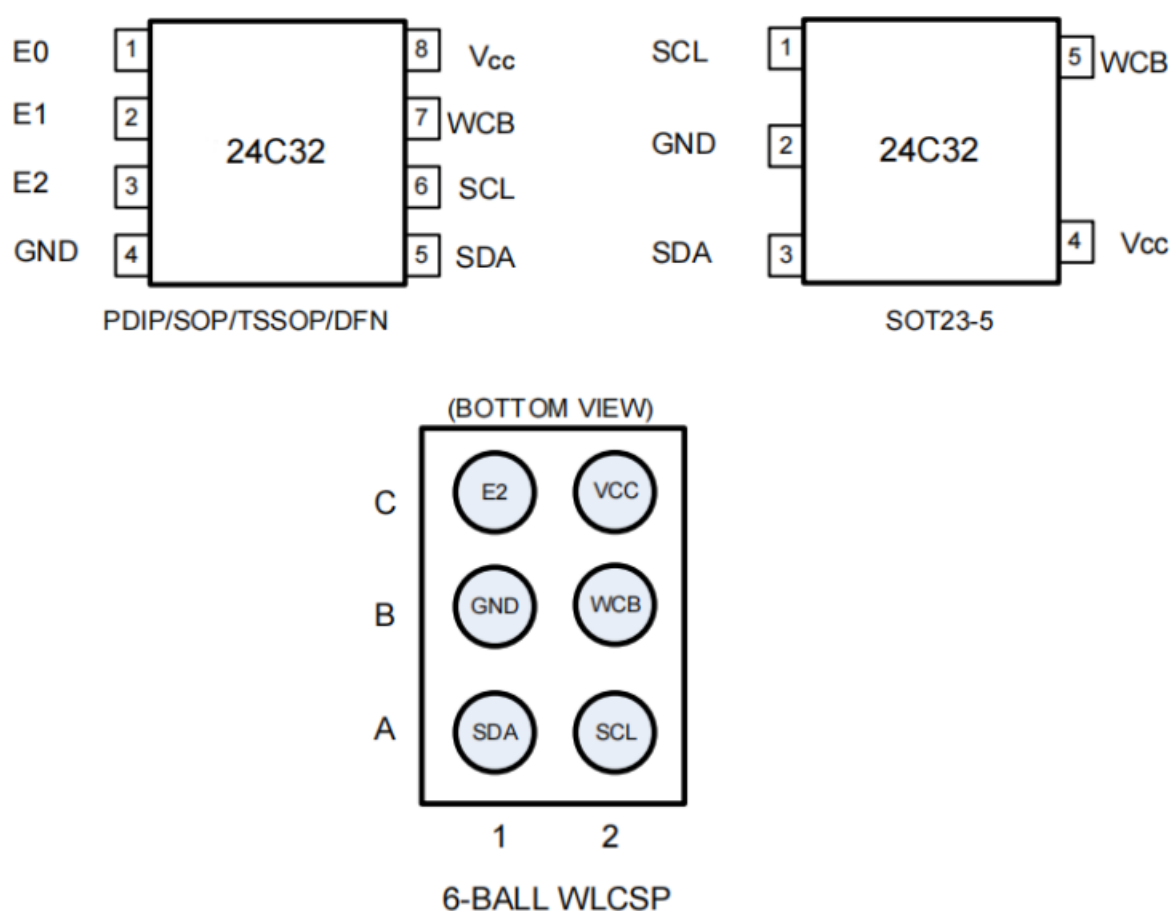
1.2 Pin Definition

Table 1-1 Pin Definition

Pin	Name	Type	Description
1	E0	I/O	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	GND	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	VCC	Power	Power

1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (E2, E1, E0): The E2, E1, and E0 pins are device address inputs. Typically, the E2, E1, and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1, and E0 pins will be internally pulled down to GND.

Write Control (WCB): The Write Control input, when WCB is connected directly to VCC, all write operations to the memory are inhibited. When connected to GND, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to GND.

Block Diagram

Figure 2-1 Block Diagram

3. Electrical Characteristics

Absolute Maximum Ratings

- Storage Temperature ....-65°C to +150°C

- Operation Temperature .... -40°C to +125°C

- Maximum Operation Voltage 6.25V

- Voltage on Any Pin with

   Respect to Ground........................ -1.0V to (Vcc+1.0) V

- DC Output Current ....5.0 mA

   NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-1 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (E0,E1,E2,WCB,SCL)	6	pF	V_{IN}=GND

Note: [1] Test Conditions: TA = 25℃, F = 1MHz, Vcc = 5.0V.

Table 3-2 DC Characteristics (Unless otherwise specified, VCC = 1.7V to 5.5V, TA = −40℃ to 125℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	24C32-MI
		1.8	-	5.5	V	24C32-NK
		2.5	-	5.5	V	24C32-DE
Isb	Standby Current	-	-	1.0	uA	Vcc = 3.3V, TA = 85℃
		-	-	3.0	uA	Vcc = 5.5V, TA = 85℃
		-	-	6.0	uA	Vcc = 5.5V, TA = 105℃
		-	-	10.0	uA	Vcc = 5.5V, TA = 125℃
ICC1	Supply Current	-	0.2	0.4	mA	Vcc=5.5V, Read at 400 Khz
ICC2	Supply Current	-	0.8	1.6	mA	Vcc=5.5V Write at 400 Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	µA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	µA	V_{OUT} = V_{CC} or GND
V_{IL}	Input Low Level	−0.6	-	0.3VCC	V	
V_{IH}	Input High Level	0.7VCC	-	VCC+0.5	V	
V_{OL1}	Output Low Level VCC = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level VCC = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-3 AC Characteristics (Unless otherwise specified, VCC = 1.7V to 5.5V, TA = −40°C to 125°C, CL=100pF, Test Conditions are listed in Notes [2])

Symbol	Parameter	1.7≤VCC<2.5			2.5≤VCC≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	µs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	µs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	µs
t_{I}	Noise Suppression Time	-	-	0.1	-	-	0.05	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	µs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	µs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	µs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	µs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	µs
t_{R}	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	µs
t_{F}	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	µs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	µs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	µs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	µs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	µs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes:[1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

✧ R_L (connects to V_{CC}): 1.3k (2.5V, 5.5V), 10k (1.7V)

✧ Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

✧ Input rise and fall times: ≤50ns

✧ Input and output timing reference voltages: 0.5V_{CC}

Table 3-4 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

Figure 3-1 Bus Timing
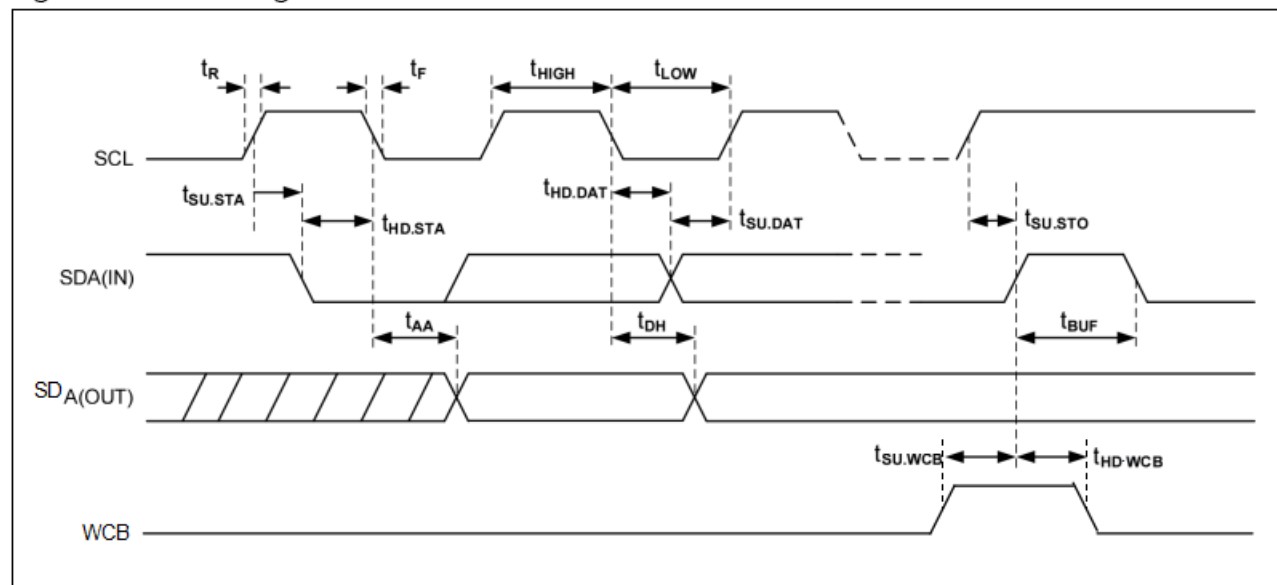
Figure 3-2 Write Cycle Timing
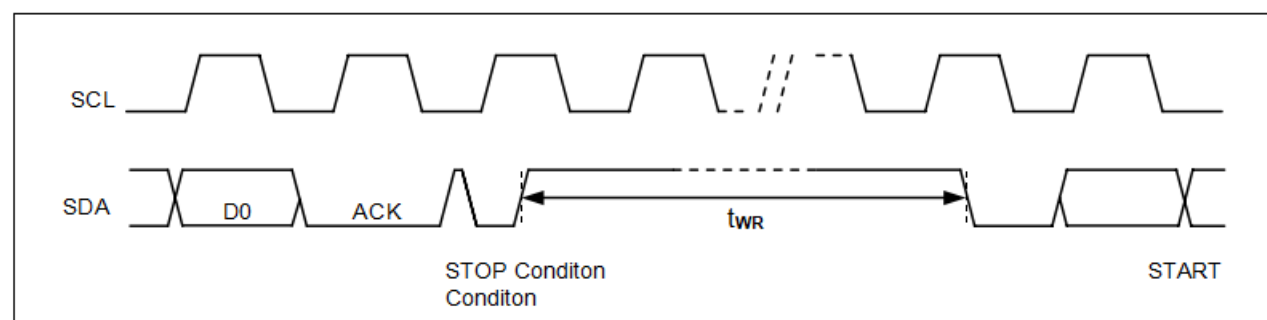
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 4-1 Data Validity
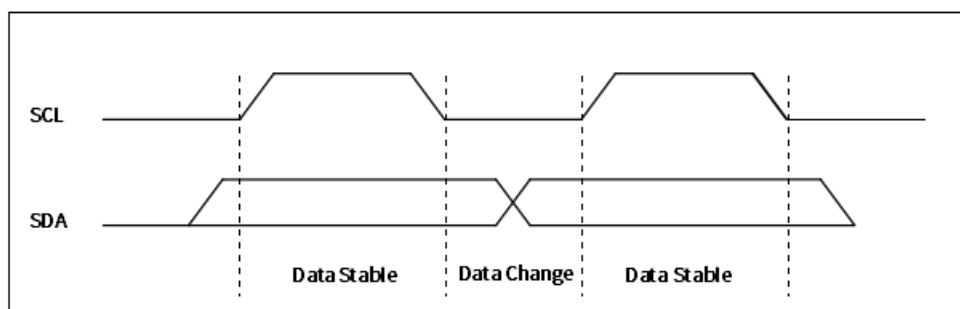
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the 24C32 in a standby power mode (see Figure 4-2).

Figure 4-2 Start and Stop Definition
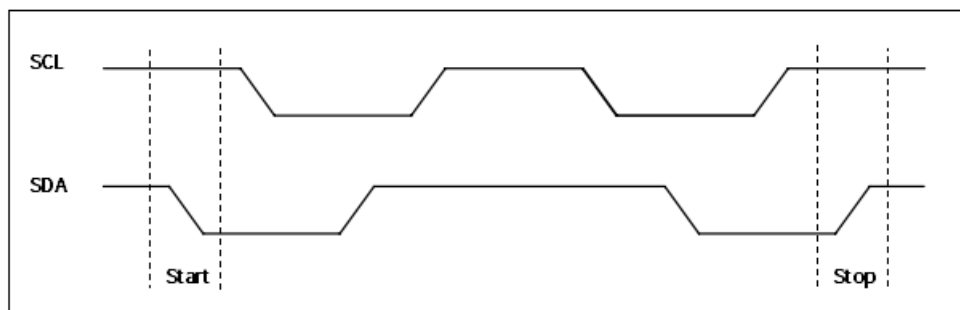
4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the 24C32 in 8-bit words. The 24C32 sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

**Figure 4-3 Output Acknowledge**
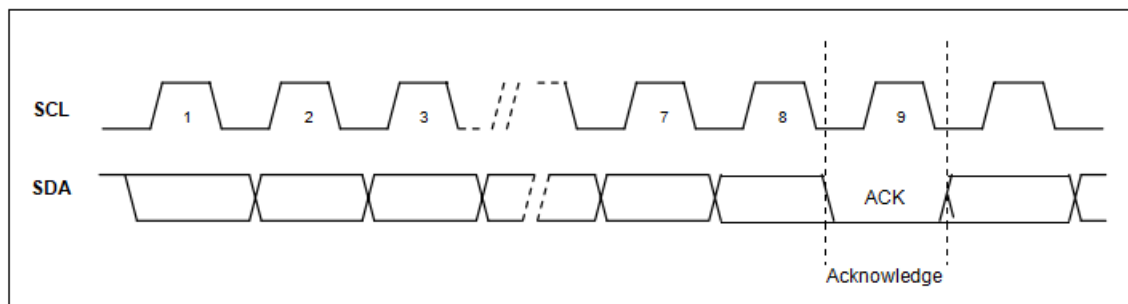
4.5 Standby Mode

The 24C32 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these

steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset
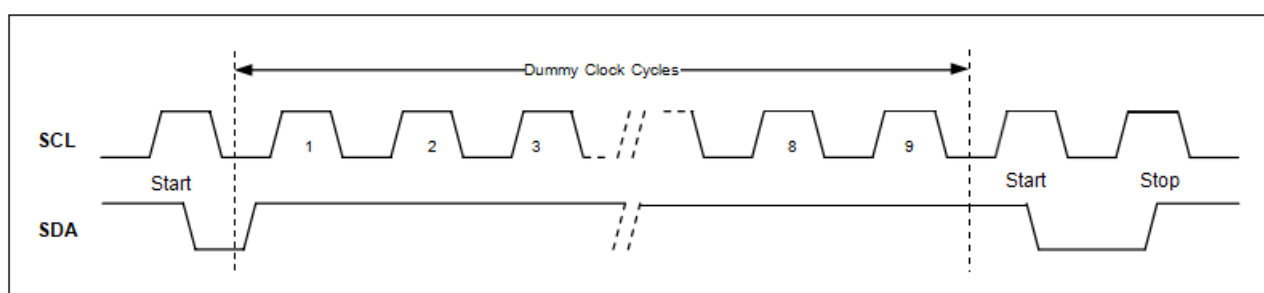
4.7 Device Addressing

The 24C32 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	E2	E1	E0	R/W
ID Page	1	0	1	1	E2	E1	E0	R/W
ID LOCK Bit	1	0	1	1	E2	E1	E0	R/W
Serial Number	1	0	1	1	E2	E1	E0	1

Table 4-2 First Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	X	X	X	X	A11	A10	A9	A8
ID Page	X	X	X	X	0	0	X	X
ID LOCK Bit	X	X	X	X	X	1	X	X
Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Second Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
ID Page	X	X	X	A4	A3	A2	A1	A0
ID LOCK Bit	X	X	X	X	X	X	X	X
Serial Number	X	X	X	X	A3	A2	A1	A0

The three E2, E1, and E0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The E2, E1, and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.8 Data Security

24C32 has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

5. Instructions

5.1 Write Operations

5.1.1 BYTE WRITE

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the 24C32 will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the 24C32 will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the 24C32 enters an internally timed write cycle, all inputs are disabled during this write cycle and the 24C32 will not respond until the write is complete (see Figure 5-1).

Figure 5-1 Byte Write
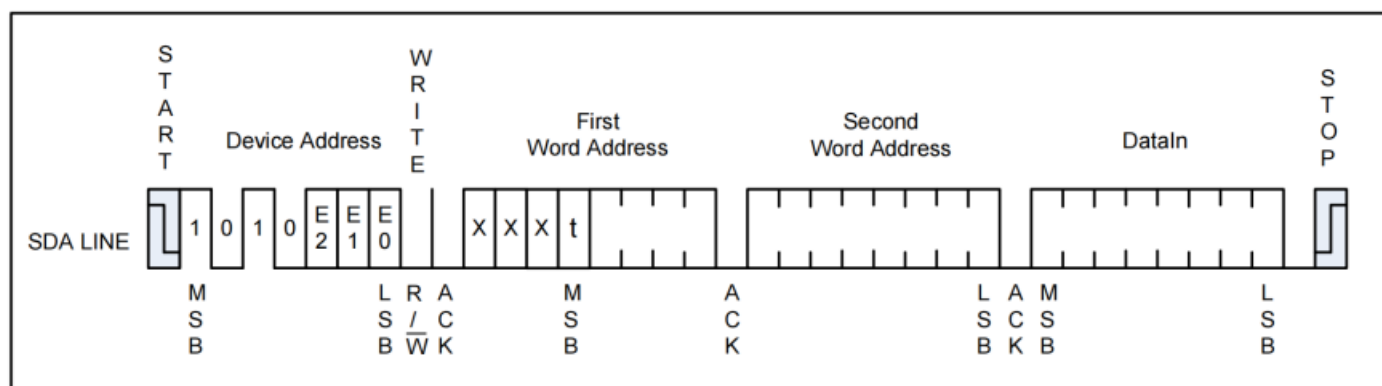
Notes: [1] x means don't care bits.

[2] t means don't care bit for 24C32

5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the 24C32 acknowledges receipt of the first data word, the master can transmit more data words. The 24C32 will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write
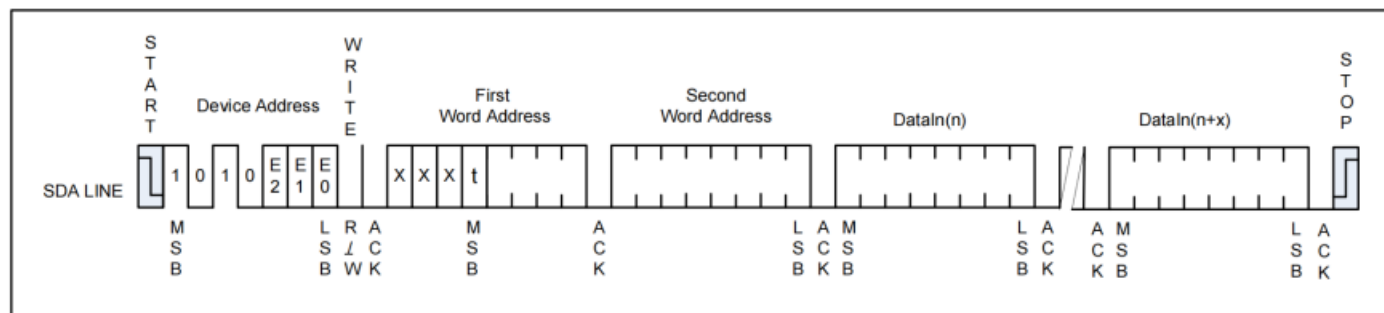
Notes: [1] x means don't care bits.

[2] t means don't care bit for 24C32

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location.

When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the 24C32, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the 24C32 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the 24C32 respond with a "0", allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

● Device type identifier = 1011b

● MSB address bits A15/A5 are don't care except for address bit A11/A10 which must be '00'.

● LSB address bits A4/A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

● Device type identifier = 1011b

● Address bit A10 must be '1'; all other address bits are don'tcare

● The data byte must be equal to the binary value xxxxxx1x, where x is don'tcare

5.2 Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the 24C32, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 5-3).
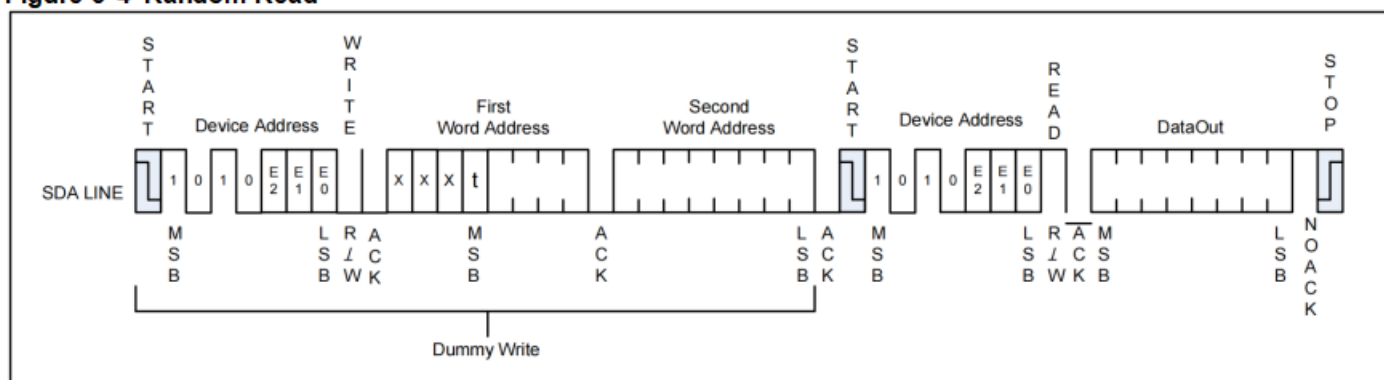
Figure 5-3 Current Address Read
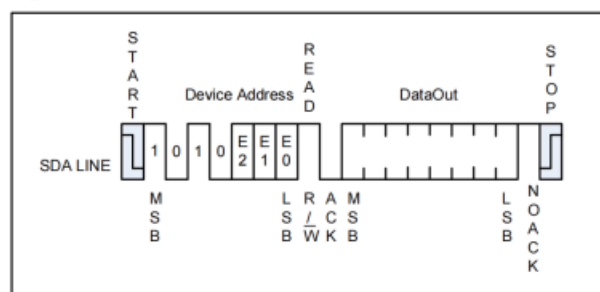
5.2.2 Random Read

A Random Read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the 24C32, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The 24C32 acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-4).

Figure 5-4 Random Read

Notes: [1] x means don't care bits.

[2] t means don't care bit for 24C32A

5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the 24C32 receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-5)

Figure 5-5 Sequential Read
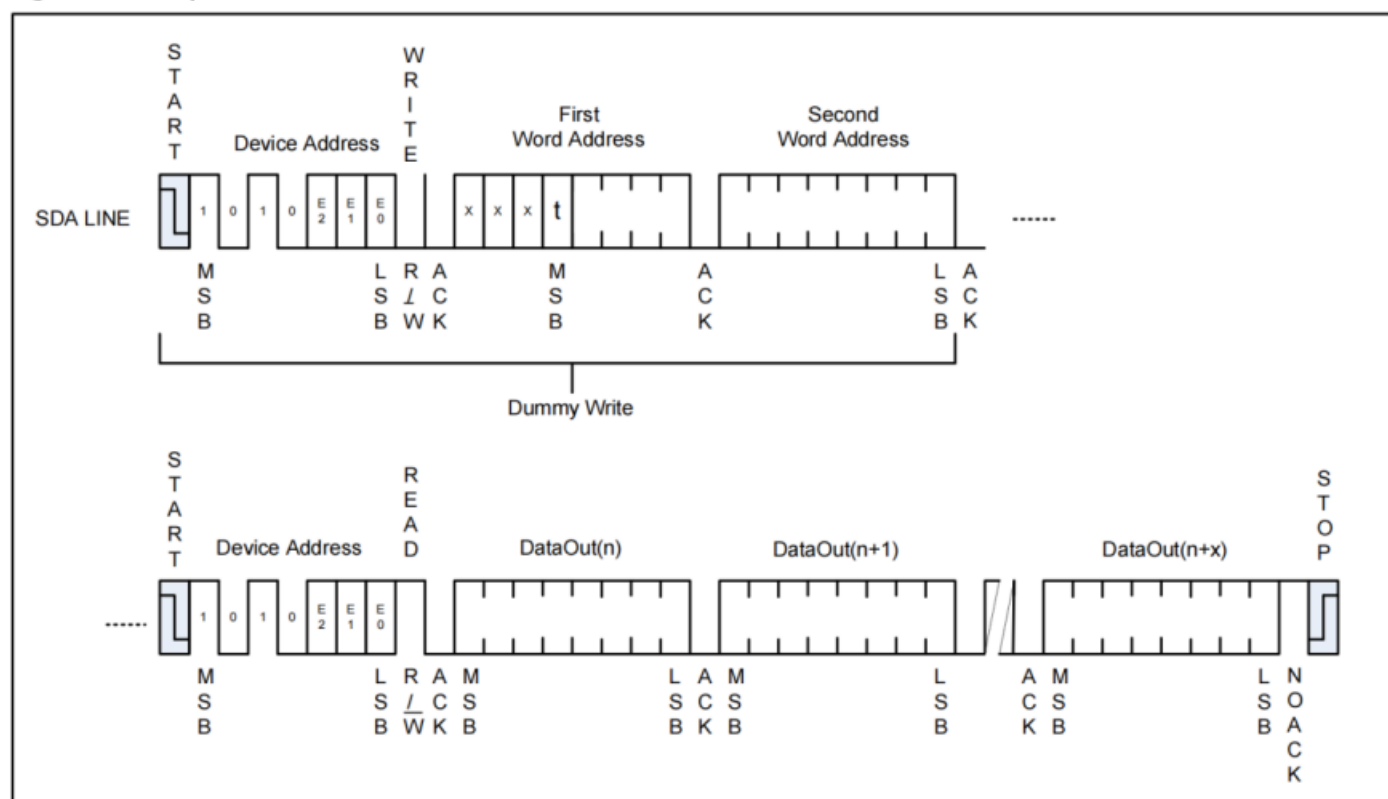
Notes: [1] x means don't care bits.

[2] t means don't care bit for 24C32

5.2.4 Read Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page

boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.2.5 Read Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

Figure 5-5 Lock Status Read (When Identification page locked, return NoACK after one data byte)
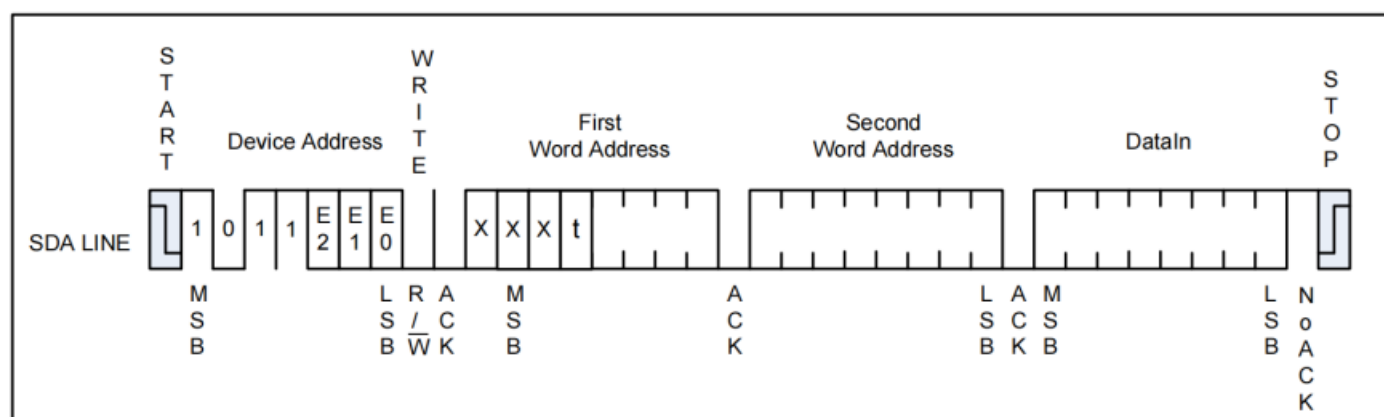
5.2.6 Read Serial Number

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 4-1 on page 9, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A11 and A10 of the word address, regardless of

the intended address as depicted in Table 4-2 on page 9. If a word address other than '10' is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in rolling over to the first byte. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 5-6)
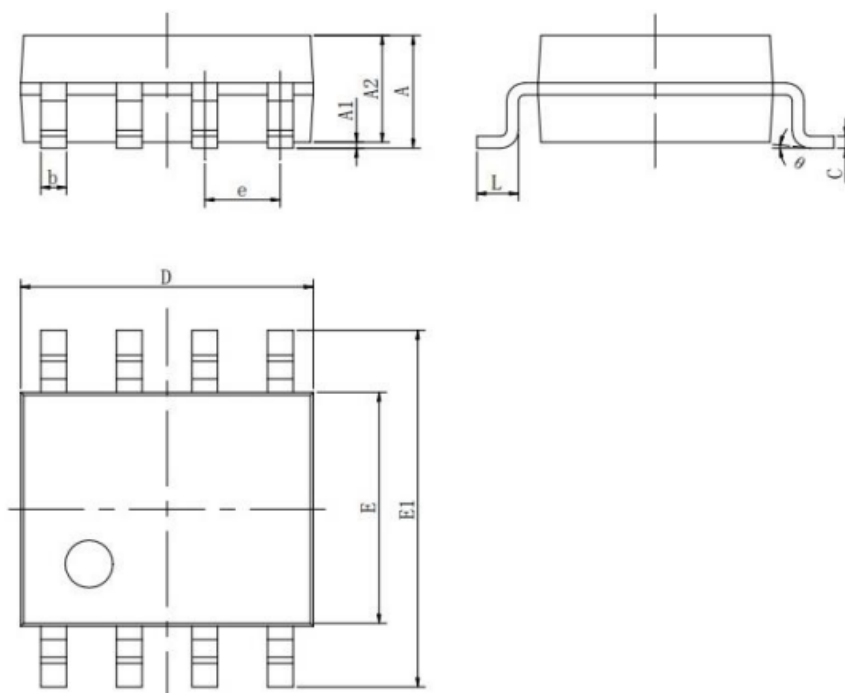
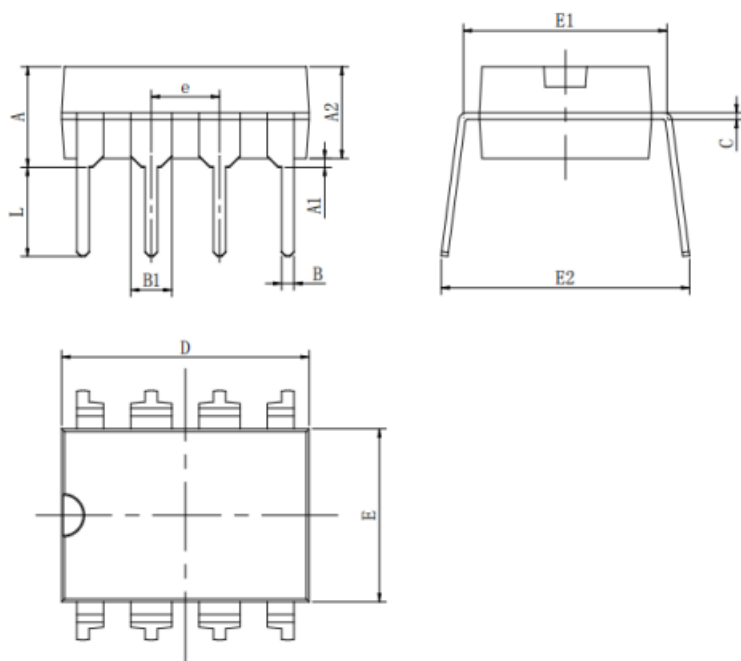Figure 5-6 Serial Number Read
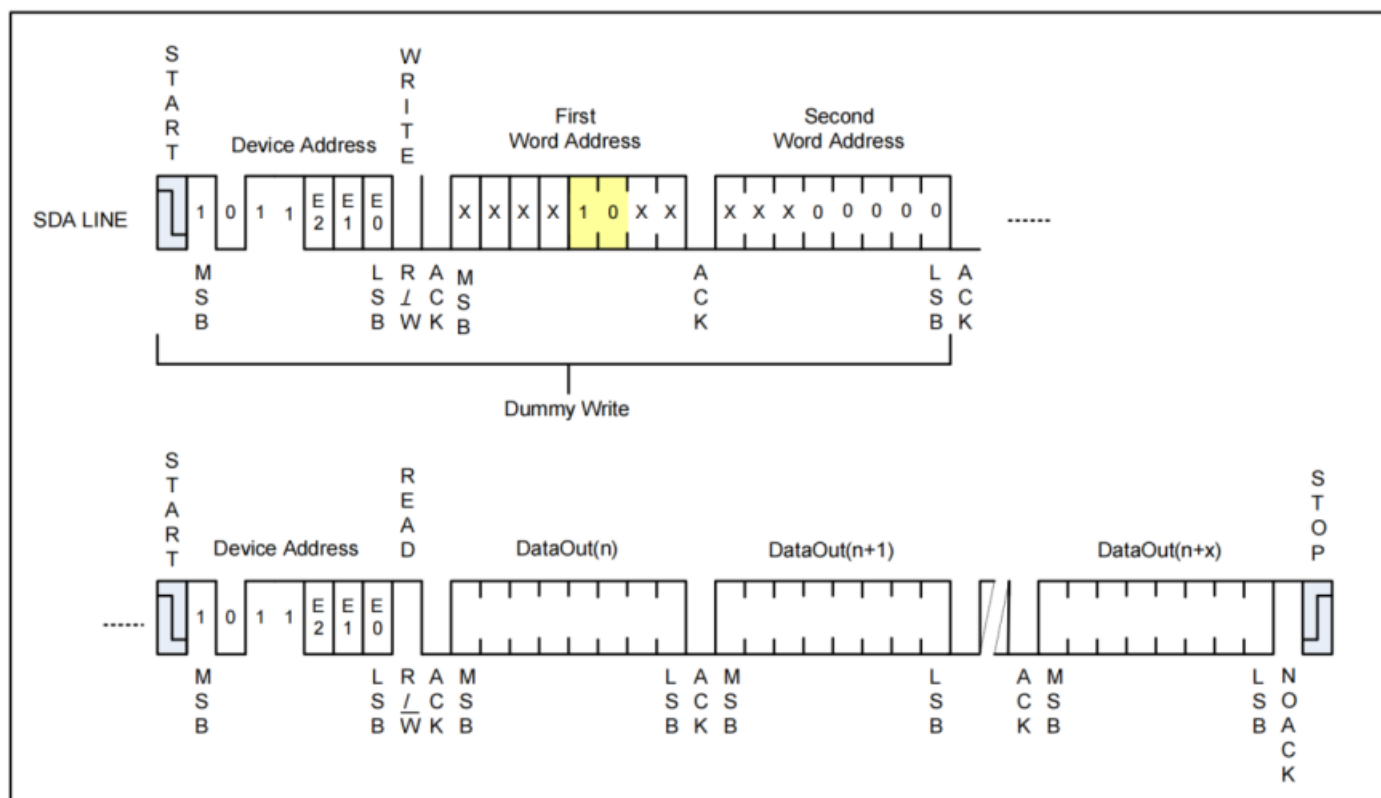
Outline Dimensions

SOP-8 — Unit : mm

Symbol	DimensionsInMillimeters		DimensionsInInches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.050	0.250	0.004	0.010
A2	1.250	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.006	0.010
D	4.780	5.000	0.185	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP-8   Unit:mm

Symbol	DimensionsInMillimeters		DimensionsInInches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

MSOP-8

Unit : mm
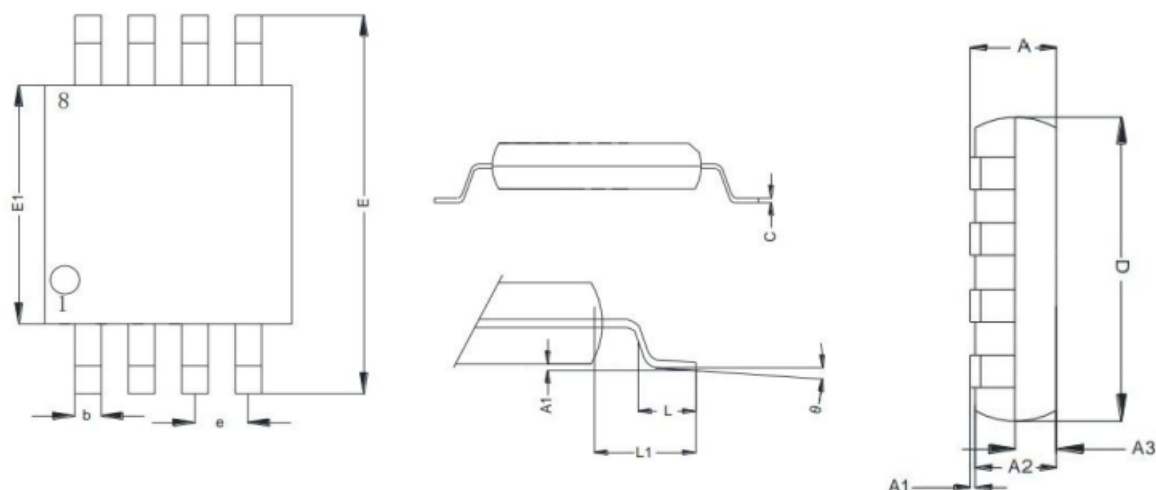
Symbol	Min	Typ	Max
A			1.100
A1	0.050		0.150
A2	0.750	0.850	0.950
A3	0.300	0.350	0.400
b	0.280		0.360
C	0.150		0.190
D	2.900	3.000	3.100
E	4.700	4.900	5.100
E1	2.900	3.000	3.100
e	-	0650	
L	0.400		0.700
L1		0.950	
θ	0		8°

TSSOP-8   Unit : mm
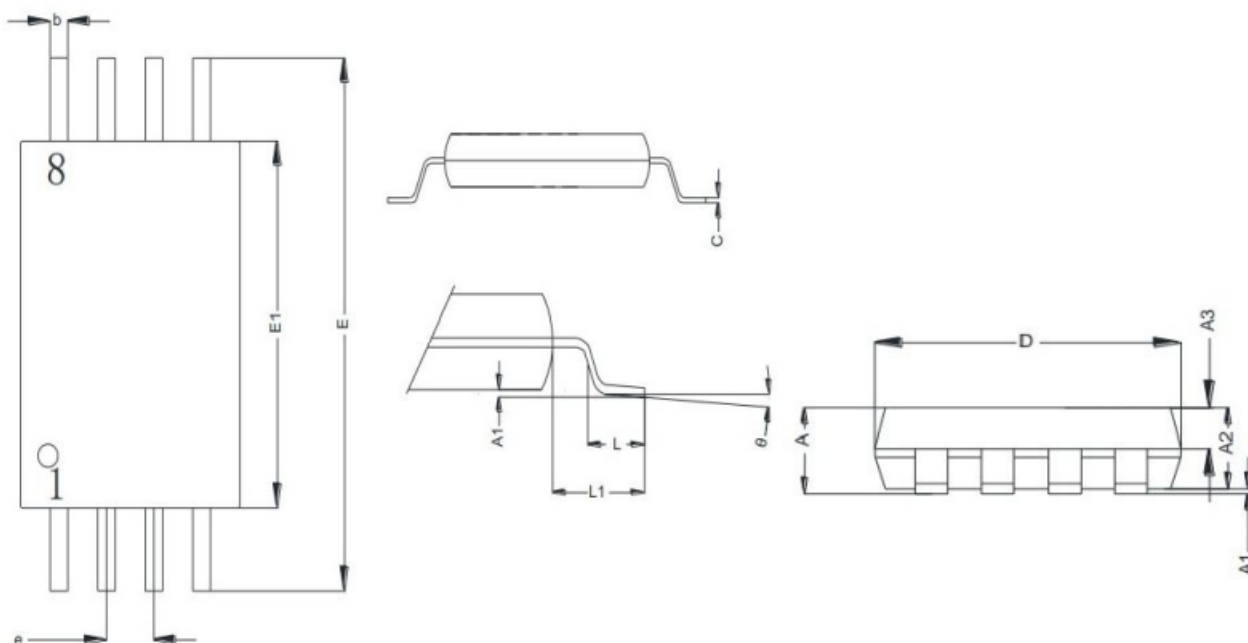
Symbol	Min	Typ	Max
A			1.200
A1	0.050	-	0.150
A2	0.900		
A3	0.390	0.440	0.490
b	0.200		0.280
C	0.090		0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e		0.650	
L	0.450	-	0.750
L1		1.000	-
θ	0		8°

SOT23-5

Unit : mm
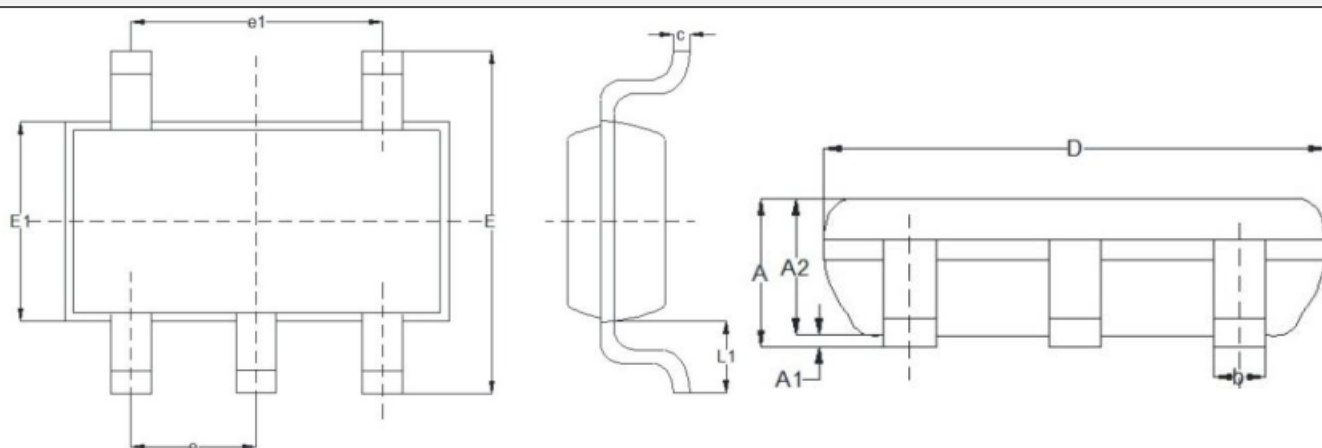
Symbol	Min	Typ	Max
A	1.000		1.250
A1	0.030		0.090
A2	1.050		1.150
c	0.080		0.200
D		2.900BSC	
E		2.800BSC	
E1		1.600BSC	
e		0.950BSC	
e1		1.900BSC	
L1		0.600REF	
b	0.300		0.450

DFN8(UN)

Unit : mm

TOP VIEW

EXPOSED THERMAL
PAD ZONE

BOTTOM VIEW

SIDE VIEW
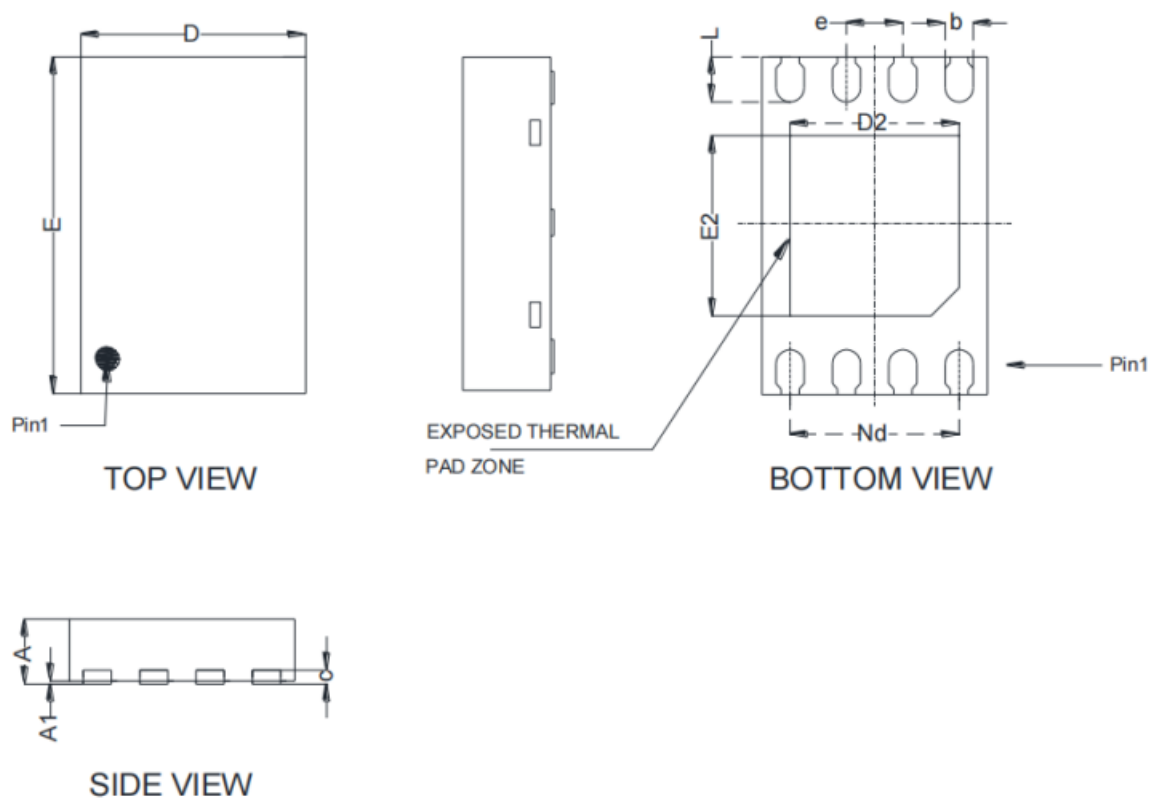
Symbol	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.18	0.24	0.30
D	1.90	2.00	2.10
D2	1.30		1.60
E	2.90	3.00	3.10
E2	1.20		1.70
e		0.50	
L	0.25	-	0.50
c	0.10	0.15	0.20
Nd	-	1.50	

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