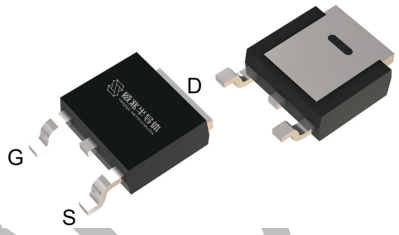
Features

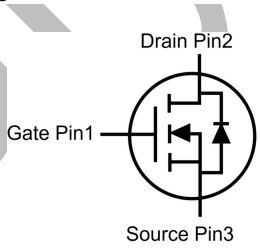
- Enhancement mode
- Super junction technology
- 100% Avalanche Tested, 100% Rg Tested

V_{DS}	600	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	230	mΩ
$I_{D(Silicon\ limited)}$	15	A

TO-252



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSD60R280S	TO-252	D60R280S	2500pcs/Reel

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		600	V
V_{GS}	Gate-source voltage		±30	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	15	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	15	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	9	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	30	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	1.9	A
		T_A=70°C	1.5	A
EAS	Maximum Avalanche energy, single pulsed ②		61	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	151	W
		T_C = 100°C	60	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	2.5	W
		T_A = 70°C	1.6	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 150	°C

Thermal Characteristics

Electrical Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.69	0.83	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	42	50	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	600	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=600V,V_{GS}=0V	--	--	1	μA
	Zero gate voltage drain current(Tj=125℃) ⑦	V_{DS}=600V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=10V, I_D=7A	--	230	280	mΩ
		(Tj=100℃) ⑦	--	416	--	mΩ
G_{FS}	Forward transconductance	V_{DS}=15V, I_D=7A	--	10	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=400V,V_{GS}=0V, f=100kHz	--	855	--	pF
Coss	Output capacitance ⑦		--	20	--	pF
Crss	Reverse transfer capacitance ⑦		--	1	--	pF
Co(er)	Output capacitance,energy related ⑦⑨	V_{DS}=0V to 400V V_{GS}=0V	--	31	--	pF
Co(tr)	Output capacitance,time related ⑦⑩		--	182	--	pF
Rg	Gate resistance	f=1MHz	--	4.4	--	Ω
Qg	Total gate charge ⑦	V_{DS}=400V,I_D=7A, V_{GS}=10V	--	19	--	nC
Qgs	Gate-source charge ⑦		--	3.8	--	nC
Qgd	Gate-drain charge ⑦		--	6.4	--	nC
Qoss	Output charge ⑦	V_{DS}=0V to 400V V_{GS}=0V	--	73	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay time	V_{DD}=400V, I_D=7A, R_G=300Ω, V_{GS}=10V, L=8mH	--	100	--	ns
Tr	Turn-on rise time		--	62	--	ns
Td(off)	Turn-off delay time		--	506	--	ns
Tf	Turn-off fall time		--	139	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=7A,V_{GS}=0V	--	0.83	1	V
Trr	Reverse recovery time ⑦	V_{DD}=50V, I_{sd}=7A, V_{GS}=0V di/dt=100A/μs	--	198	--	ns
Qrr	Reverse recovery charge⑦		--	1.9	--	uC

NOTE:

①Single pulse; pulse width ≤ 100μs.

②This maximum value is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 3.5A, V_{GS} =10V；100% FT tested at L = 10mH, I_{AS} = 3A.

③The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.

⑥These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦Guaranteed by design, not subject to production testing.

⑧Pulse width ≤ 380μs; duty cycle≤ 2%.

⑨ Equivalent capacitance to give same stored energy from 0V to 400V.

⑩ Equivalent capacitance to give same charging time from 0V to 400V.

Typical Characteristics

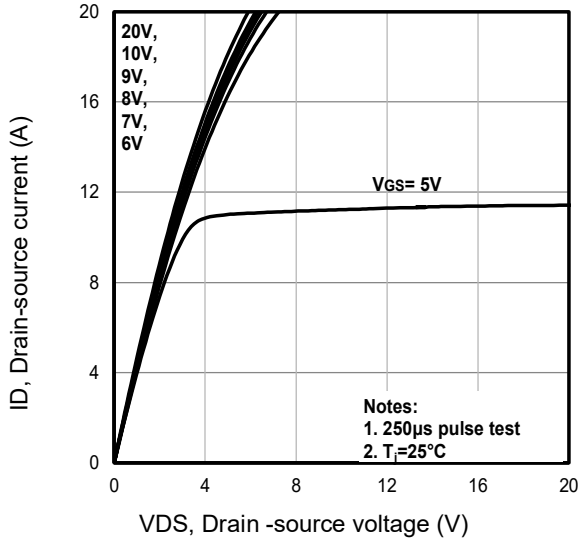


Fig1. Typical output characteristics

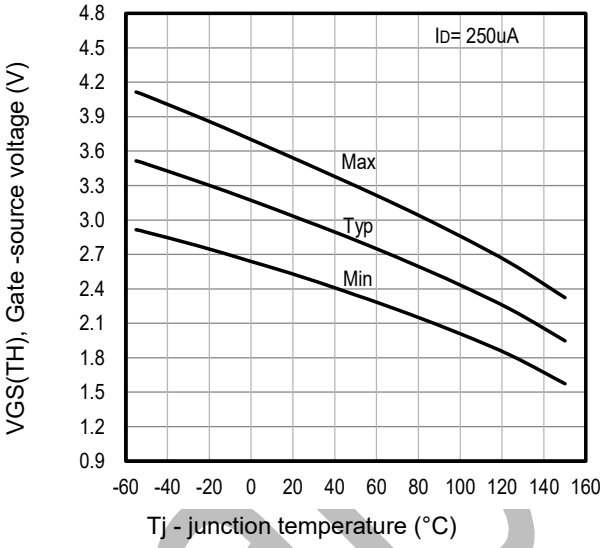


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

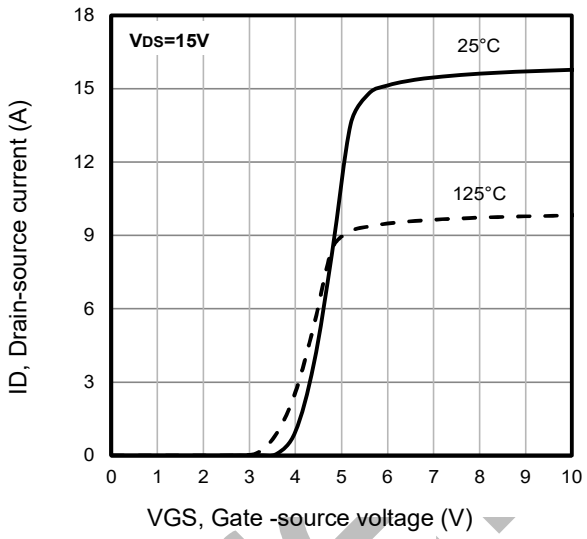


Fig3. Typical transfer characteristics

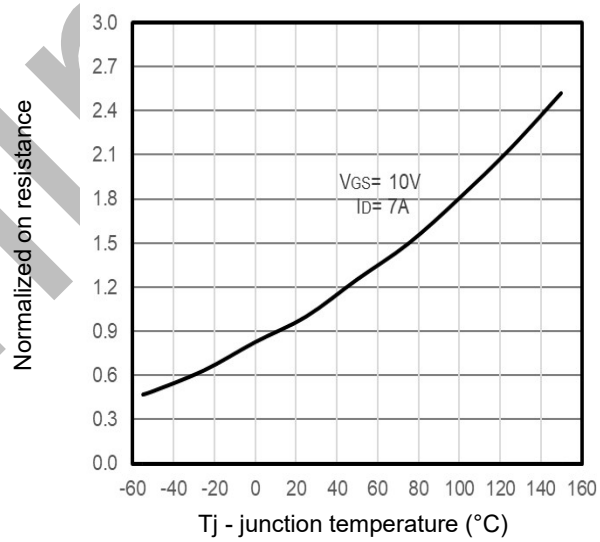


Fig4. Typical normalized on-resistance Vs. Tj

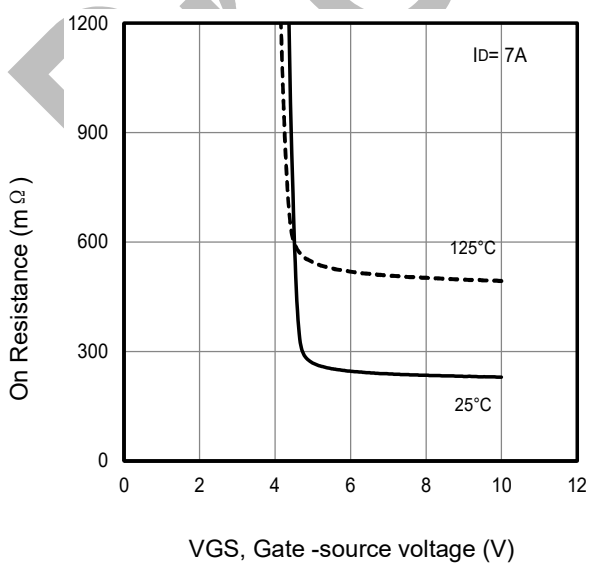


Fig5. Typical on resistance Vs gate -source voltage

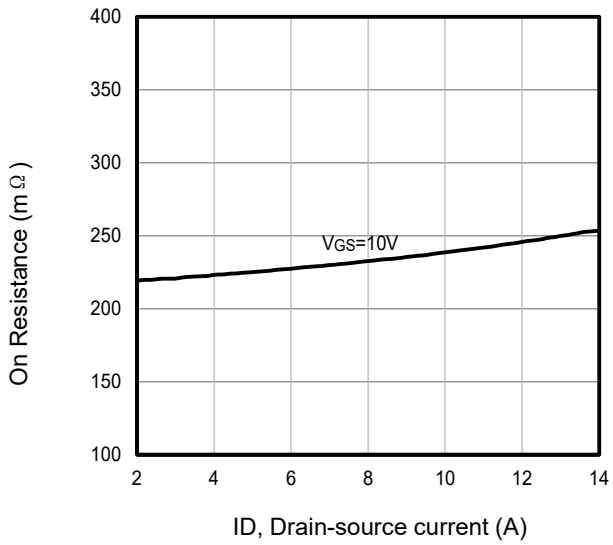


Fig6. Typical on resistance Vs drain current

Typical Characteristics

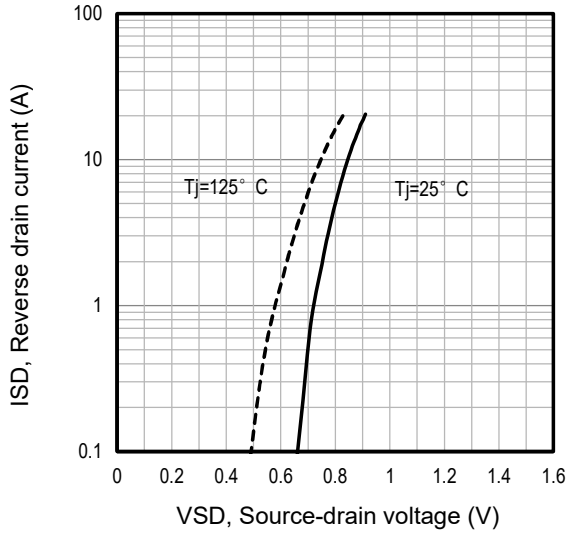


Fig7. Typical source-drain diode forward voltage

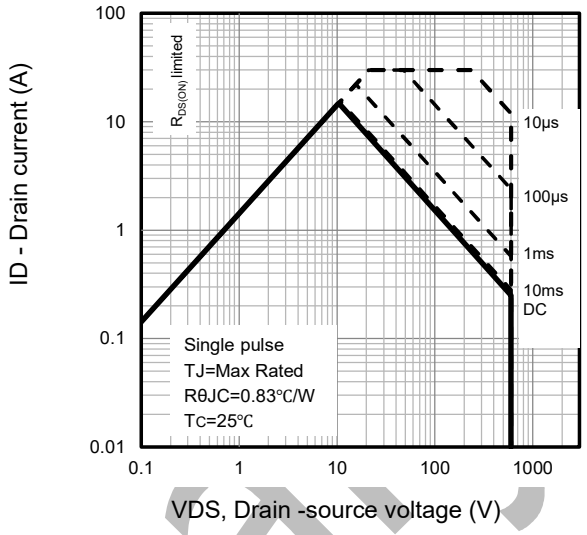


Fig8. Maximum safe operating area

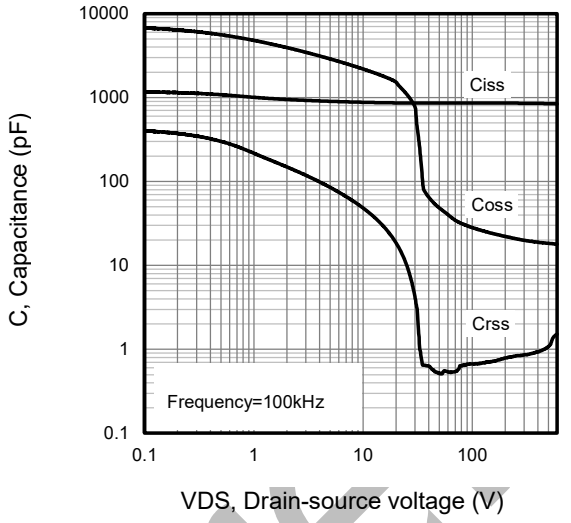


Fig9. Typical capacitance Vs. drain-source voltage

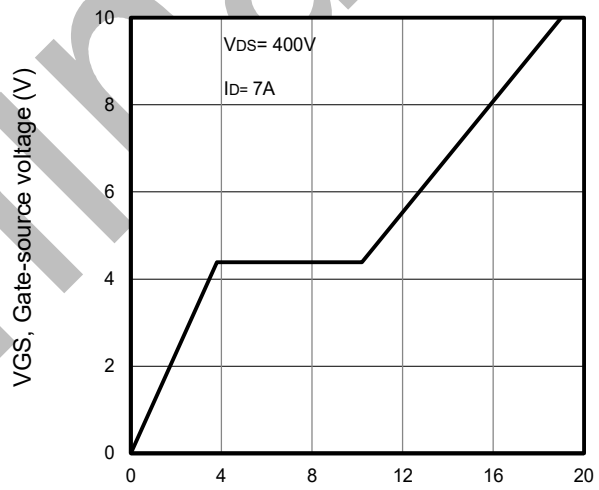


Fig10. Typical gate charge Vs. gate-source voltage

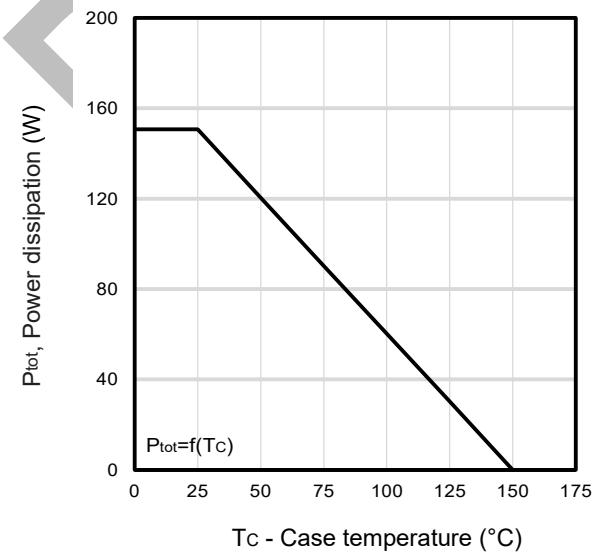


Fig11. Power dissipation Vs. case temperature

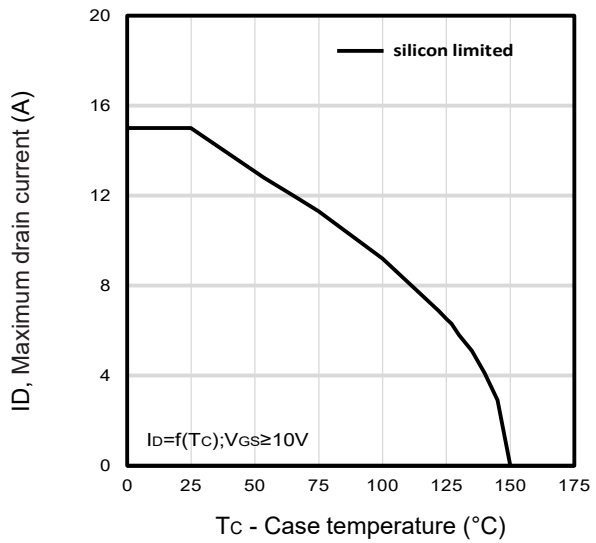


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

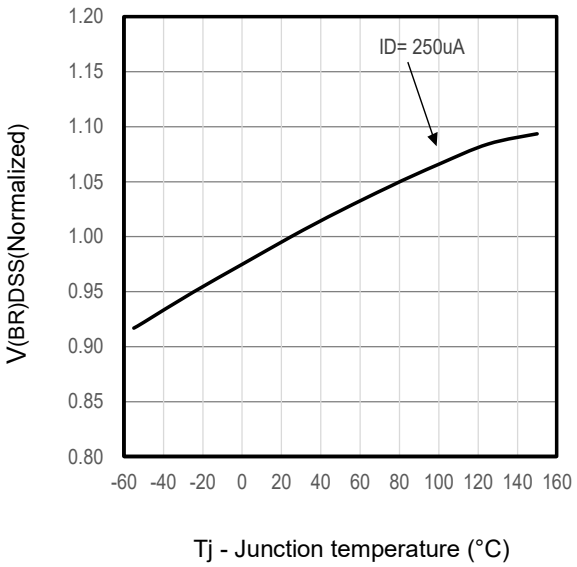


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

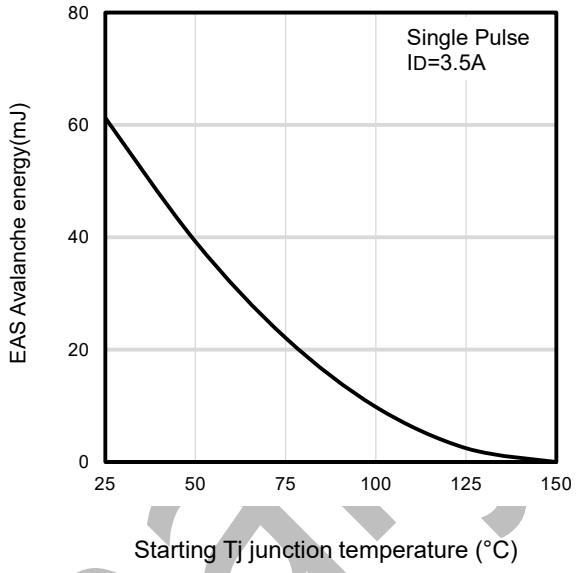


Fig14. Maximum avalanche energy vs temperature (°C)

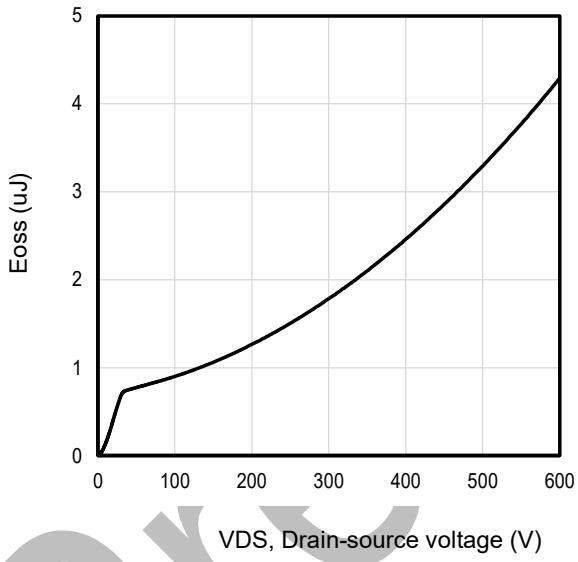


Fig15. Typical Coss stored energy

Typical Characteristics

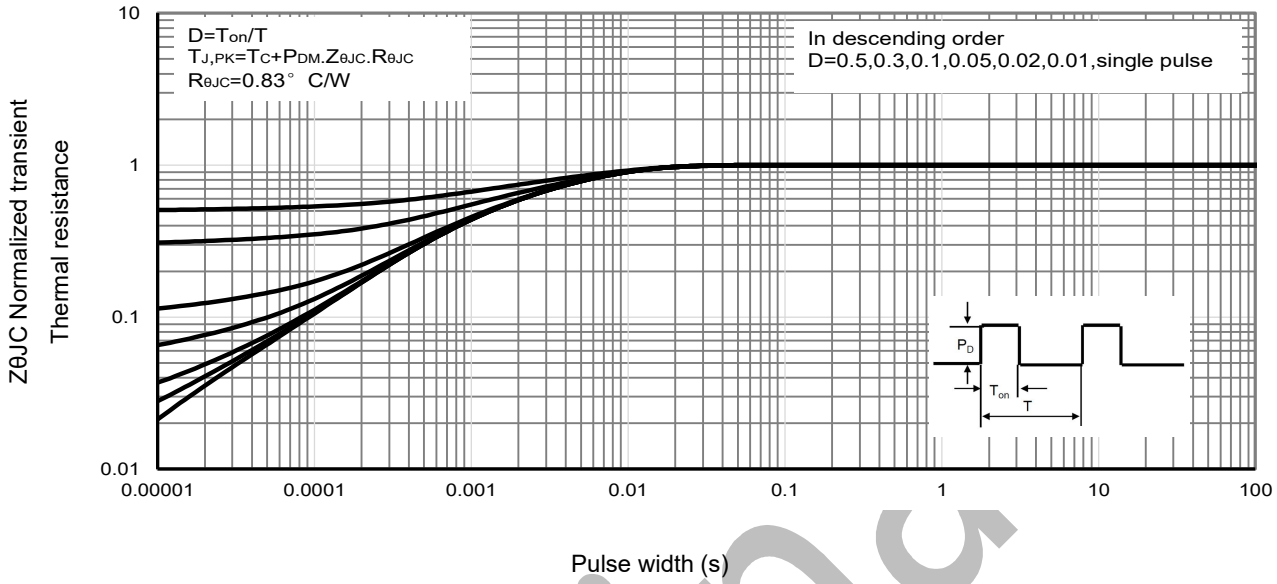


Fig16 . Normalized maximum transient thermal impedance

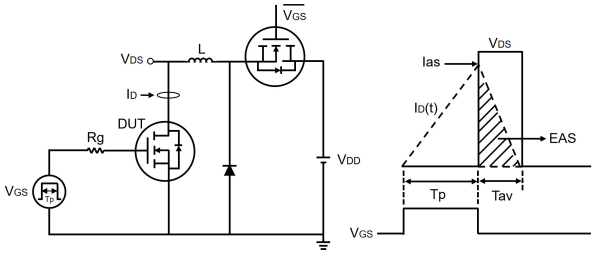


Fig17. Unclamped inductive test circuit and waveforms

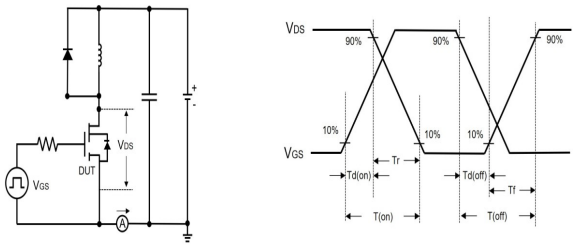
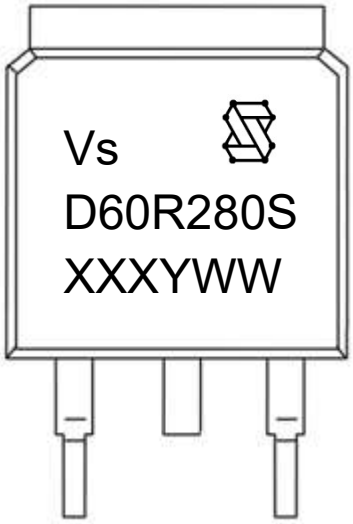


Fig18. Switching time test circuit and waveforms

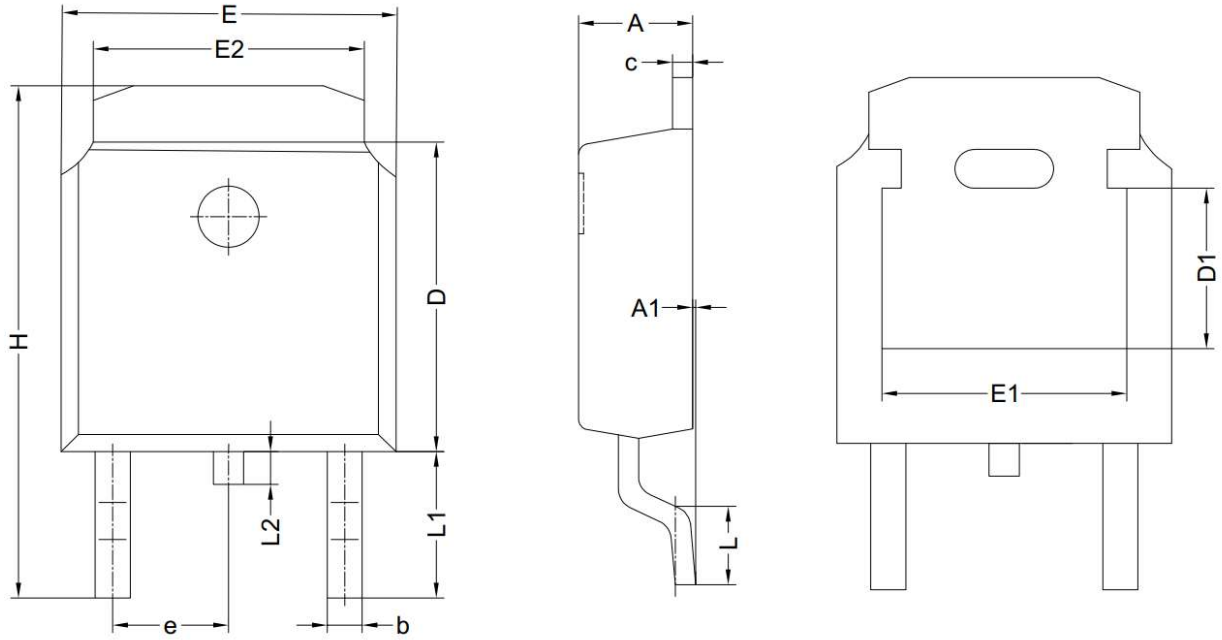
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（D60R280S）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.200	2.300	2.400
A1	--	--	0.127
b	0.640	0.690	0.740
c	0.460	0.520	0.580
D	6.000	6.100	6.200
D1	3.166 REF		
E	6.500	6.600	6.700
E1	4.826 REF		
E2	5.334 REF		
e	--	2.286	--
H	9.900	10.100	10.300
L	1.400	1.550	1.700
L1	2.888 REF		
L2	0.600	0.800	1.000