

Features

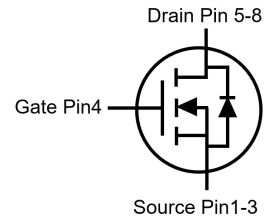
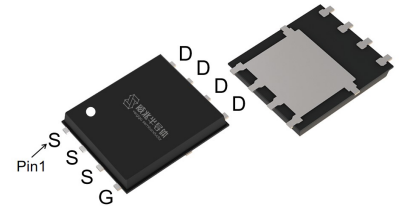
- Enhancement mode
- VitoMOS® II Technology
- 100% Avalanche tested, 100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses
- AEC-Q101 Compliant



Part ID	Package Type	Marking	Packing
VSP025N20HS-IG	PDFN5060X	025N20H	3000pcs/Reel

V_{DS}	200	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	25	mΩ
$I_D(\text{Silicon Limited})$	56	A

PDFN5060X



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		200	V
V_{GS}	Gate-source voltage		± 25	V
I_S	Diode continuous forward current (Silicon limited)	$T_C = 25^\circ\text{C}$	56	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$	56	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	35	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	170	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	6.3	A
		$T_A = 70^\circ\text{C}$	5.1	A
E_{AS}	Avalanche energy, single pulsed ②		256	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	205	W
		$T_C = 100^\circ\text{C}$	82	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	2.6	W
		$T_A = 70^\circ\text{C}$	1.7	W
T_J, T_{STG}	Operating junction and storage temperature range		-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.51	0.61	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	40	48	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _J =25°C (unless otherwise stated)						
V(BR)DSS	Drain-source breakdown voltage	V _{GS} =0V, I _D =250uA	200	--	--	V
I _{DSS}	Zero gate voltage drain current(T _J =25°C)	V _{DS} =200V,V _{GS} =0V	--	--	1	μA
	Zero gate voltage drain current(T _J =125°C)⑦	V _{DS} =200V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-body leakage current	V _{GS} =±25V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} ,I _D =250μA	2.5	3	3.5	V
R _{DS(on)}	Drain-source on-state resistance ⑧	V _{GS} =10V, I _D =40A	--	25	31	mΩ
		(T _J =100°C)⑦	--	39	--	mΩ
G _{FS}	Forward transconductance	V _{DS} =5V, I _D =40A	--	45	--	S
Dynamic Electrical Characteristics @ T _J = 25°C (unless otherwise stated)						
C _{iss}	Input capacitance ⑦	V _{DS} =100V,V _{GS} =0V, f=100kHz	--	1765	--	pF
C _{oss}	Output capacitance ⑦		--	190	--	pF
C _{rss}	Reverse transfer capacitance ⑦		--	20	--	pF
R _g	Gate resistance	f=1MHz	--	3.6	--	Ω
Q _g	Total gate charge ⑦	V _{DS} =100V,I _D =40A, V _{GS} =10V	--	26	--	nC
Q _{gs}	Gate-source charge ⑦		--	9.5	--	nC
Q _{gd}	Gate-drain charge ⑦		--	5.7	--	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on delay time	V _{DD} =100V, I _D =40A, R _G =3.9Ω, V _{GS} =10V	--	11	--	ns
T _r	Turn-on rise time		--	28	--	ns
T _{d(off)}	Turn-off delay time		--	24	--	ns
T _f	Turn-off fall time		--	23	--	ns
Source- Drain Diode Characteristics@ T _J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A,V _{GS} =0V	--	0.88	1	V
T _{rr}	Reverse recovery time ⑦	V _{DD} =100V, I _{sd} =40A, V _{GS} =0V	--	116	--	ns
Q _{rr}	Reverse recovery charge ⑦	di/dt=100A/μs	--	461	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 32A, V_{GS} = 10V; 100% FT tested at L = 0.1mH, I_{AS} = 47A.
- ③ The power dissipation P_d is based on T_J(max), using junction-to-case thermal resistance RθJC.
- ④ The power dissipation P_{dsm} is based on T_J(max), using junction-to-ambient thermal resistance RθJA.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles 2%.

Typical Characteristics

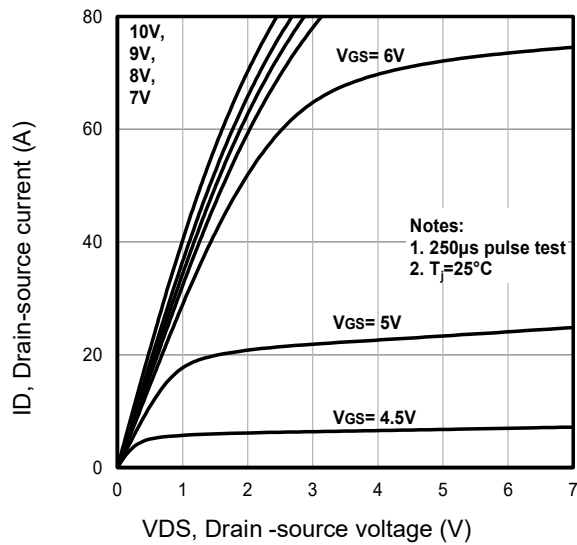


Fig1. Typical output characteristics

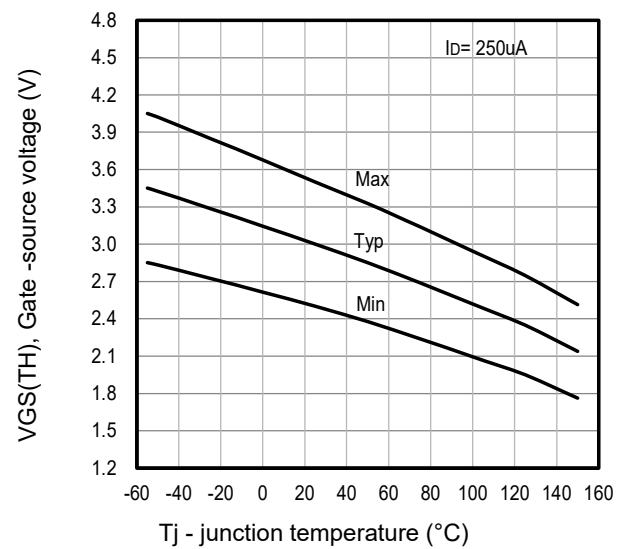


Fig2. Typical $V_{GS(TH)}$ gate-source voltage Vs. T_j

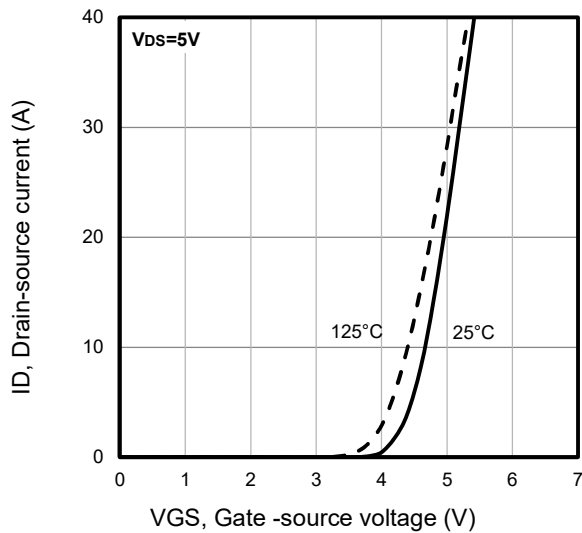


Fig3. Typical transfer characteristics

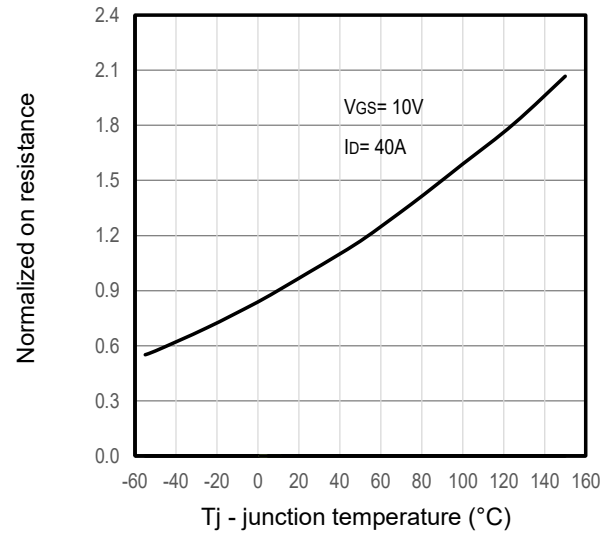


Fig4. Typical normalized on-resistance Vs. T_j

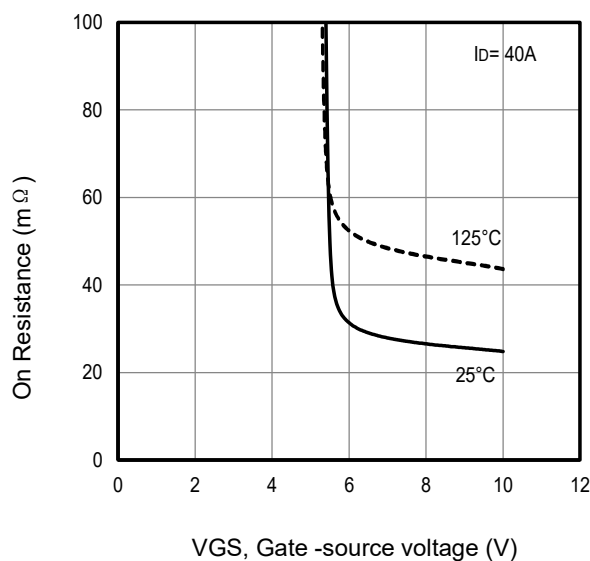


Fig5. Typical on resistance Vs gate-source voltage

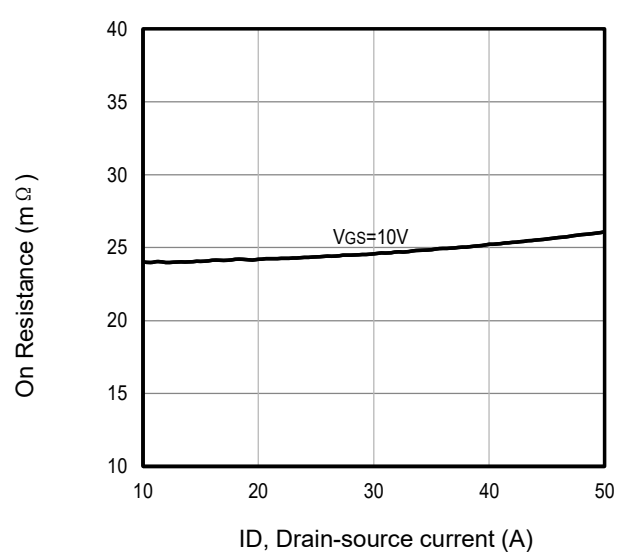


Fig6. Typical on resistance Vs drain current

Typical Characteristics

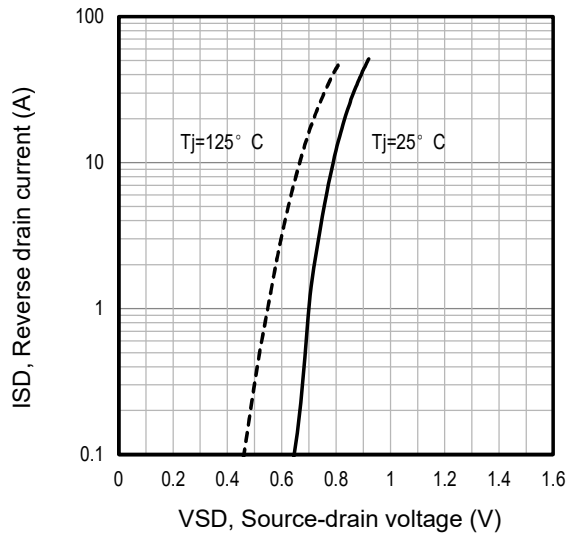


Fig7. Typical source-drain diode forward voltage

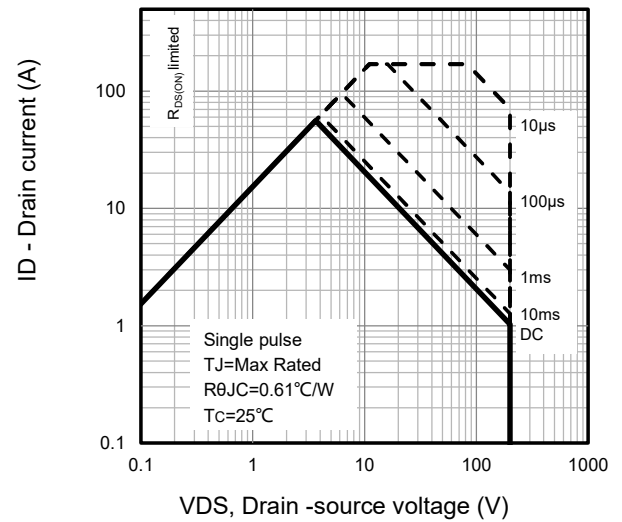


Fig8. Maximum safe operating area

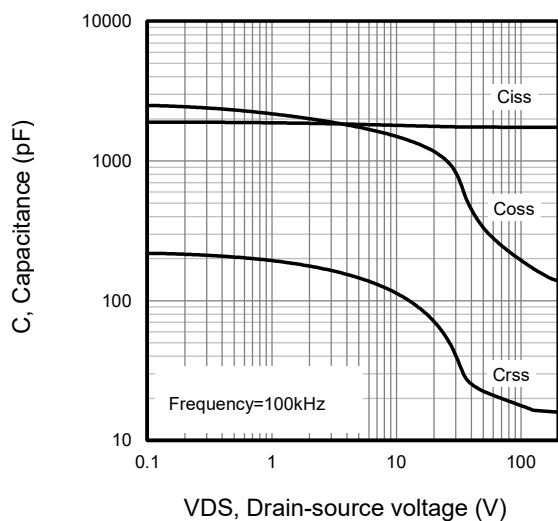


Fig9. Typical capacitance Vs. drain-source voltage

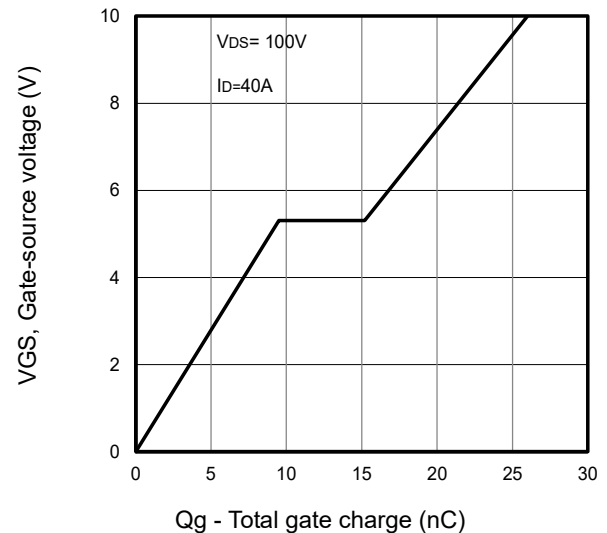


Fig10. Typical gate charge Vs. gate-source voltage

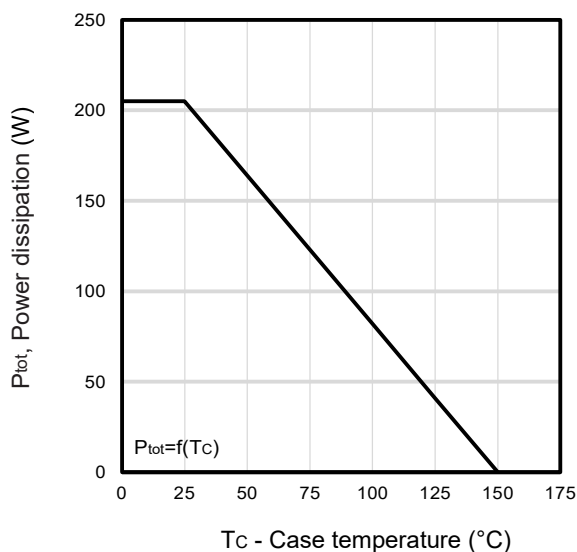


Fig11. Power dissipation Vs. case temperature

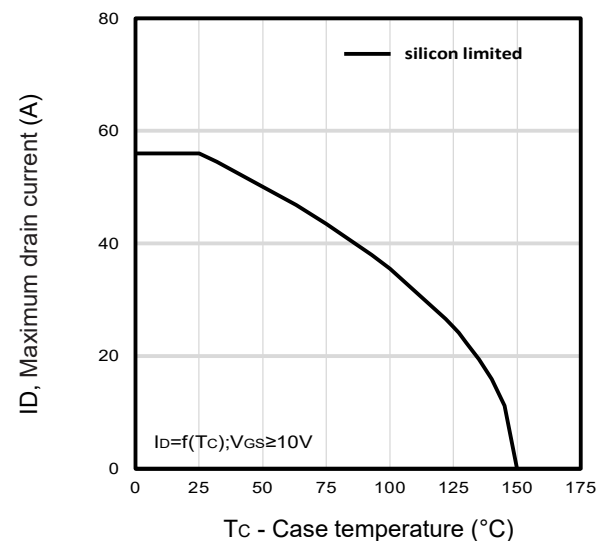
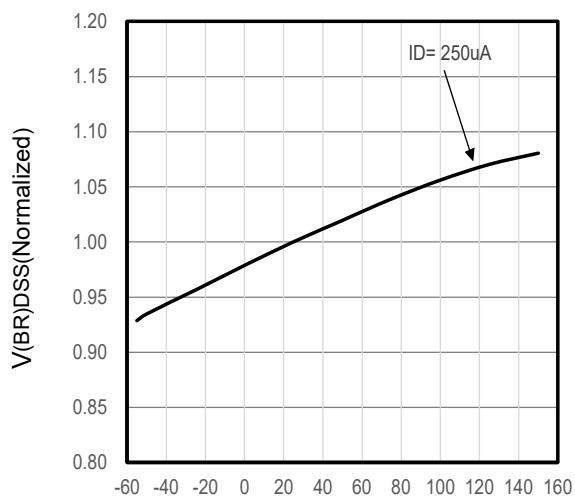


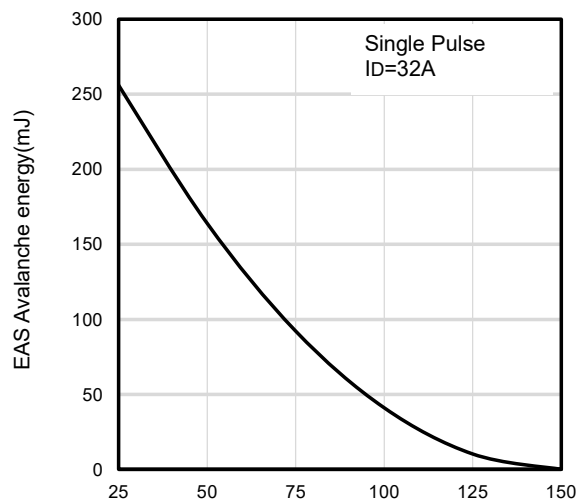
Fig12. Maximum drain current Vs. case temperature

Typical Characteristics



Tj - Junction temperature (°C)

Fig13. Typical V(BR)DSS Vs Tj



Starting Tj junction temperature (°C)

Fig14. Maximum avalanche energy vs temperature (°C)

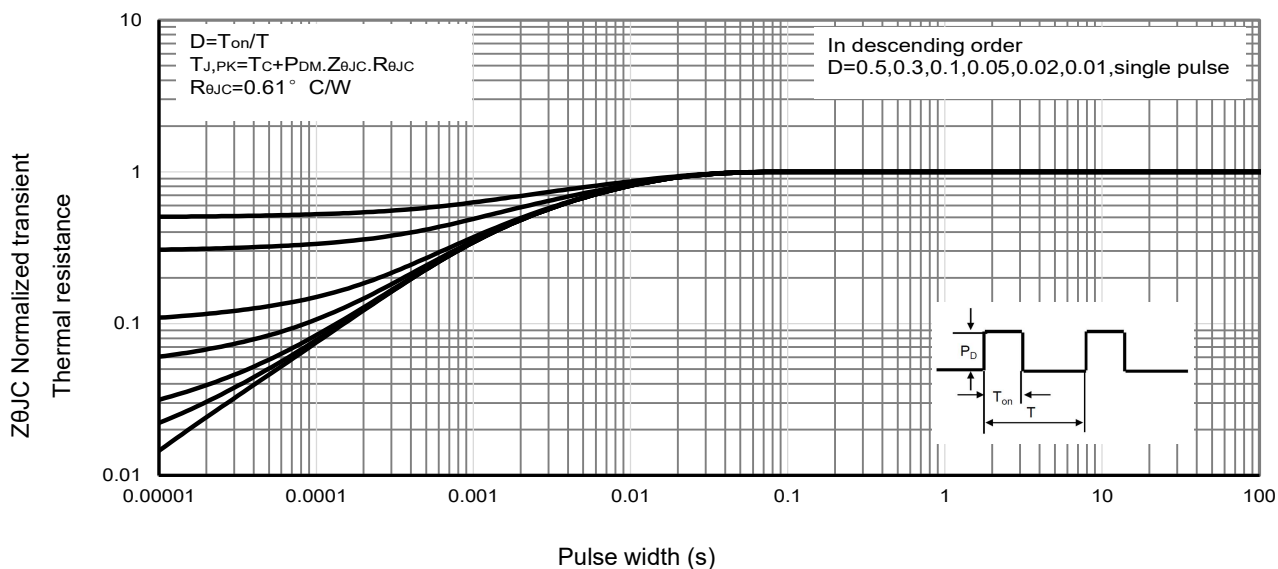


Fig15. Normalized maximum transient thermal impedance

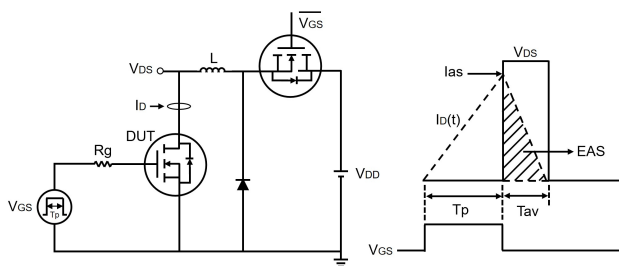


Fig16. Unclamped inductive test circuit and waveforms

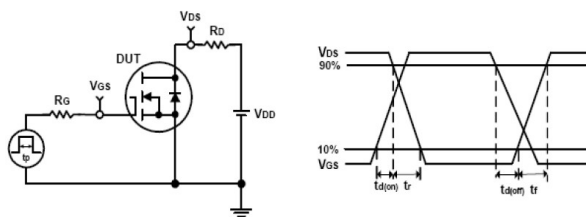
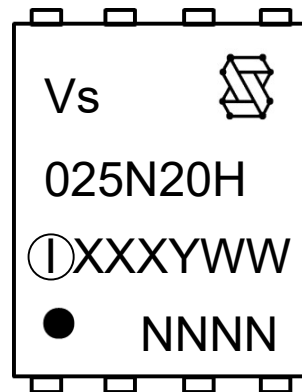


Fig17. Switching time test circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (025N20H)

3rd line: Date code (①XXXYWW)

①: Fixed printing

XXX: Wafer Lot Number Code, code changed with Lot Number

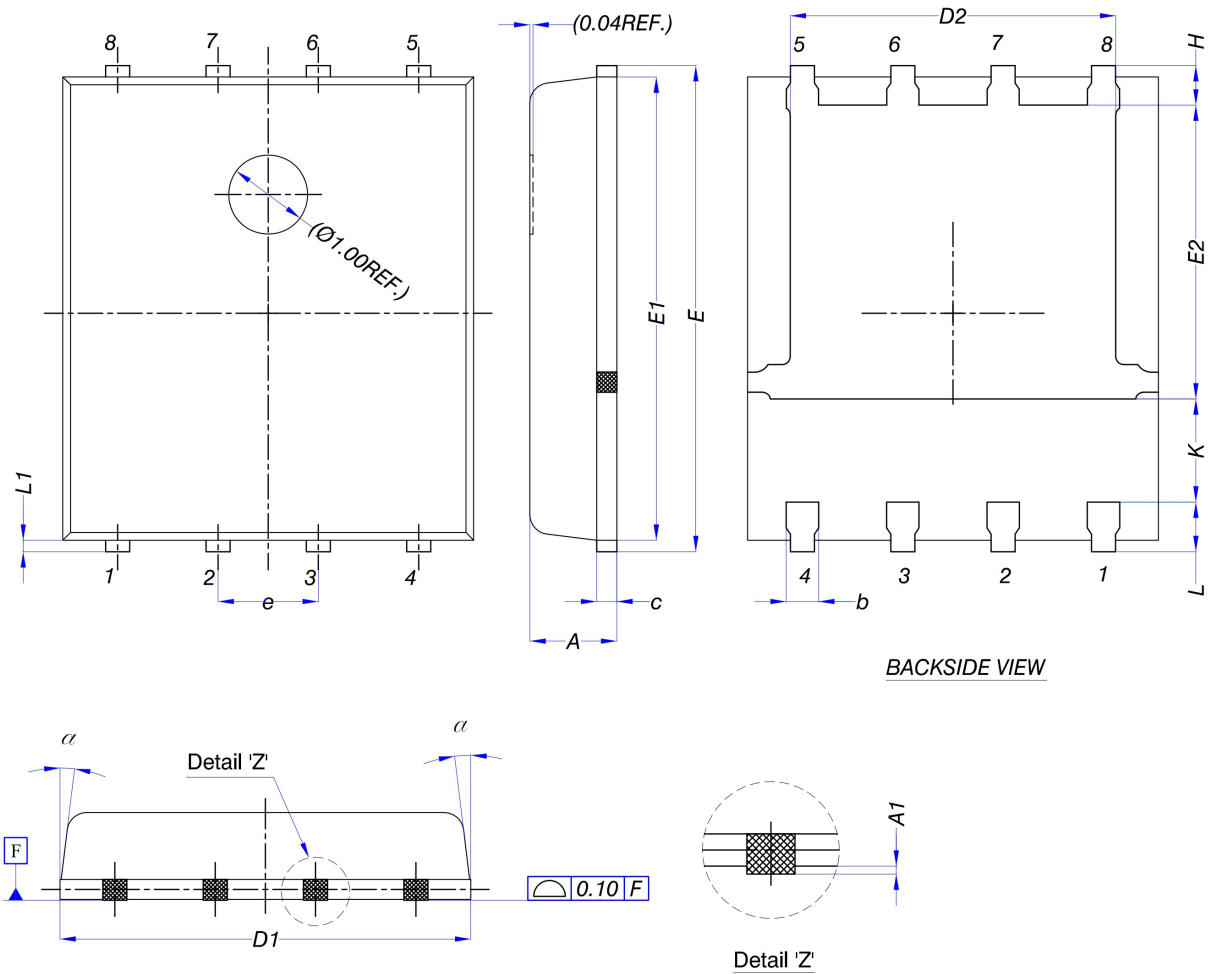
Y: Year Code, refer to table below

WW: Week Code (01 to 53)

NNNN: Assembly lot No.

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5060X Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	1.00	1.10	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.50
c	0.20	0.25	0.30
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
E	5.95	6.15	6.35
E1	5.66	5.86	6.06
E2	3.52	3.72	3.92
e	1.27 BSC		
H	0.40	0.50	0.60
K	1.10	--	--
L	0.50	0.60	0.70
L1	0.08	0.15	0.22
α	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.