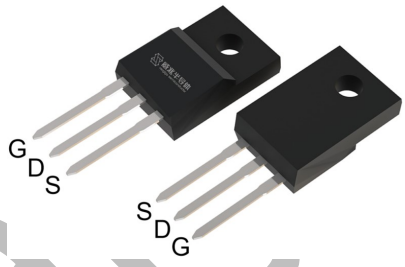
Features

- Enhancement mode
- Super junction technology
- 100% Avalanche Tested, 100% Rg Tested

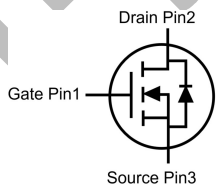
V_{DS}	600	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	220	mΩ
$I_{D(Silicon\ limited)}$	12	A

TO-220F



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VSF60R280S	TO-220F	F60R280S	50pcs/Tube



Preliminary

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		600	V
V_{GS}	Gate-source voltage		±30	V
I_S	Diode continuous forward current (Silicon limited)①	T_C = 25°C	12	A
I_D	Continuous drain current @VGS=10V (Silicon limited)①	T_C = 25°C	12	A
I_D	Continuous drain current @VGS=10V (Silicon limited)①	T_C = 100°C	7.7	A
I_{DM}	Pulse drain current tested ②	T_C = 25°C	34	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	1.9	A
		T_A=70°C	1.5	A
EAS	Maximum Avalanche energy, single pulsed ③		31	mJ
P_D	Maximum power dissipation ④	T_C = 25°C	66	W
		T_C = 100°C	26	W
P_{DSM}	Maximum power dissipation ⑤	T_A = 25°C	2.5	W
		T_A = 70°C	1.6	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑥	1.6	1.9	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑦	42	50	°C/W

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Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	600	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=600V,V_{GS}=0V	--	--	1	μA
	Zero gate voltage drain current(Tj=125℃) ⑧	V_{DS}=600V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-source on-state resistance ⑨	V_{GS}=10V, I_D=7A	--	220	280	mΩ
		(Tj=100℃) ⑧	--	400	--	mΩ
G_{FS}	Forward transconductance	V_{DS}=15V, I_D=7A	--	12	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑧	V_{DS}=400V,V_{GS}=0V, f=100kHz	--	850	--	pF
Coss	Output capacitance ⑧		--	20	--	pF
Crss	Reverse transfer capacitance ⑧		--	1	--	pF
Co(er)	Output capacitance,energy related ⑧⑩	V_{DS}=0V to 400V V_{GS}=0V	--	32	--	pF
Co(tr)	Output capacitance,time related ⑧⑪		--	181	--	pF
Rg	Gate resistance	f=1MHz	--	4.1	--	Ω
Qg	Total gate charge ⑧	V_{DS}=400V,I_D=7A, V_{GS}=10V	--	19	--	nC
Qgs	Gate-source charge ⑧		--	3.8	--	nC
Qgd	Gate-drain charge ⑧		--	6.7	--	nC
Qoss	Output charge ⑧	V_{DS}=0V to 400V V_{GS}=0V	--	72	--	nC
Switching Characteristics ⑧						
Td(on)	Turn-on delay time	V_{DD}=400V, I_D=7A, R_G=300Ω, V_{GS}=10V, L=8mH	--	100	--	ns
Tr	Turn-on rise time		--	62	--	ns
Td(off)	Turn-off delay time		--	506	--	ns
Tf	Turn-off fall time		--	139	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=7A,V_{GS}=0V	--	0.84	1	V
Trr	Reverse recovery time ⑧	V_{DD}=50V, I_{sd}=7A, V_{GS}=0V di/dt=100A/μs	--	198	--	ns
Qrr	Reverse recovery charge ⑧		--	1.91	--	uC

NOTE: ① Drain current limited only by maximum junction temperature; TO-220AB equivalent.

② Single pulse; pulse width limited by Tj(max).

③ This maximum value is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 2.5A, V_{GS} =10V；100% FT tested at L = 10mH, I_{AS} = 2A.

④ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

⑤ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑥ Thermal resistance from junction to case, this test is performed on a cold plate.

⑦ The value of RθJA is measured with the device in a still air environment with TA =25° C.

⑧ Guaranteed by design, not subject to production testing.

⑨ Pulse width ≤ 380μs; duty cycle≤ 2%.

⑩ Equivalent capacitance to give same stored energy from 0V to 400V.

⑪ Equivalent capacitance to give same charging time from 0V to 400V.

Preliminary

Typical Characteristics

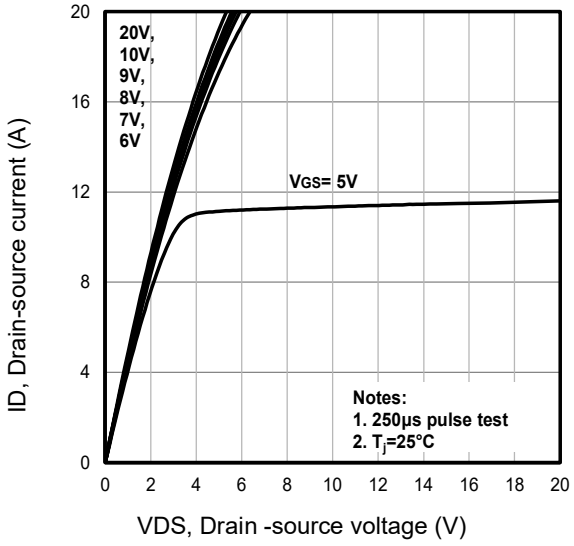

Fig1. Typical output characteristics

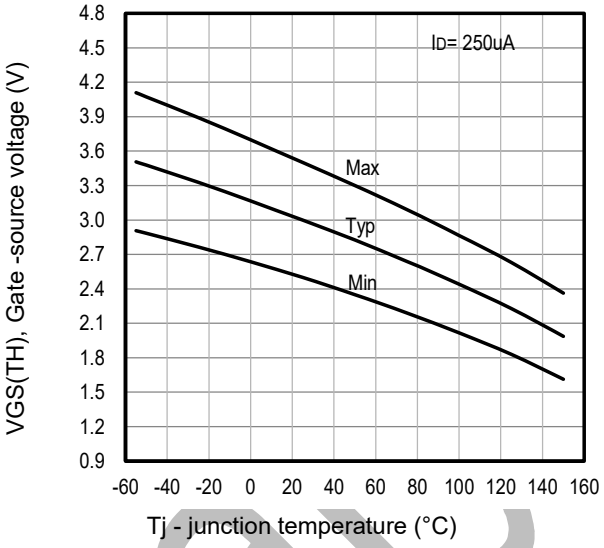

Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

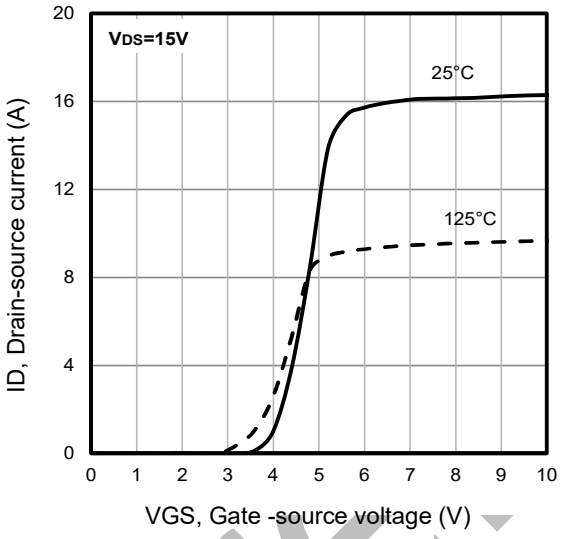

Fig3. Typical transfer characteristics

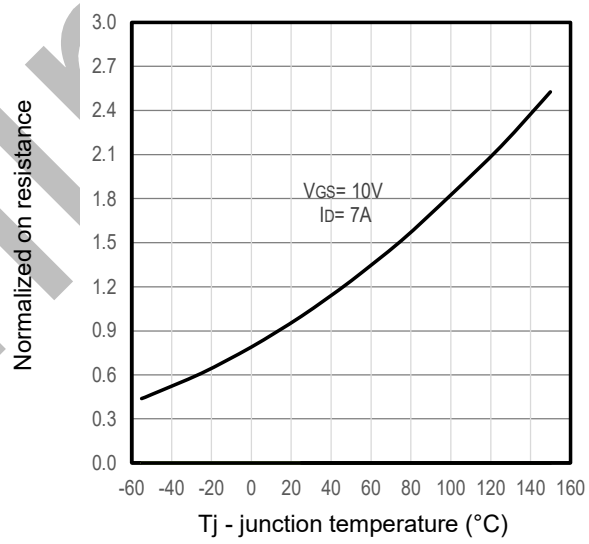

Fig4. Typical normalized on-resistance Vs. Tj

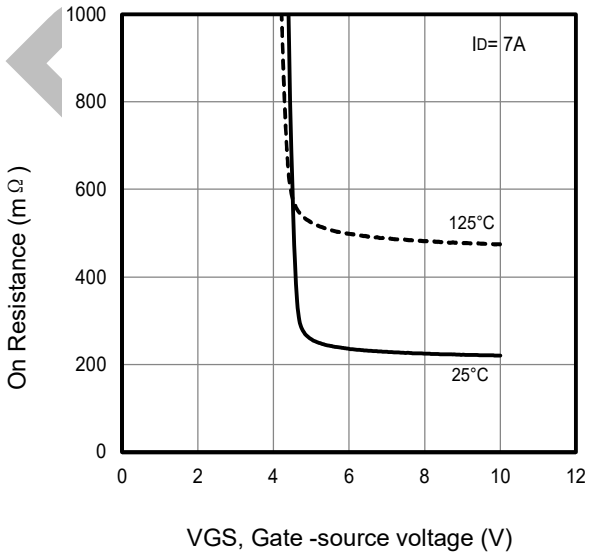

Fig5. Typical on resistance Vs gate -source voltage

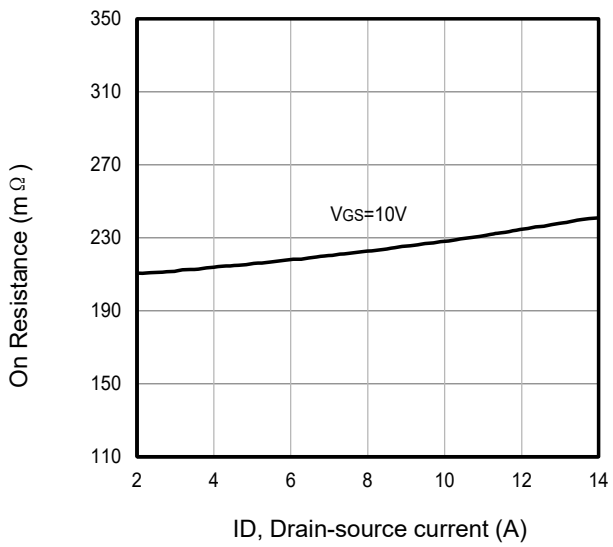

Fig6. Typical on resistance Vs drain current

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Typical Characteristics

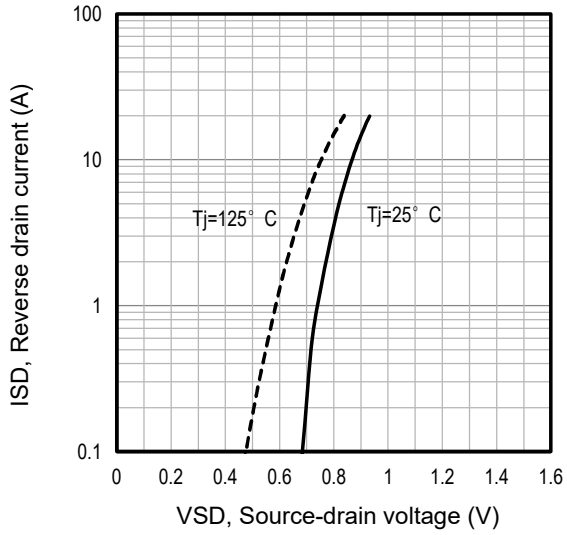


Fig7. Typical source-drain diode forward voltage

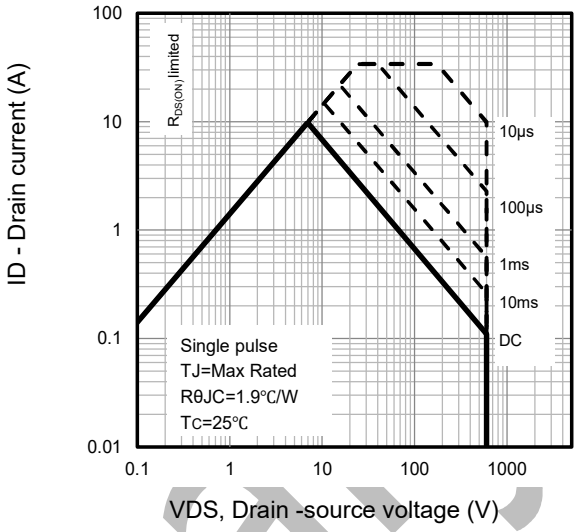


Fig8. Maximum safe operating area

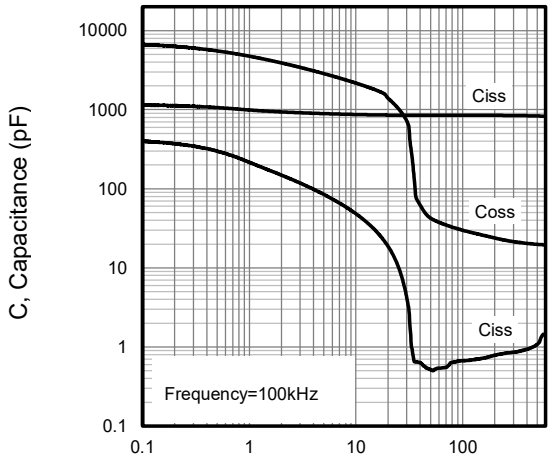


Fig9. Typical capacitance Vs. drain-source voltage

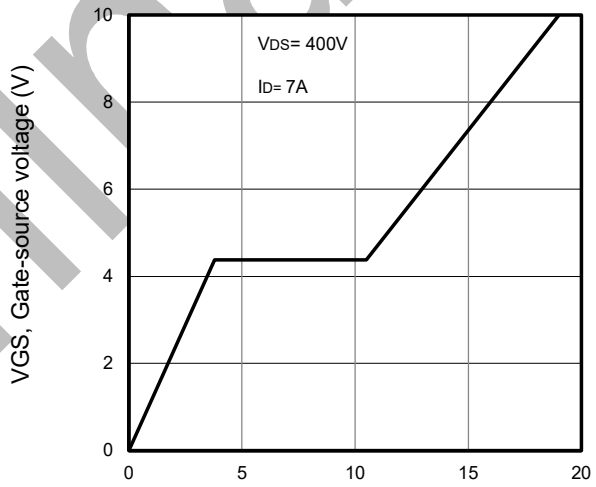


Fig10. Typical gate charge Vs. gate-source voltage

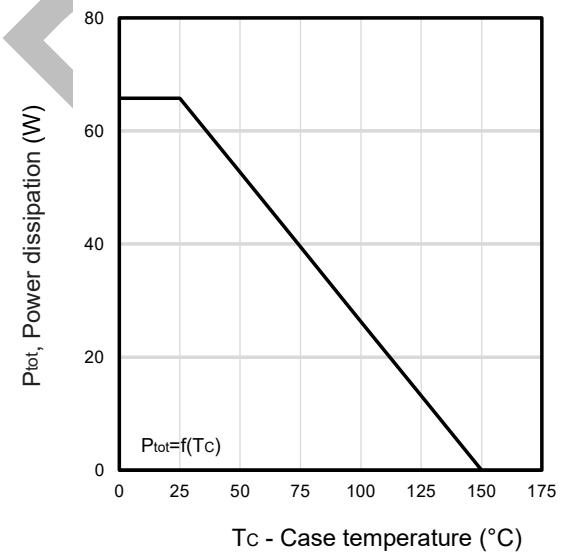


Fig11. Power dissipation Vs. case temperature

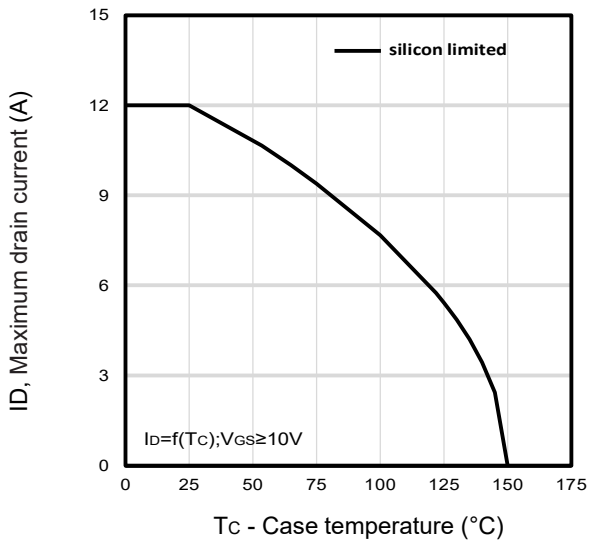


Fig12. Maximum drain current Vs. case temperature

Preliminary

Typical Characteristics

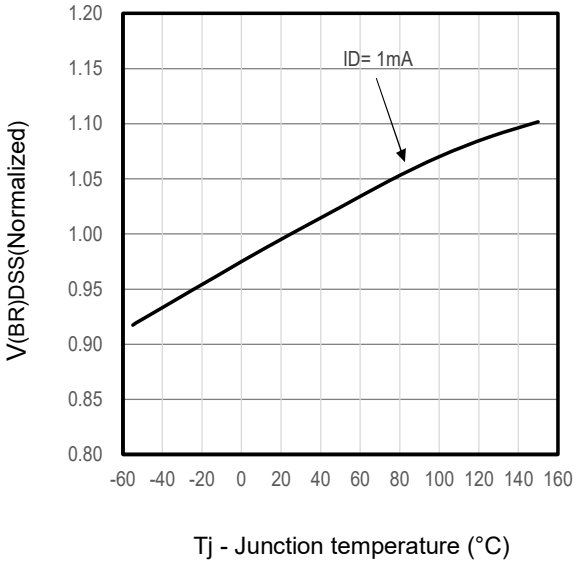


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

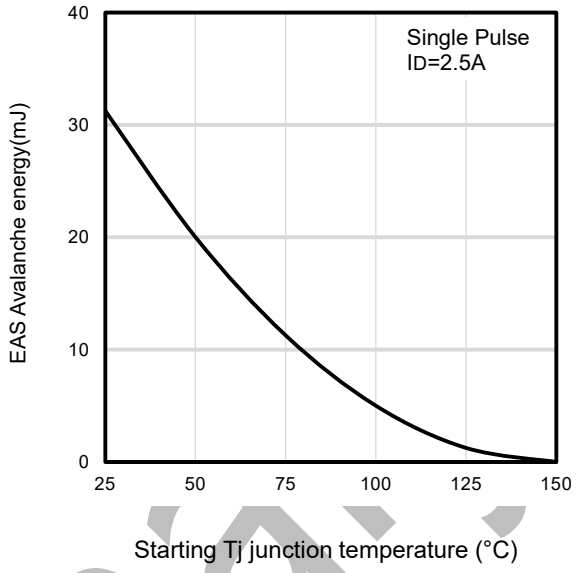


Fig14. Maximum avalanche energy vs temperature (°C)

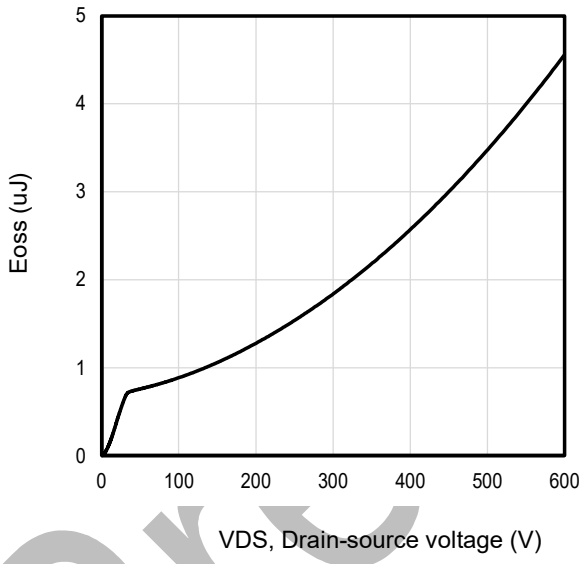


Fig15. Typical Coss stored energy

Preliminary

Typical Characteristics

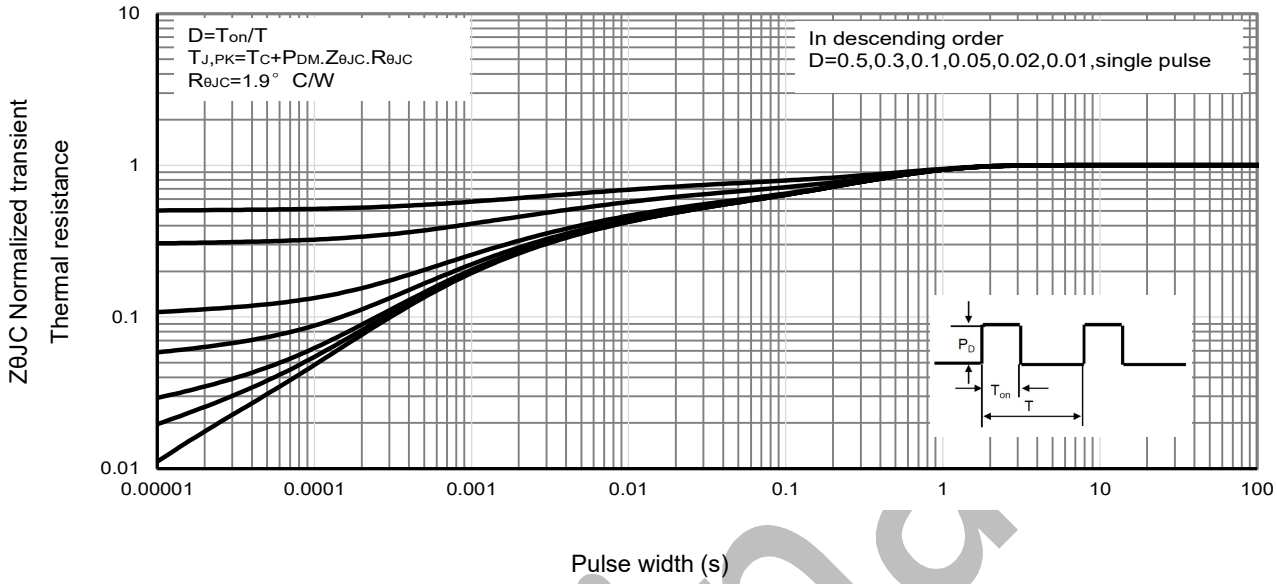


Fig16 . Normalized maximum transient thermal impedance

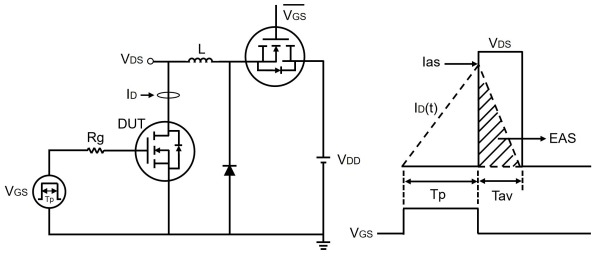


Fig17. Unclamped inductive test circuit and waveforms

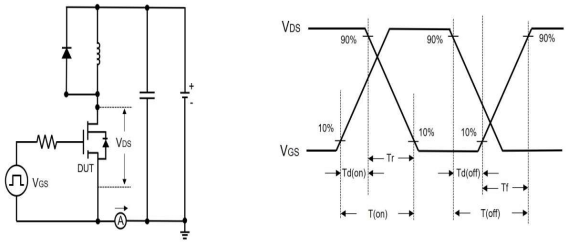
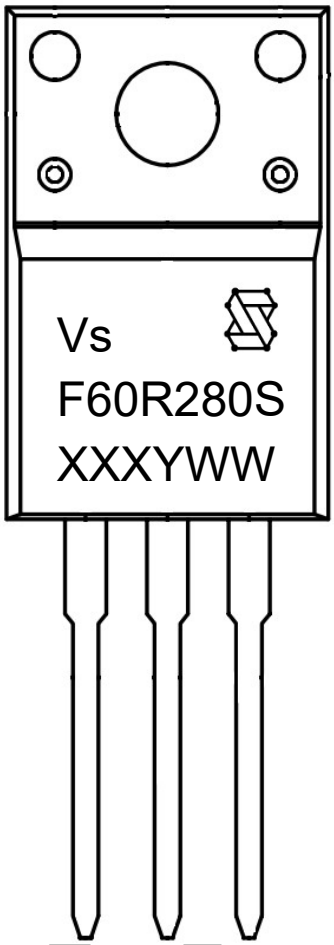


Fig18. Switching time test circuit and waveforms

Preliminary

Marking Information



1st line: Vergiga Code（Vs）, Vergiga Logo
2nd line: Part Number（F60R280S）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

Preliminary

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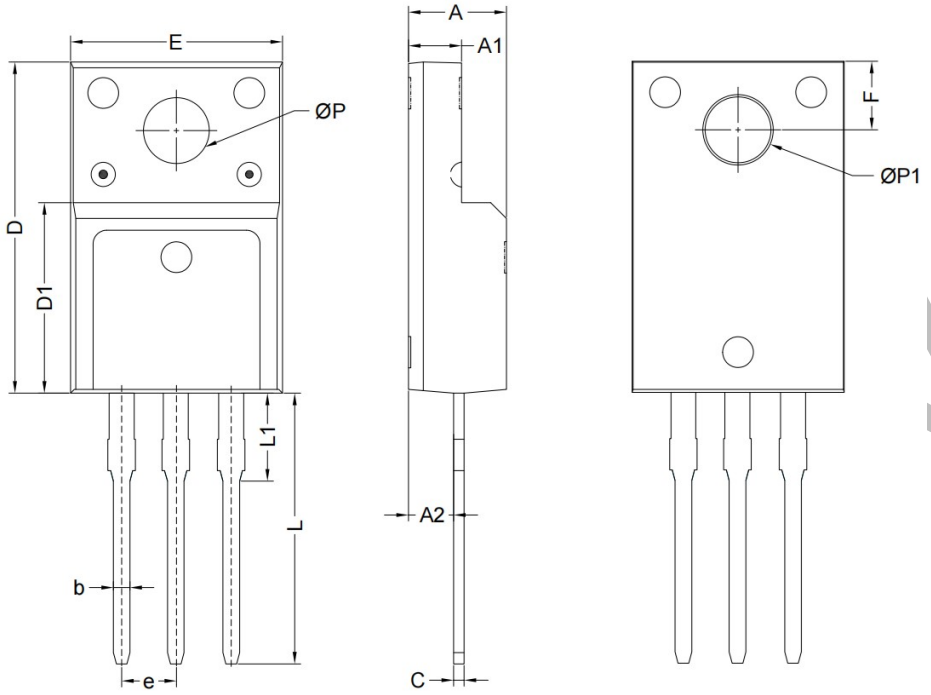
TO-220F Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	2.66	2.76	2.86
b	0.75	0.80	0.85
C	0.45	0.50	0.55
D	15.67	15.87	16.07
D1	9.04	9.12	9.20
e	2.50	2.54	2.58
E	10.00	10.16	10.30
F	3.20	3.30	3.40
L	12.78	12.98	13.18
L1	3.13	3.23	3.33
ΦP	3.08	3.18	3.28
ΦP1	3.30	3.40	3.50

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