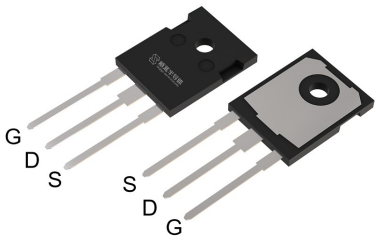
Features

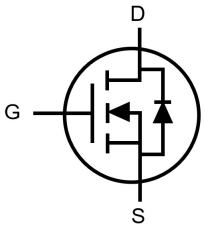
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=10 V
- Super Junction Technology
- 100% Avalanche test,100% Rg Tested

V_{DS}	650	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	63	mΩ
$I_{D(Silicon\ Limited)}$	48	A

TO-247



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSU070N65HS3	TO-247	070N65H	30pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		650	V
V_{GS}	Gate-Source voltage		±30	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	48	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	48	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	31	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	123	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	4.4	A
		T_A = 70°C	3.5	A
EAS	Avalanche energy, single pulsed ②		1620	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	391	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	3.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.27	0.32	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	32	38	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=600V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)⑦	V_{DS}=520V,V_{GS}=0V	--	--	50	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±30V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.5	3.5	4.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=20A	--	63	70	mΩ
		T_j=100℃ ⑦	--	108	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=400V,V_{GS}=0V, f=250kHz	--	3115	--	pF
Coss	Output Capacitance ⑦		--	80	--	pF
Crss	Reverse Transfer Capacitance ⑦		--	3	--	pF
Rg	Gate Resistance	f=1MHz	--	0.8	--	Ω
Qg	Total Gate Charge ⑦	V_{DS}=400V,I_D=20A, V_{GS}=10V	--	78	--	nC
Qgs	Gate-Source Charge ⑦		--	16	--	nC
Qgd	Gate-Drain Charge ⑦		--	32	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=400V, I_D=20A, R_G=10Ω, V_{GS}=10V	--	22	--	ns
Tr	Turn-on Rise Time		--	28	--	ns
Td(off)	Turn-Off Delay Time		--	108	--	ns
Tf	Turn-Off Fall Time		--	33	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.84	1	V
Trr	Reverse Recovery Time ⑦	V_{DD}=100V I_{sd}=20A, V_{GS}=0V di/dt=100A/μs	--	381	--	ns
Qrr	Reverse Recovery Charge ⑦		--	7.6	--	uC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This value is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} =10V； 100% FT tested at L = 10mH, I_{AS} = 9A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad).

⑥ The value of RθJA is measured with the device in a still air environment with TA =25° C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

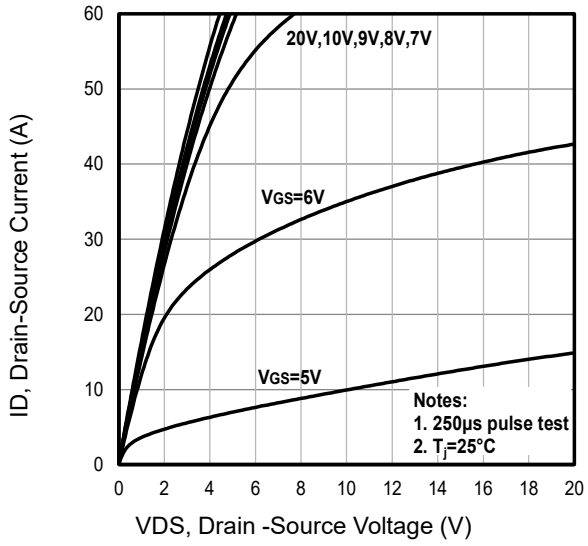


Fig1. Typical Output Characteristics

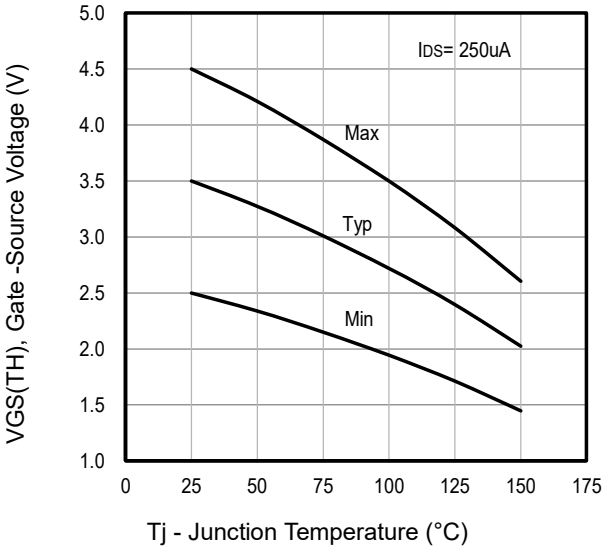


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

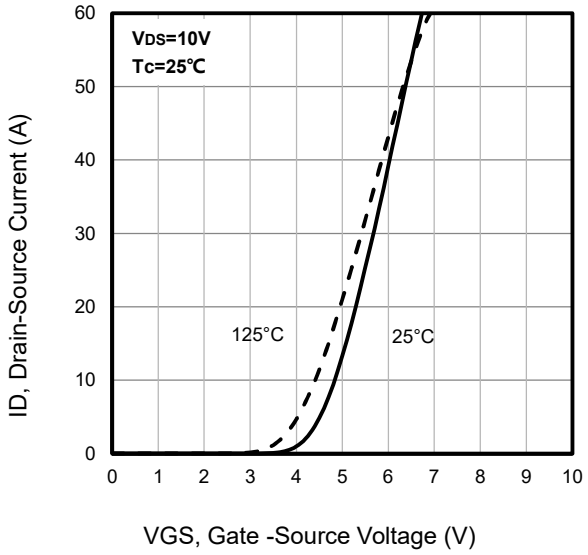


Fig3. Typical Transfer Characteristics

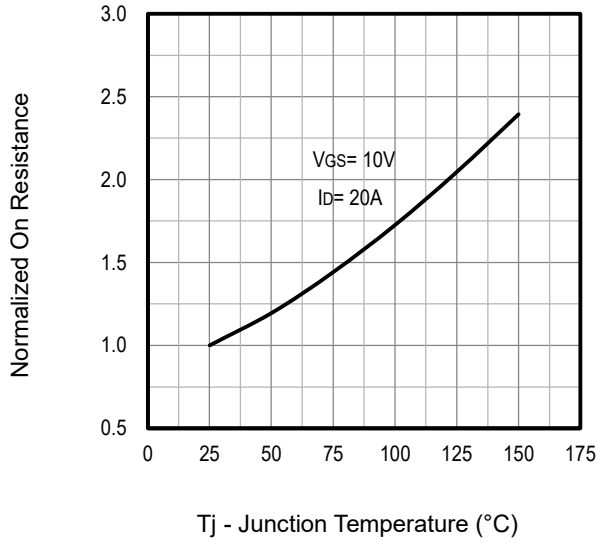


Fig4. Typical Normalized On-Resistance Vs. Tj

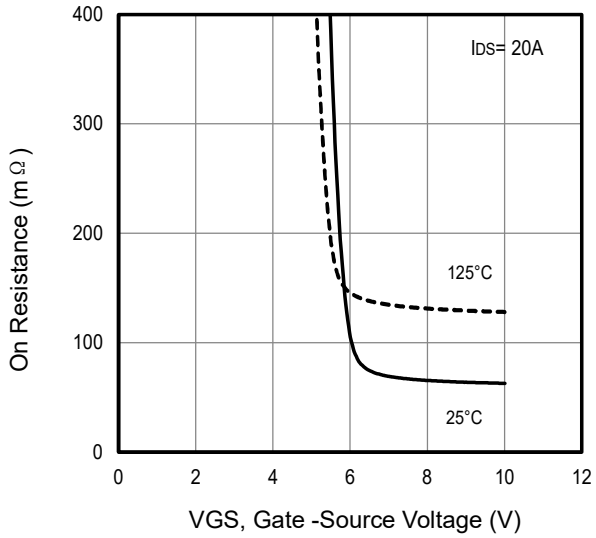


Fig5. Typical On Resistance Vs Gate -Source Voltage

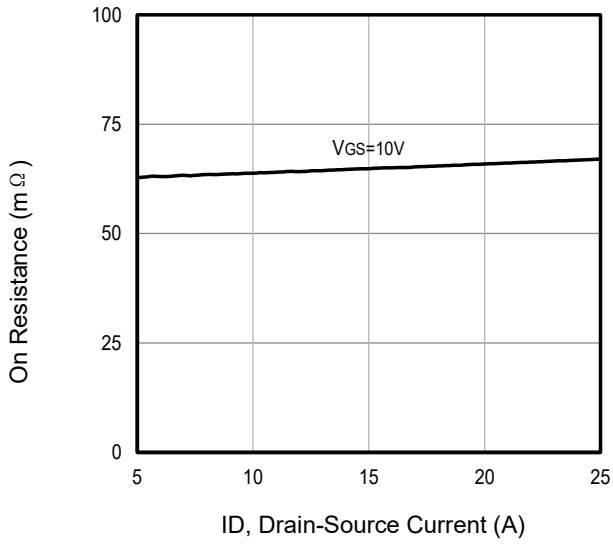


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

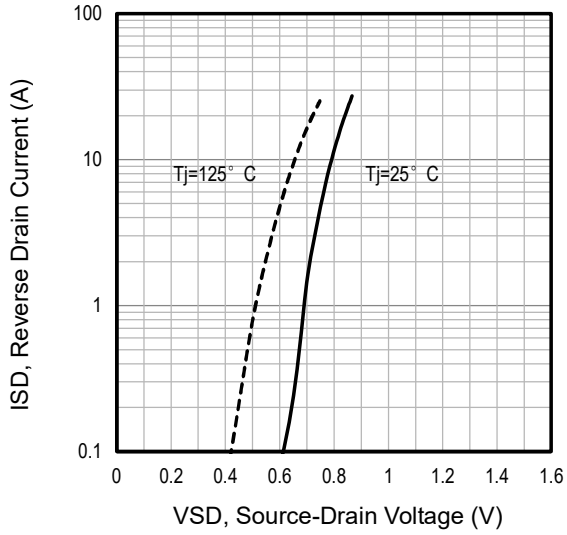


Fig7. Typical Source-Drain Diode Forward Voltage

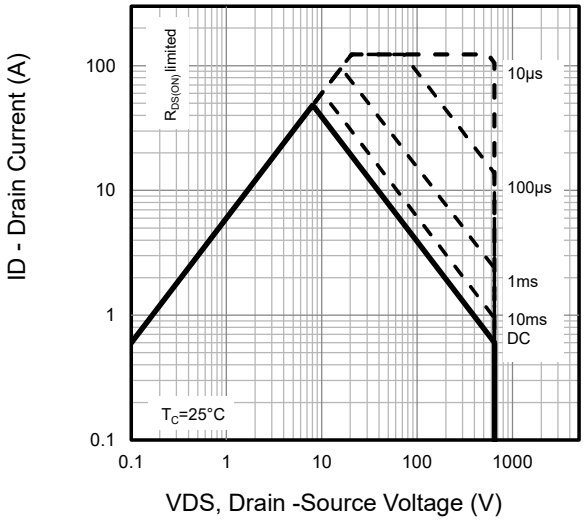


Fig8. Maximum Safe Operating Area

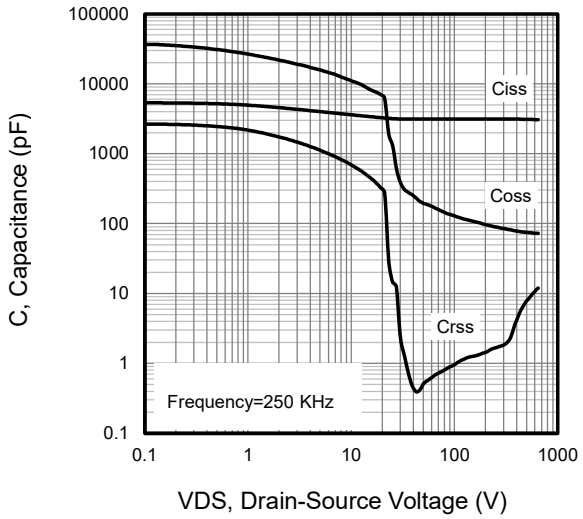


Fig9. Typical Capacitance Vs. Drain-Source Voltage

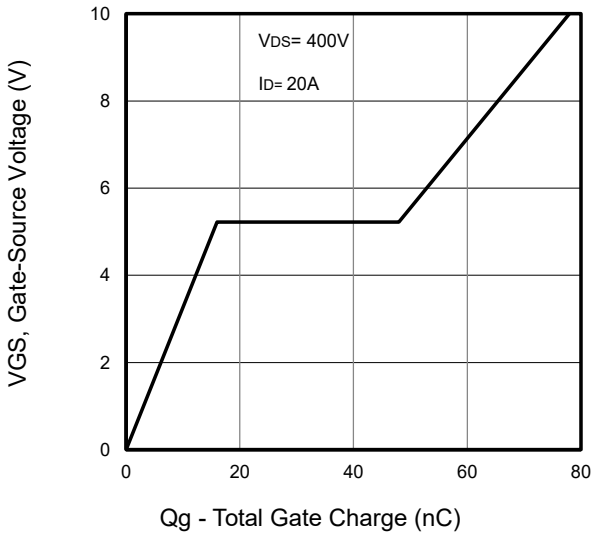


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

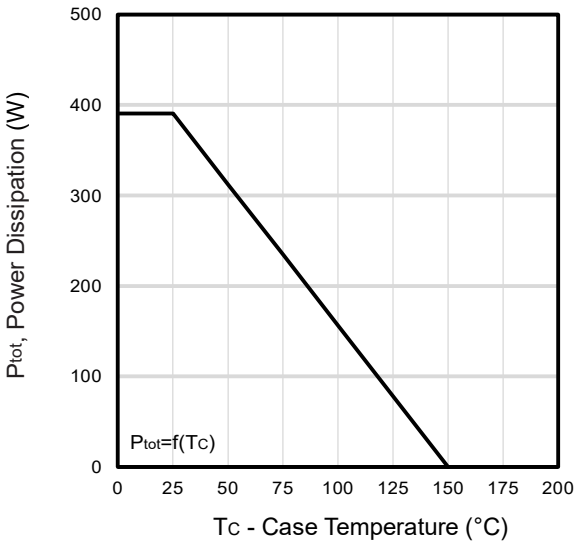


Fig11. Power Dissipation Vs. Case Temperature

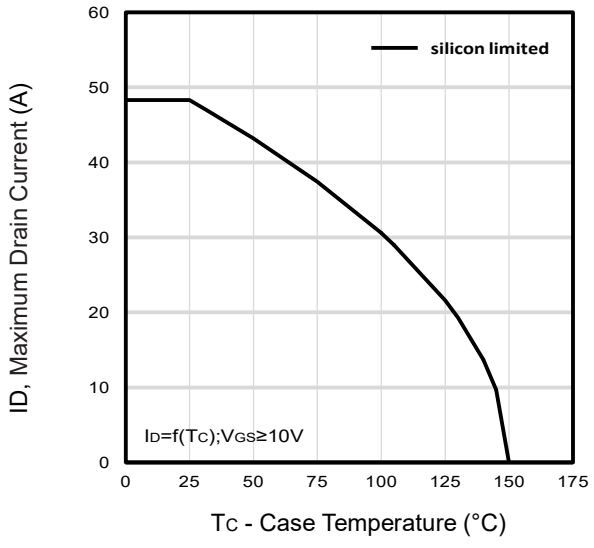


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

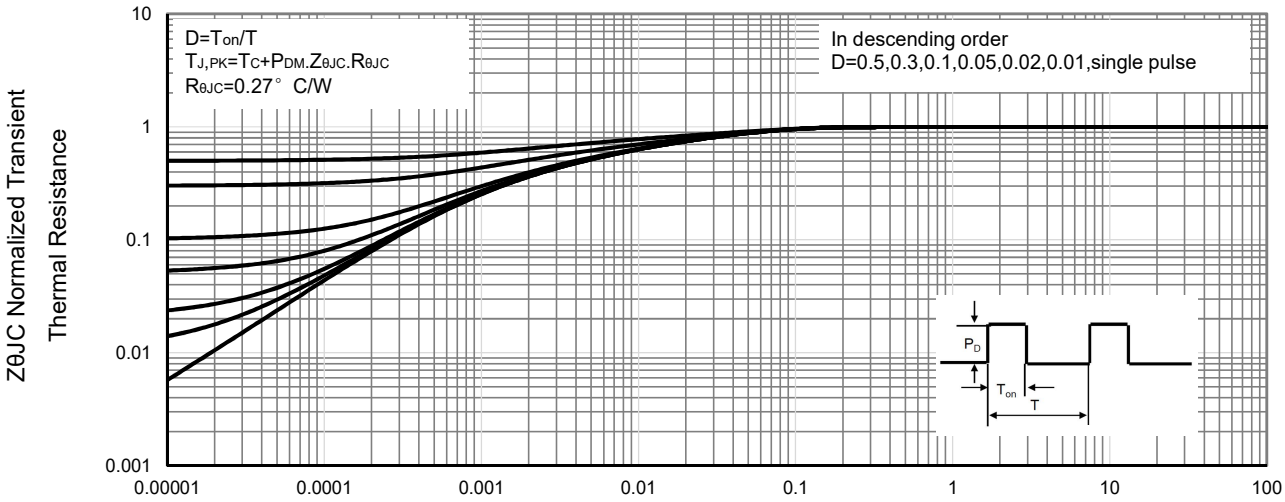


Fig13 . Normalized Maximum Transient Thermal Impedance

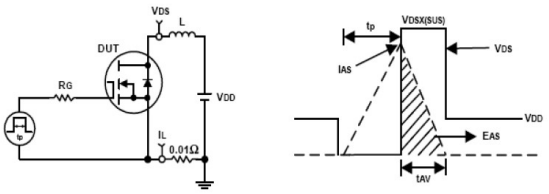


Fig14. Unclamped Inductive Test Circuit and waveforms

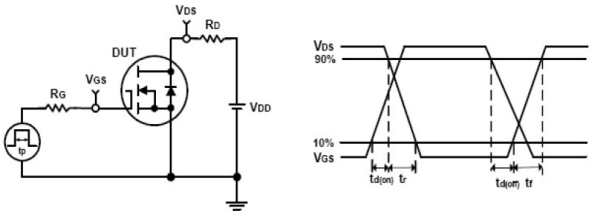
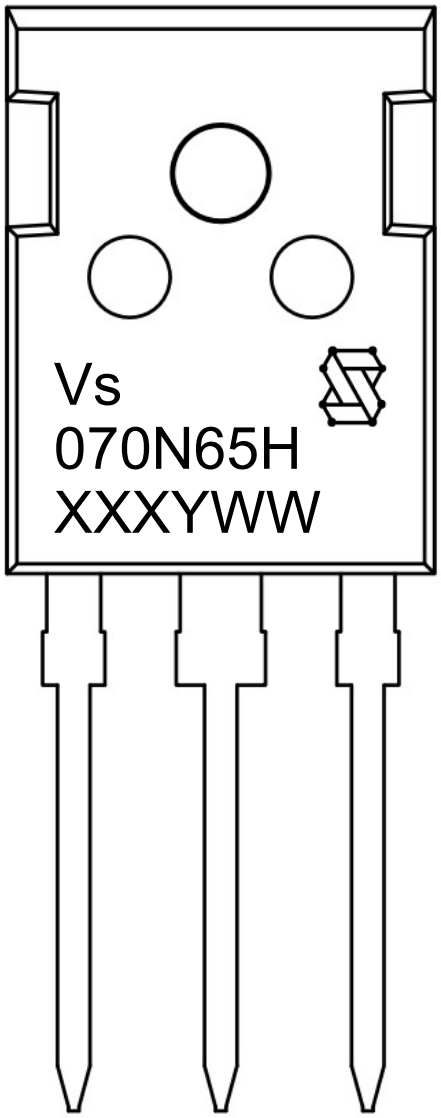


Fig15. Switching Time Test Circuit and waveforms

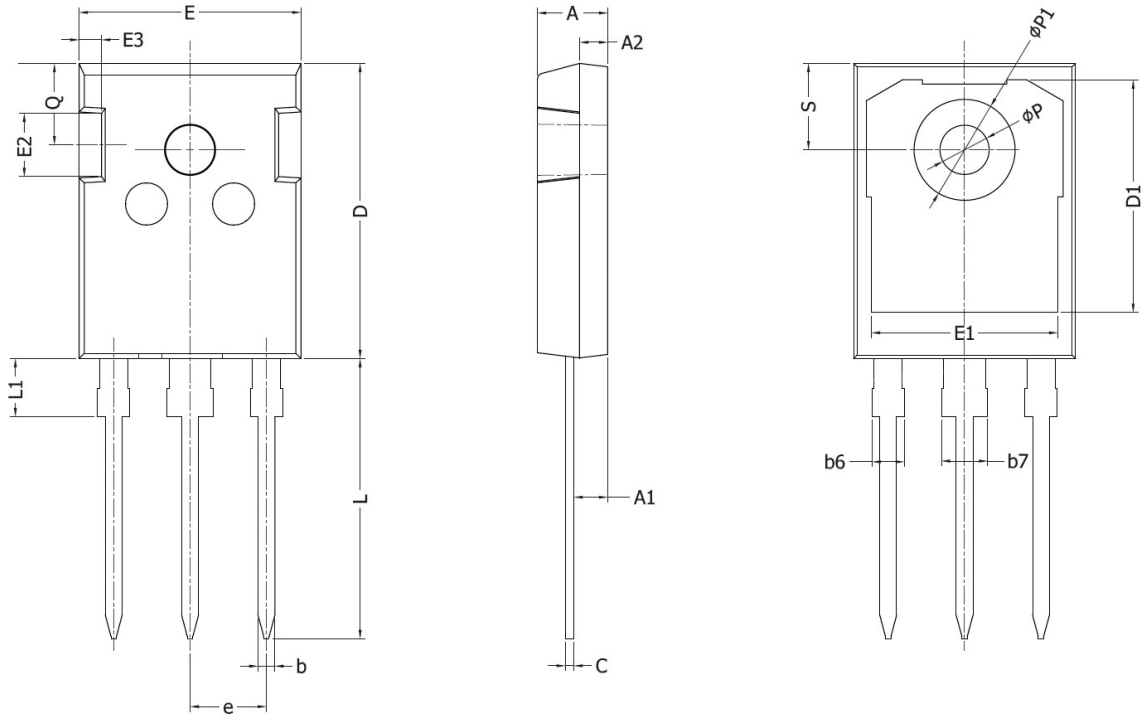
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（070N65H）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Nom	Max
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b6	1.91	--	2.21
b7	2.91	--	3.21
C	0.51	0.61	0.75
D	20.80	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.40	--	5.20
E3	1.50	1.60	1.70
e	5.44 BSC		
L	19.80	19.92	20.22
L1	--	--	4.30
ΦP	3.40	3.60	3.80
ΦP1	7.00	--	7.40
Q	5.60	5.80	6.00
S	6.05	6.15	6.25

Notes:

1. Package Reference: JEDEC TO-247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.