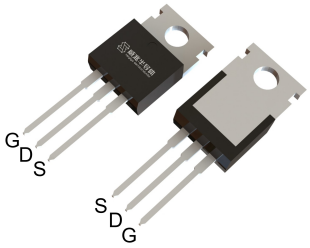
Features

V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	6	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	7.5	mΩ
$I_{D(Silicon\ limited)}$	90	A

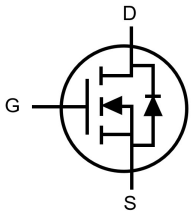
- Enhancement mode
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested,100% Rg Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-220AB



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS1804GTM	TO-220AB	1804GTM	50pcs/Tube



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		100	V
V_{GS}	Gate-source voltage		±20	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	90	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	90	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	64	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	360	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	12	A
		T_A=70°C	10	A
EAS	Maximum avalanche energy, single pulsed ②		156	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	136	W
		T_C = 100°C	68	W
P_{DSM}	Maximum power dissipation ④	T_A=25°C	2.5	W
		T_A=70°C	1.8	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.89	1.1	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250uA	100	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero gate voltage drain current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	1.3	1.8	2.4	V
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=10V, I_D=40A	--	6	8	mΩ
		(Tj=100℃) ⑦	--	9	--	mΩ
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=4.5V, I_D=30A	--	7.5	10.5	mΩ
G_{FS}	Forward transconductance	V_{DS}=5V, I_D=40A	--	52	--	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=100kHz	--	2670	--	pF
Coss	Output capacitance ⑦		--	680	--	pF
Crss	Reverse transfer capacitance ⑦		--	15	--	pF
Rg	Gate resistance	f=1MHz	--	1.4	--	Ω
Qg(10V)	Total gate charge ⑦	V_{DS}=50V,I_D=40A, V_{GS}=10V	--	42	--	nC
Qg(4.5V)	Total gate charge ⑦		--	20	--	nC
Qgs	Gate-source charge ⑦		--	8.9	--	nC
Qgd	Gate-drain charge ⑦		--	6.7	--	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay time	V_{DD}=50V, I_D=40A, R_G=3Ω, V_{GS}=10V	--	11	--	ns
Tr	Turn-on rise time		--	41	--	ns
Td(off)	Turn-off delay time		--	34	--	ns
Tf	Turn-off fall time		--	53	--	ns
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	--	0.92	1	V
Trr	Reverse recovery time ⑦	V_{DD}=50V I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	--	39	--	ns
Qrr	Reverse recovery charge ⑦		--	35	--	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 25A, V_{GS} =10V； 100% FT tested at L = 0.1mH, I_{AS} = 38A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

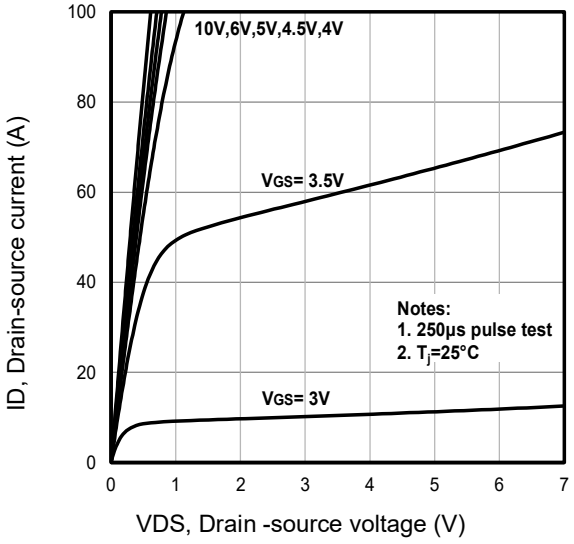


Fig1. Typical output characteristics

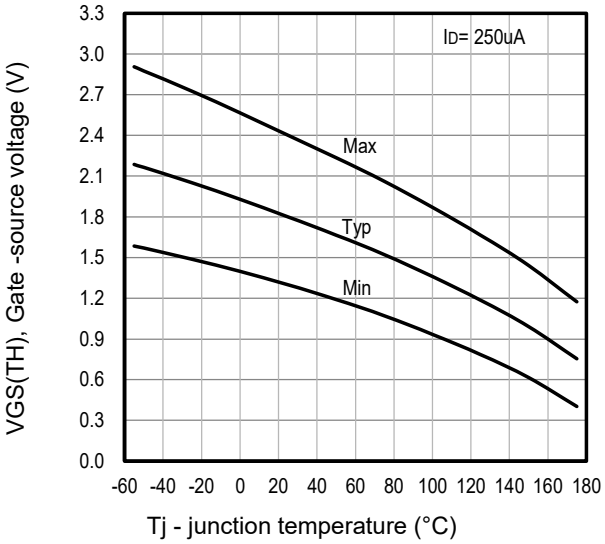


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

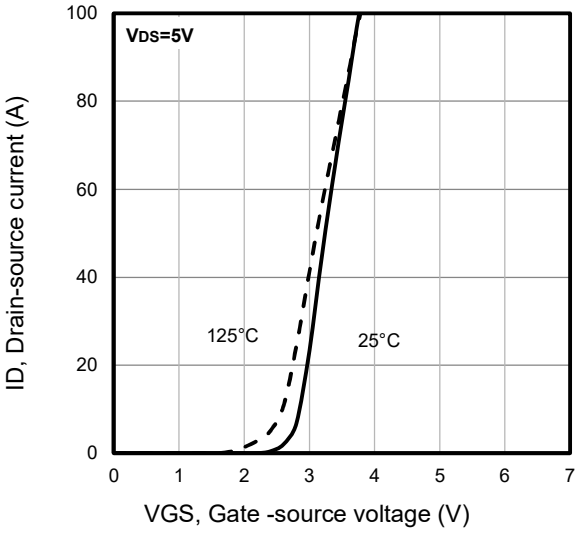


Fig3. Typical transfer characteristics

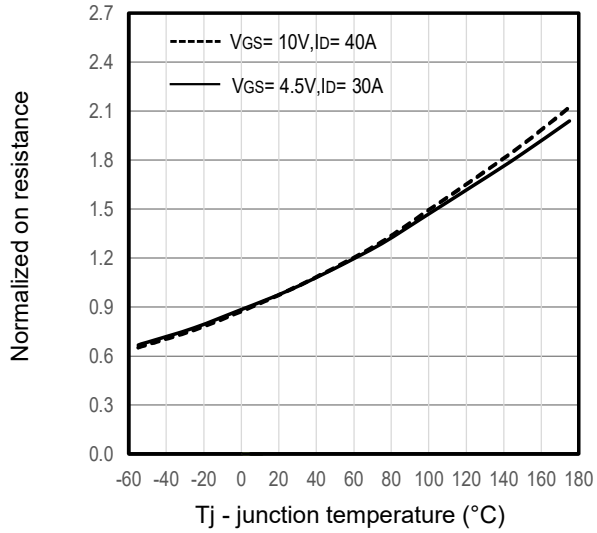


Fig4. Typical normalized on-resistance Vs. Tj

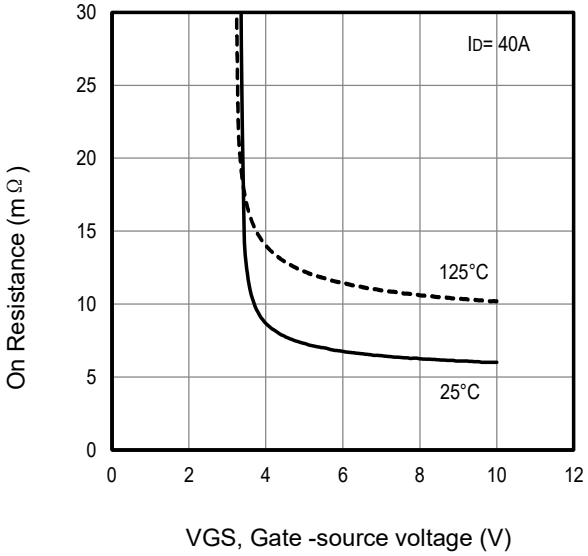


Fig5. Typical on resistance Vs gate -source voltage

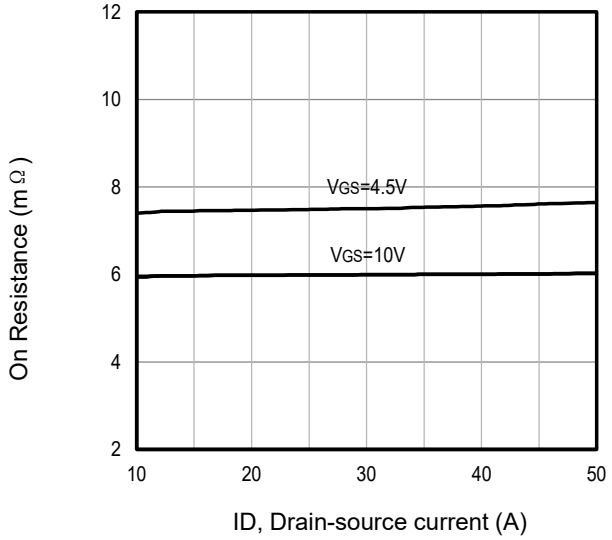


Fig6. Typical on resistance Vs drain current

Typical Characteristics

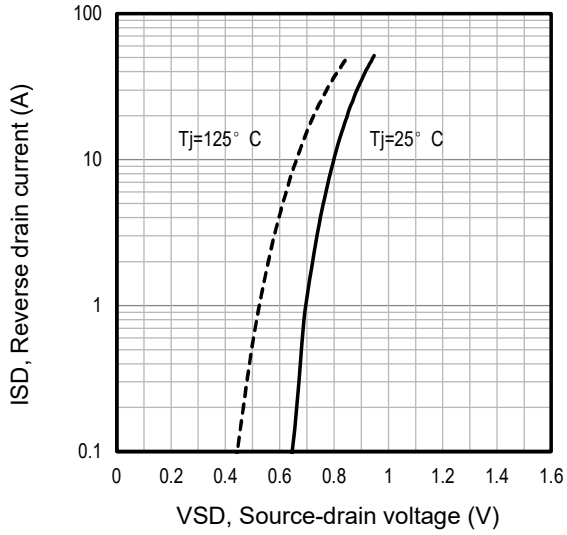


Fig7. Typical source-drain diode forward voltage

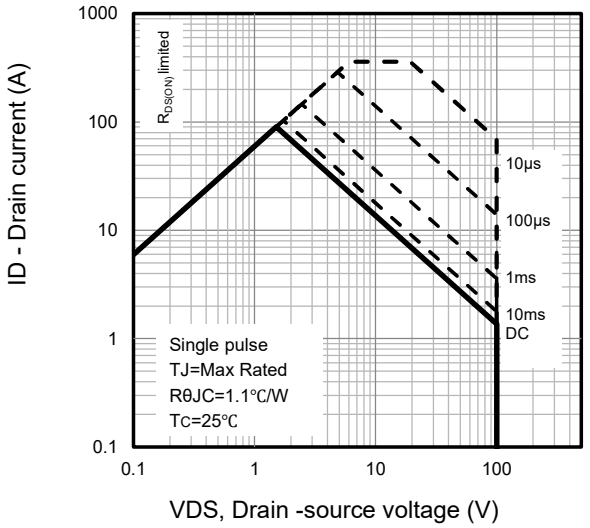


Fig8. Maximum safe operating area

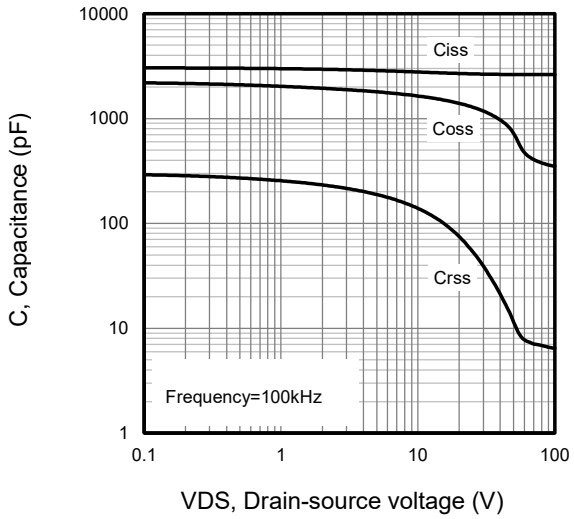


Fig9. Typical capacitance Vs. drain-source voltage

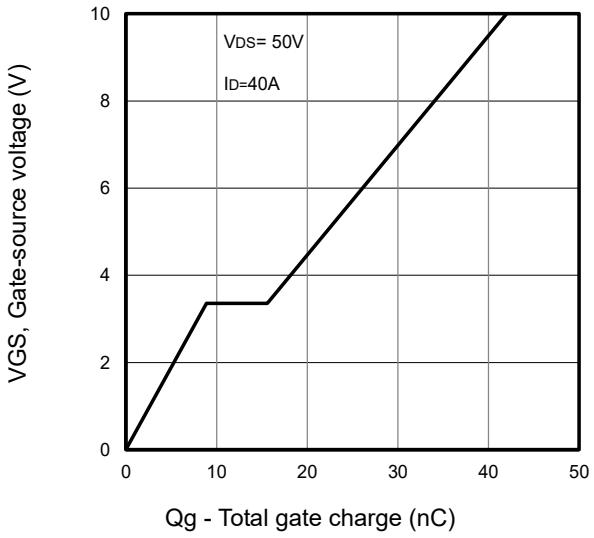


Fig10. Typical gate charge Vs. gate-source voltage

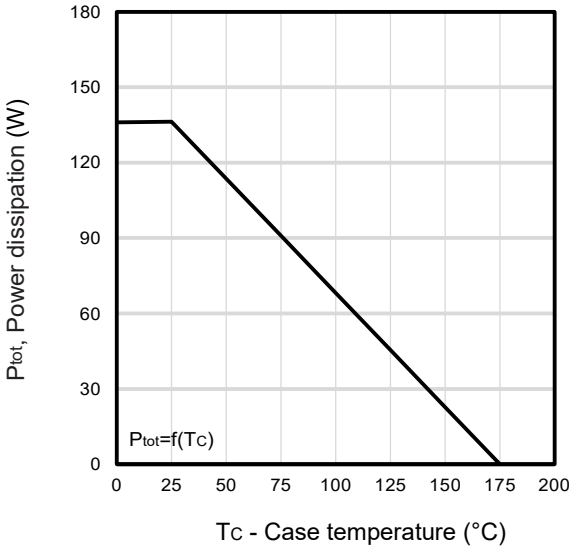


Fig11. Power dissipation Vs. case temperature

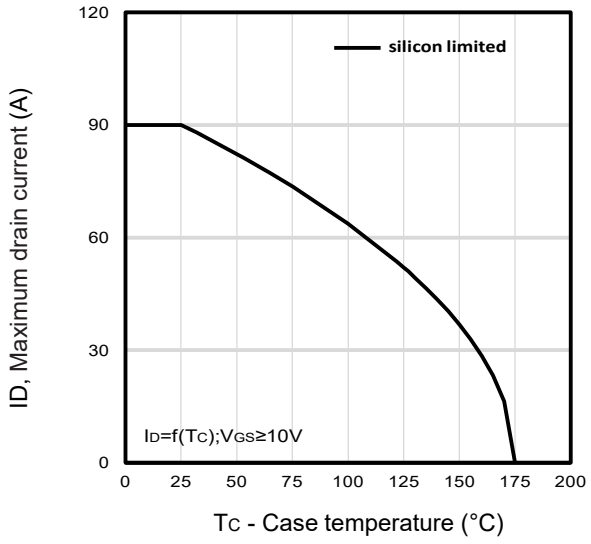


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

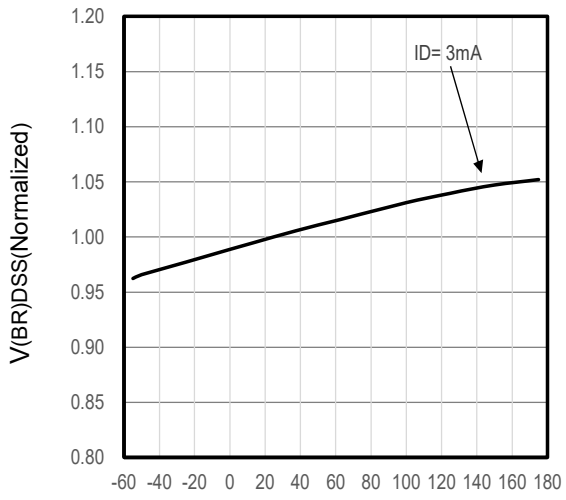


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

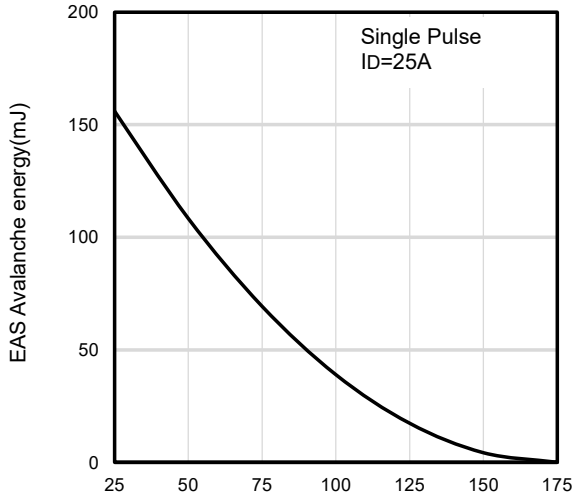


Fig14. Maximum avalanche energy vs temperature (°C)

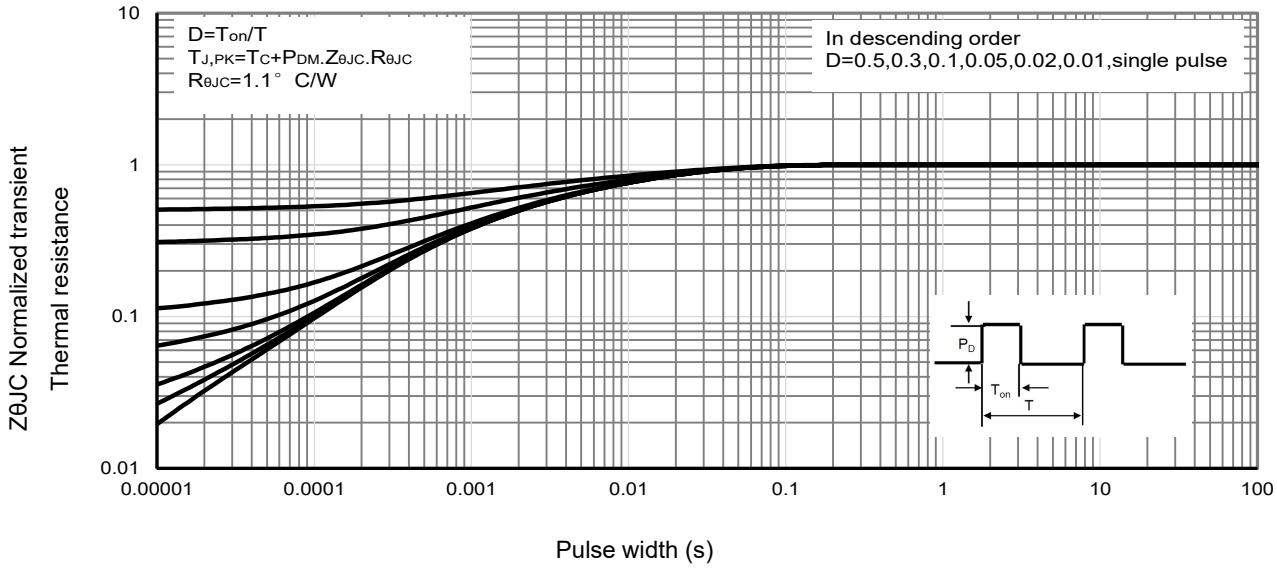


Fig15 . Normalized maximum transient thermal impedance

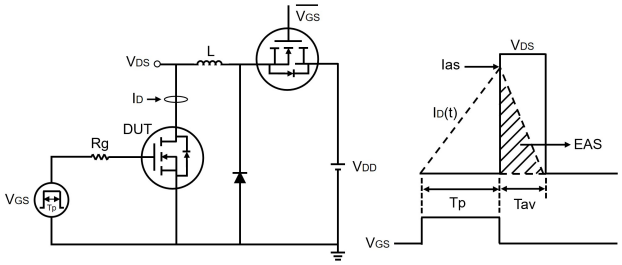


Fig16. Unclamped inductive test circuit and waveforms

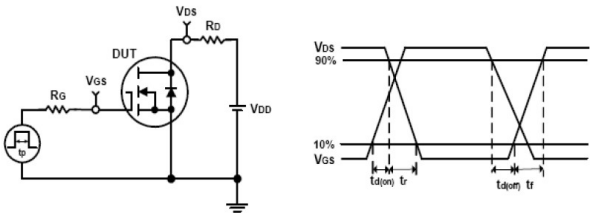
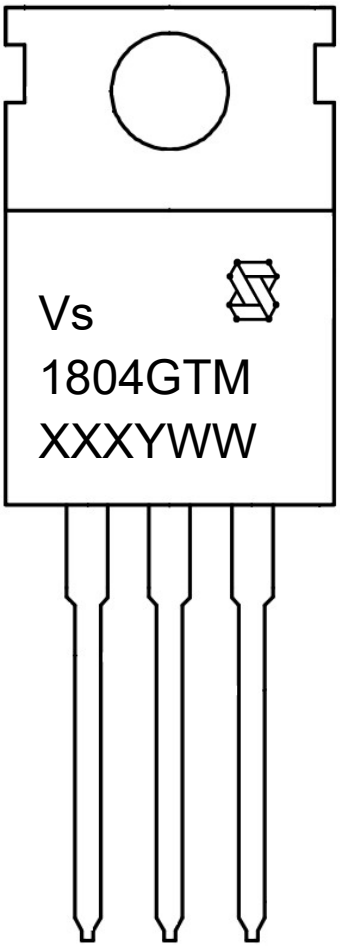


Fig17. Switching time test circuit and waveforms

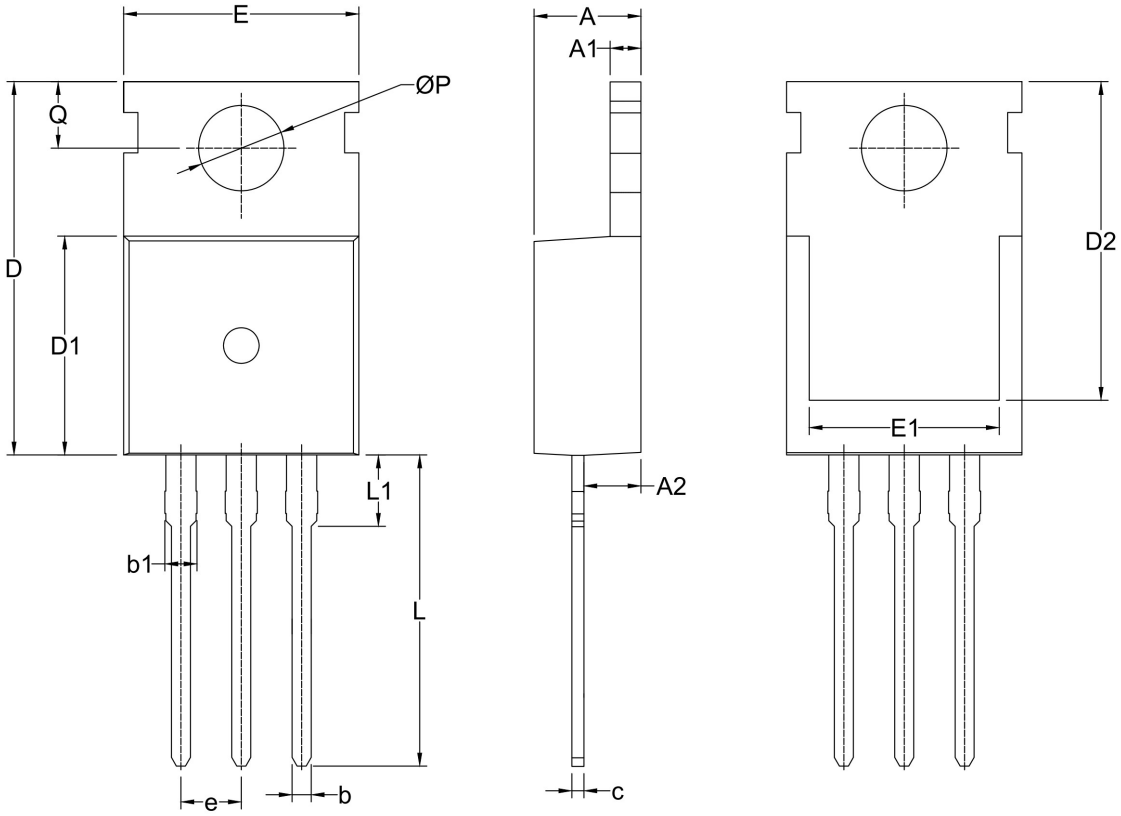
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（1804GTM）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.40	4.50	4.60
A1	1.25	1.30	1.35
A2	2.30	2.40	2.50
b	0.70	0.80	0.90
b1	1.25	1.33	1.42
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	12.80	--	13.70
E	9.70	9.90	10.20
E1	7.50	--	8.20
e	2.54 BSC		
L	12.78	13.28	13.45
L1	--	--	3.50
Q	2.70	2.80	2.90
ΦP	3.55	3.68	3.75

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.