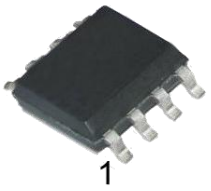
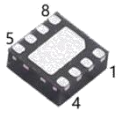
Fault Protected CAN Transceiver with CAN FD

Features

- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- All devices support classic CAN and 5Mbps CAN FD
- I/O Voltage range supports 3.3V and 5V MCUs
- Ideal passive behavior when unpowered
- IEC ESD protection up to ±15kV
- Bus Fault protection: ±70V
- Undervoltage protection
- Driver dominant time out (TXD DTO)
- Thermal shutdown protection
- Receiver common mode input voltage: ±30V
- SOP-8 package and DFN-8 3*3 package



SOP-8



DFN-8 3*3

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
TJA1051M/TR	SOP-8	A1051	REEL	2500pcs/reel
TJA1051DQ3/TR	DFN-8 3*3	A1051	REEL	5000pcs/reel
TJA1051-3M/TR	SOP-8	A1051-3	REEL	2500pcs/reel
TJA1051-3DQ3/TR	DFN-8 3*3	A51-3	REEL	5000pcs/reel

Description

The TJA1051 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to a CAN protocol controller.

The TJA1051 offer offers improved EMC and ESD performance, and also features:

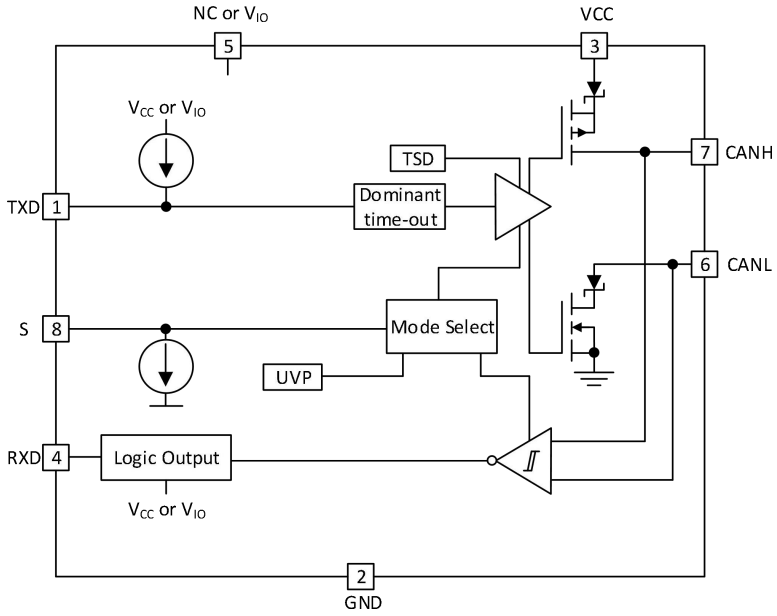
- Ideal passive behavior to the CAN bus when the supply voltage is off
- Variants with a V_{IO} pin can be interfaced directly with microcontrollers with supply voltages from 3.3V to 5V

The TJA1051 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5Mbps.

Applications

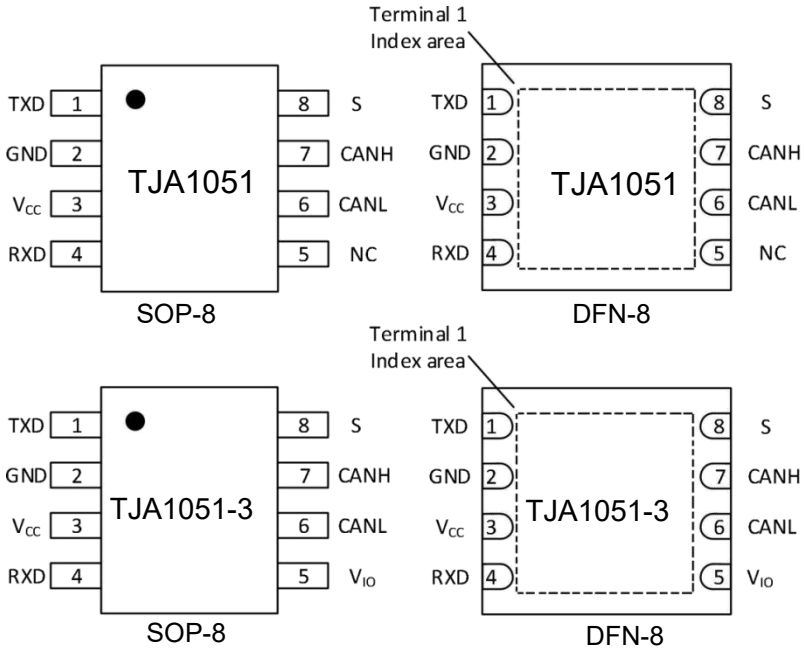
- Automotive and Transportation
- All devices support highly loaded CAN networks
- Heavy machinery ISOBUS applications ISO 11783

Block Diagram



Functional Block Diagram

Pin Configurations and Functions



Pin Functions

Pins		TYP	Description
Name	No.		
TXD	1	DIGITAL INPUT	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
GND(1)	2	GND	Ground connection
V_{CC}	3	POWER	Transceiver 5V supply voltage
RXD	4	DIGITAL OUTPUT	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
NC	5	-	No Connect
V_{IO}	5	POWER	Transceiver I/O level shifting supply voltage
CANL	6	BUS I/O	Low level CAN bus input/output line
CANH	7	BUS I/O	High level CAN bus input/output line
S	8	DIGITAL INPUT	Silent Mode control input (active high)

Note:(1) For DFN-8 package options, the thermal pad may be connected to GND in order to optimize the thermal characteristics of the package.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

Symbol	Parameter		MIN	MAX	UNIT
V_{CC}	5V Supply Voltage Range	All Devices	-0.3	7	V
V_{IO}	I/O Level-Shifting Voltage Range	For devices in this series with VIO ports	-0.3	7	V
V_{BUS}	CAN Bus I/O voltage range (CANH, CANL)		-70	70	V
$V_{(Diff)}$	Max differential voltage between CANH and CANL		-70	70	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range (TXD, S)	All Devices	-0.3	+7 and $V_I \le V_{IO}$ + 0.3	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range (RXD)		-0.3	+7 and $V_I \le V_{IO}$ + 0.3	V
$I_{O(RXD)}$	RXD (Receiver) output current		-8	8	mA
T_J	Virtual junction temperature range		-55	150	°C
T_{STG}	Storage temperature range		-65	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)		-	260	°C

Note:(1)Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.Exposure to absolute-maximum-rated condition for extended periods may affect device reliability.
(2)All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

ESD Ratings

Parameter	Test Conditions	VALUE	UNIT
Human Body Model (HBM) ESD stress voltage	All terminals	±8000	V
	CAN bus terminals (CANH, CANL)	±15000	
Charged Device Model (CDM) ESD stress voltage	All terminals	±2000	V
IEC Contact Discharge (IEC 61000-4-2)	CAN bus terminals (CANH, CANL)	±8000	

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	UNIT
V_{CC}	5V Supply Voltage Range	4.5	5.5	V
V_{IO}	I/O Level-Shifting Voltage Range	3	5.5	
$I_{OH(RXD)}$	RXD terminal HIGH level output current	-2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current		2	

Electrical Characteristics

Over recommended operating conditions (unless otherwise noted).

Symbol	Parameter		Test Conditions	Min	Typ(1)	Max	Unit
Supply Characteristics							
I_{CC}	5V supply current	Normal mode (dominant)	See **Figure 6-1**, TXD = 0V, R_L = 60Ω,C_L = open, R_{CM} = open, S = 0V		40	70	mA
			See **Figure 6-1**, TXD = 0V, R_L = 50Ω,C_L = open, R_{CM} = open,S = 0V		45	80	
		Normal mode (dominant– with bus fault)	See **Figure 6-1**, TXD = 0V, S = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} =open			180	
		Normal mode (recessive)	See **Figure 6-1**, TXD = V_{CC} , R_L = 50Ω,C_L = open, R_{CM} = open, S = 0V		0.6	1.0	
		Silent mode	See **Figure 6-1**,TXD = V_{CC}, R_L = 50Ω,C_L = open, R_{CM} = open, S = V_{CC}		2.2	5	μA
I_{IO}	I/O supply current	Normal and Silent modes	RXD floating, TXD = S = 0 or 5.5V		100	300	
UV_{VCC}	Rising undervoltage detection on V_{CC} for protected mode		All devices		3.2	3.4	V
	Falling undervoltage detection on V_{CC} for protected mode			2.8	3.0	3.25	
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV
UV_{VIO}	Undervoltage detection on V_{IO} for protected mode		Device with V_{IO} pin	1.3		2.75	V
$V_{HYS(UVVIO)}$	Hysteresis voltage on UV_{VIO} for protected mode				80		mV
S Terminal (Mode Select Input)							
V_{IH}	High-level input voltage		Devices with V_{IO} pin	0.7V_{IO}			V
			Devices without V_{IO} pin	2			
V_{IL}	Low-level input voltage		Devices with V_{IO} pin			0.3V_{IO}	
			Devices without V_{IO} pin			0.8	
I_{IH}	High-level input leakage current		S = V_{CC} = V_{IO} = 5.5V	-2	0	2	μA
I_{IL}	Low-level input leakage current		S = 0V, V_{CC} = V_{IO} = 5.5V	-15	-10	-2	
$I_{LKG(OFF)}$	Unpowered leakage current		S = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	1	

Electrical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices with V_{IO} pin	$0.7V_{IO}$			V
		Devices without V_{IO} pin	2			
V_{IL}	Low-level input voltage	Devices with V_{IO} pin			$0.3V_{IO}$	
		Devices without V_{IO} pin			0.8	
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	-2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC} = V_{IO} = 5.5V	-100	-40	-7	
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5V, V_{CC} = V_{IO} = 0V	-1	0	1	
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	Devices with V_{IO} pin, See **Figure 6-2** , I_O = –2mA	$0.8V_{IO}$			V
		Devices without V_{IO} pin, See **Figure 6-2** , I_O = –2mA	4	4.6		
V_{OL}	Low-level output voltage	Devices with V_{IO} pin, See **Figure 6-2** , I_O = +2mA			$0.2V_{IO}$	
		Devices without V_{IO} pin, See **Figure 6-2** , I_O = +2mA		0.2	0.4	
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5V, V_{CC} = 0V, V_{IO} = 0V	-1	0	-1	µA
Receiver Electrical Characteristics						
V_{CM}	Common mode range, Normal mode	See **Figure 6-2** ,**Table 7-5** and **Table 6-1**,S = 0 or V_{CC} or V_{IO}	-30		+30	V
V_{IT+}	Positive-going input threshold voltage, all modes	See **Figure 6-2** ,**Table 7-5** and **Table 6-1**, S = 0 or V_{CC} or V_{IO}, -20V ≤ V_{CM} ≤ +20V			900	mV
V_{IT-}	Negative-going input threshold voltage, all modes		500			mV
V_{IT+}	Positive-going input threshold voltage, all modes	See **Figure 6-2** ,**Table 7-5** and **Table 6-1**, S = 0 or V_{CC} or V_{IO}, -30V ≤ V_{CM} ≤ +30V			1000	mV
V_{IT-}	Negative-going input threshold voltage, all modes		400			mV
V_{HYS}	Hysteresis voltage (V_{IT+} - V_{IT-})	See **Figure 6-2** ,**Table 7-5** and **Table 6-1**,S = 0 or V_{CC} or V_{IO}		120		mV
$I_{lkg(IOFF)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5V, V_{CC} = V_{IO} = 0V			4.8	µA
R_{ID}	Differential input resistance	TXD = V_{CC} = V_{IO} = 5V, S = 0V, -30V ≤ V_{CM} ≤ +30V	20	30	50	kΩ
R_{IN}	Input resistance (CANH or CANL)		10	15	25	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5V	-2%		+2%	

Electrical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted).

Symbol	Parameter		Test Conditions	Min	Typ(1)	Max	Unit
Driver Electrical Characteristics							
$V_{O(DOM)}$	Bus output voltage (dominant)	CANH	See **Figure 7-2** and **Figure 6-1**, TXD = 0V, S = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	2.75	3.6	4.5	V
		CANL		0.5	1.4	2.25	
$V_{O(REC)}$	Bus output voltage (recessive)	CANH and CANL	See **Figure 7-2** and **Figure 6-1**, TXD = V_{CC}, V_{IO} = V_{CC}, S = V_{CC} or 0V(2), R_L = open (no load), R_{CM} = open	2	0.5V_{CC}	3	
$V_{OD(DOM)}$	Differential output voltage (dominant)	CANH - CANL	See **Figure 7-2** and **Figure 6-1**, TXD = 0V, S = 0V, 45Ω ≤ R_L < 50Ω, C_L = open, R_{CM} = open	1.4		3	
			See **Figure 7-2** and **Figure 6-1**, TXD = 0V, S = 0V, 50Ω ≤ R_L ≤ 65Ω, C_L = open, R_{CM} = open	1.5	2.2	3	
			See **Figure 7-2** and **Figure 6-1**, TXD = 0V, S = 0V, R_L = 2240Ω, C_L = open, R_{CM} = open	1.5		5	
$V_{OD(REC)}$	Differential output voltage (recessive)	CANH - CANL	See **Figure 7-2** and **Figure 6-1**, TXD = V_{CC}, S = 0V, R_L = 60Ω, C_L = open, R_{CM} =open	-120		20	mV
			See **Figure 7-2** and **Figure 6-1**, TXD = V_{CC}, S = 0V, R_L = open (no load), C_L = open, R_{CM} = open	-50		50	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC}		See **Figure 6-1** and **Figure 8-2**, S at 0V, Rterm = 60Ω, Csplit = 4.7nF, C_L = open, R_{CM} = open, TXD = 250kHz, 1MHz	0.9		1.1	V/V
V_{SYM_DC}	DC Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See **Figure 6-1** and **Figure 7-2**, S = 0V, R_L = 60Ω, C_L = open, R_{CM} = open	-0.4		0.4	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current,dominant		See **Figure 7-2** and **Figure 6-7**, S at 0V, V_{CANH} = -5V to 40V, CANL = open, TXD = 0V	-100			mA
			See **Figure 7-2** and **Figure 6-7**, S at 0V, V_{CANL}= -5V to 40V, CANH = open, TXD = 0V			100	
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current,recessive		See **Figure 7-2** and **Figure 6-7**, –27V ≤ V_{BUS} ≤ 32V, Where V_{BUS} = CANH = CANL,TXD = V_{CC}, all modes	-5		5	mA

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5V and V_{IO} = 5V , R_L = 60Ω.

(2) For the bus output voltage (recessive) will be the same if the device is in Normal mode with S terminal LOW or if the device is in Silent mode with the S terminal is HIGH

Switching Characteristics

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See **Figure 6-4**, S = 0V, R_L = 60Ω,C_L = 100pF, $C_{L(RXD)}$ = 15pF		110	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive			130	200	
t_{MODE}	Mode change time, from Normal to Silent or from Silent to Normal	See **Figure 6-3**,		20	45	μs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	See **Figure 6-1**, STB = 0V, R_L = 60Ω, C_L = 100pF, R_{CM} = open		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			65		
$t_{sk(p)}$	Pulse skew ($\|t_{pHR} - t_{pLD}\|$)			15		
t_R	Differential output signal rise time			45		
t_F	Differential output signal fall time			45		
SR	Differential output slew rate, dominant-to-recessive transition				70	V/μs
t_{TXD_DTO}	Dominant timeout	S = 0V, R_L = 60Ω, C_L = open, See **Figure 6-6**	1.2	2	3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input tohigh output (Dominant to Recessive)	See **Figure 6-2**, STB = 0V, $C_{L(RXD)}$ = 15pF		55		ns
t_{pDL}	Propagation delay time, bus dominant input tolow output (Recessive to Dominant)			55		ns
t_R	RXD Output signal rise time			10		ns
t_F	RXD Output signal fall time			10		ns
FD Timing Parameters						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500ns, all devices	See **Figure 6-5** , S = 0V, R_L = 60Ω, C_L = 100pF, C_L(RXD) = 15pF, $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200ns, only without V_{IO} pin devices		155		210	
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500ns, all devices		400		550	
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200ns, only without V_{IO} pin devices		120		220	
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns, all devices		-65		40	
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns, only without V_{IO} pin devices		-45		15	

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5V and V_{IO} = 5V (if applicable), R_L = 60Ω

Parameter Measurement Information

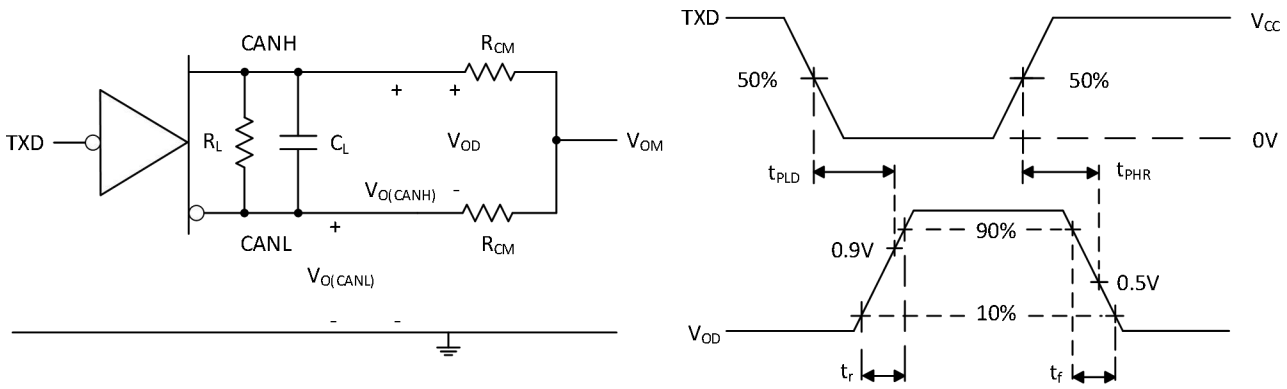


Figure 6-1. Driver Test Circuit and Measurement

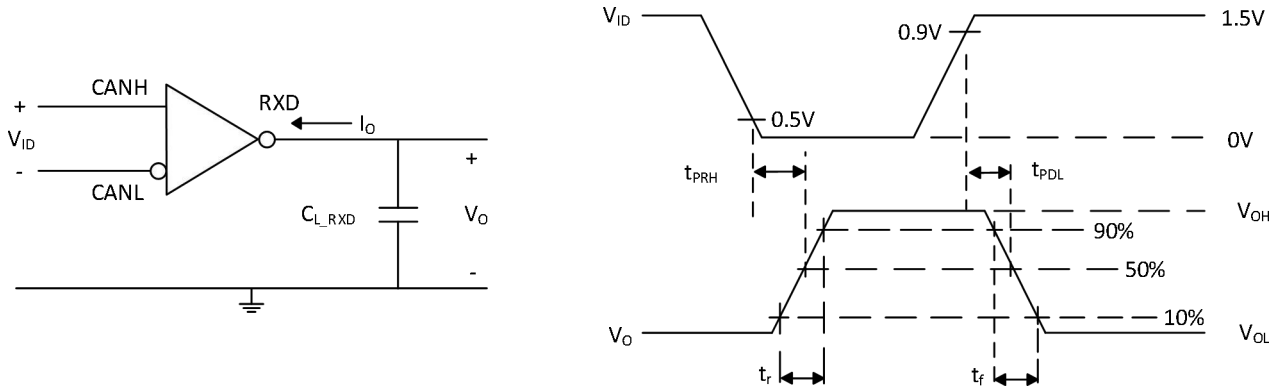


Figure 6-2. Receiver Test Circuit and Measurement

Table 6-1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-29.5 V	-30.5 V	1000mV	L	V_{OL}
30.5 V	29.5 V	1000mV	L	
-19.55 V	-20.45 V	900mV	L	
20.45 V	19.55 V	900mV	L	
-19.75 V	-20.25 V	500mV	H	V_{OH}
20.25 V	19.75 V	500mV	H	
-29.8 V	-30.2 V	400mV	H	
30.2 V	29.8 V	400mV	H	
Open	Open	X	H	

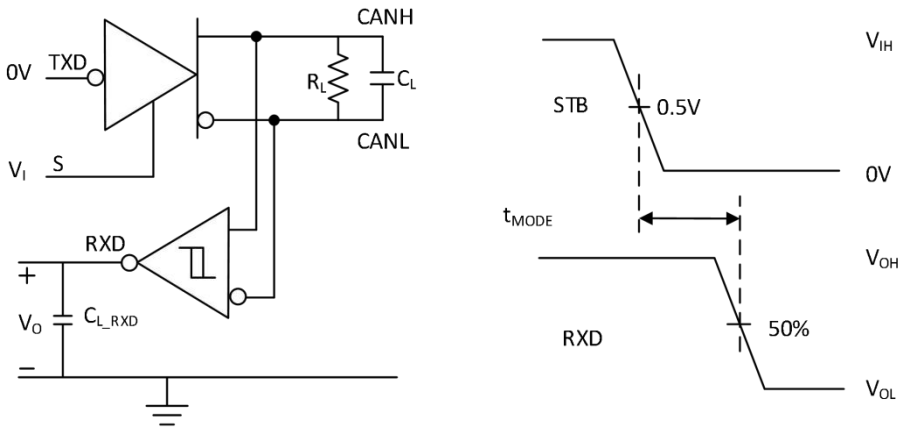


Figure 6-3. t_{MODE} Test Circuit and Measurement

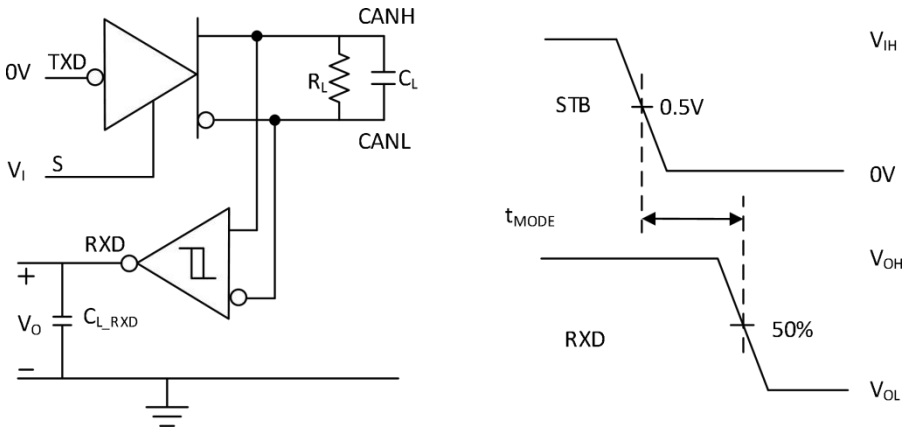


Figure 6-4. $T_{PROP(LOOP)}$ Test Circuit and Measurement

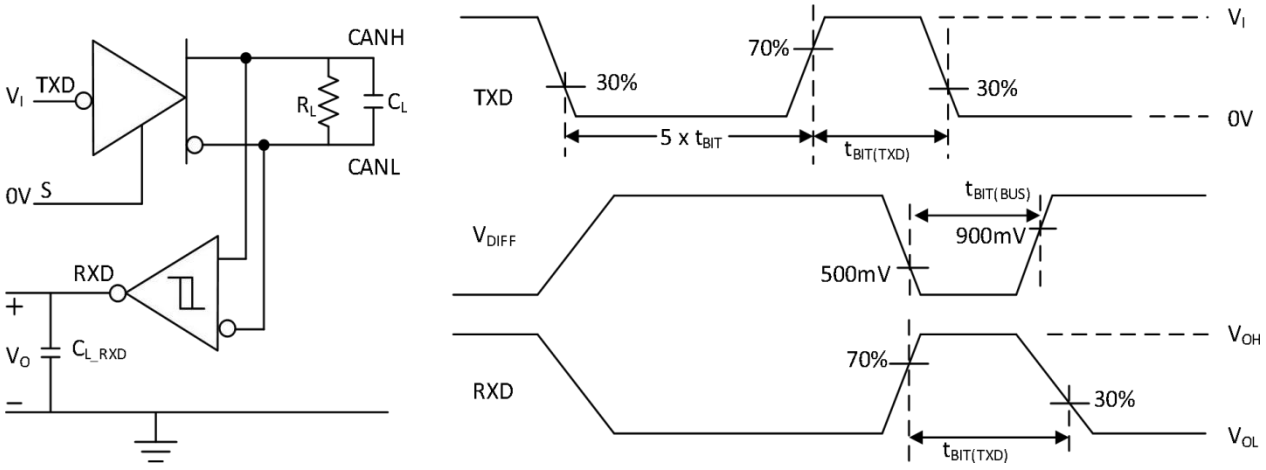


Figure 6-5. CAN FD Timing Parameter Measurement

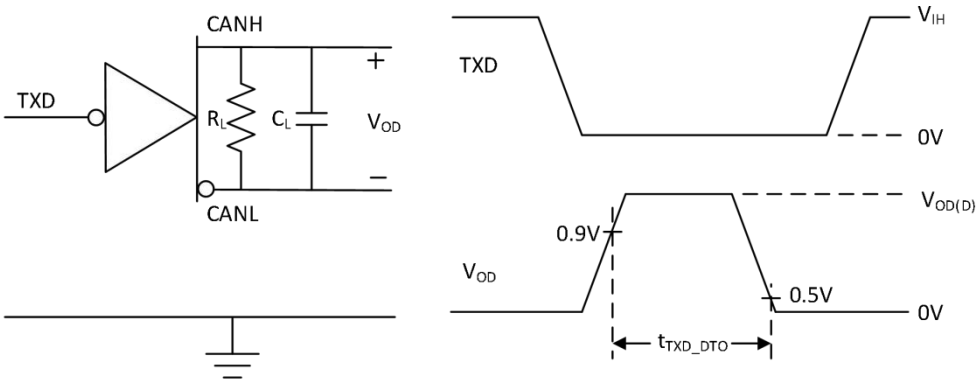


Figure 6-6. TXD Dominant Timeout Test Circuit and Measurement

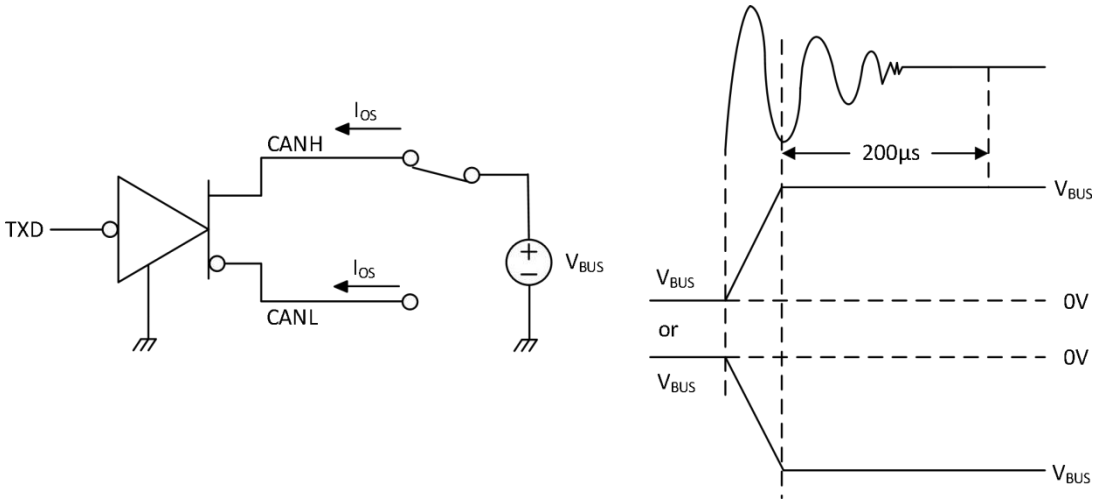


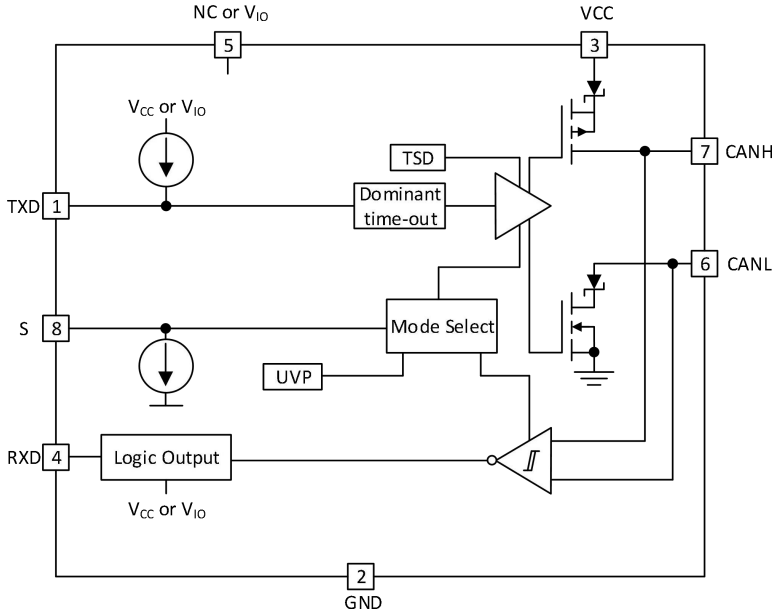
Figure 6-7. Driver Short Circuit Current Test and Measurement

Detailed Description

Overview

These CAN transceivers meet the ISO11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. They are designed for data rates in excess of 1 Mbps for CAN FD and enhanced timing margin / higher data rates in long and highly-loaded networks. These devices provide many protection features to enhance device and CAN robustness.

Functional Block Diagram



Feature Description

TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

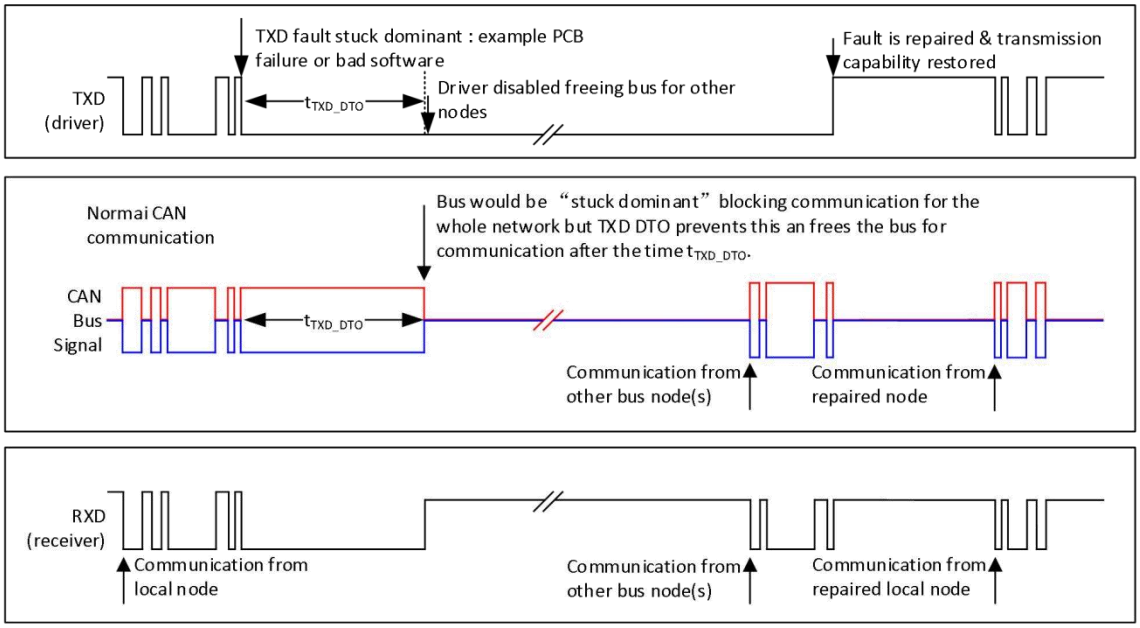


Figure 7-1. Example Timing Diagram for TXD DTO

Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuits thus blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature (T_{TSD_HYS}) below the thermal shutdown temperature (T_{TSD}) of the device.

Undervoltage Lockout

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{IO} supply terminals.

Table 7-1. Undervoltage Lockout 5V Only Devices without V_{IO} pin

VCC	Device State(1)	Bus Output	RXD
> UV_{VCC}	Normal	Per TXD	Mirrors Bus(2)
< UV_{VCC}	Protected	High Impedance	High Impedance

(1) See the V_{IT} section of the Electrical Characteristics.

(2) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 7-2. Undervoltage Lockout only Devices with V_{IO} pin

V_{CC}	V_{IO}	Device State	Bus Output	RXD
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors Bus(1)
< UV_{VCC}	> UV_{VIO}	Protected	High Impedance	High (Recessive)
> UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance
< UV_{VCC}	< UV_{VIO}	Protected	High Impedance	High Impedance

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

Floating Terminals

These devices have internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} or V_{IO} to force a recessive input level if the terminal floats. The S terminal is also pulled down to force the device into Normal mode if the terminal floats.

CAN Bus Short Circuit Current Limiting

The device has two protection features that limit the short circuit current when a CAN bus line is short-circuit fault condition: driver current limiting (both dominant and recessive states) and TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the instantaneous current during each bus state or as an average current of the two states.

Digital Inputs and Outputs

5V V_{CC} Only (Devices without V_{IO} pin):

The 5V V_{CC} only devices are supplied by a single 5V rail. The digital inputs have TTL input thresholds and are therefore 5V and 3.3V compatible. The RXD outputs on these devices are driven to the V_{CC} rail for logic high output. Additionally, the TXD pin is internally pulled up to V_{CC}, and the S pin is pulled low to GND. The internal bias of the mode pins may only place the device into a known state if the terminals float, they may not be adequate for system-level biasing during transients or noisy enviroments.

5V V_{CC} with V_{IO} I/O Level Shifting (Devices with V_{IO} pin):

These devices use a 5V V_{CC} power supply for the CAN driver and high speed receiver blocks. These transceivers have a second power supply for I/O level-shifting (V_{IO}). This supply is used to set the CMOS input thresholds of the TXD and S pins and the RXD high level output voltage. Additionally, the TXD pin is internally pulled up to V_{IO}, and the S pin is pulled low to GND.

Device Functional Modes

The device has two main operating modes: Normal mode and Silent mode. Operating mode selection is made via the S input terminal.

Table 7-3. Operating Modes

S Terminal	Mode	Driver	Receiver	RXD Terminal
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State(1)

CAN Bus States

The CAN bus has two states during powered operation of the device: dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals.

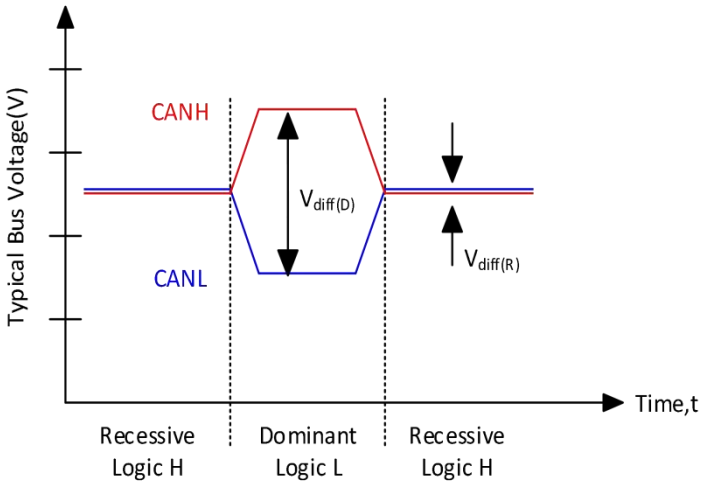


Figure 7-2. Bus States (Physical Bit Representation)

Normal Mode

Select the Normal mode of device operation by setting S terminal low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver translates a digital input on TXD to a differential output on CANH and CANL. The receiver translates the differential signal from CANH and CANL to a digital output on RXD.

Silent Mode

Activate Silent mode by setting S terminal high. The CAN driver is disabled, preventing communication from the TXD pin to the CAN bus. The high speed receiver remains active so that CAN bus communication continues to be relayed to the RXD output pin.

Driver and Receiver Function Tables

Table 7-4. Driver Function Table

Device	Inputs		Outputs		Driven Bus State
	STB(1)	TXD(1) (2)	CANH(1)	CANL(1)	
All Devices	L or Open	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Z = common mode (recessive) bias to V_{CC}/2. See CAN Bus States for bus state and common mode bias information.

(2) Devices have an internal pull up to V_{CC} or V_{IO} on TXD terminal. If the TXD terminal is open, the terminal is pulled high and the transmitter remain in recessive (non-driven) state.

Table 7-5. Receiver Function Table

Device mode	CAN Differential Inputs $V_{ID}=V_{CANH} - V_{CANL}$	Bus State	RXD Terminal(1)
Normal or Silent	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	L(2)
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	?	?(2)
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	H(2)
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.

(2) See Receiver Electrical Characteristics section for input thresholds.

Application and Implementation

Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5V and 3.3V microprocessor applications. The bus termination is shown for illustrative purposes.

Typical Applications

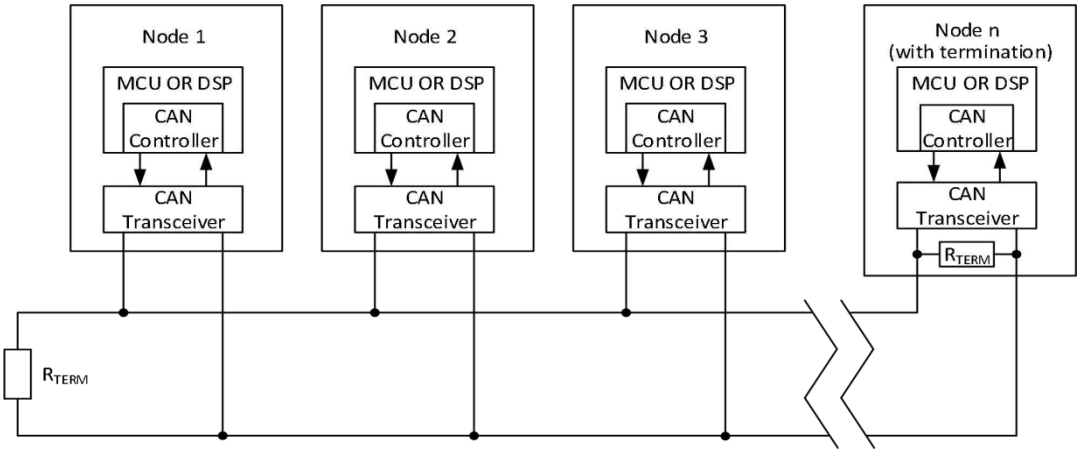


Figure 8-1. Typical CAN Bus Application

Design Requirements

Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TJA1051 family of transceivers. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus.

The TJA1051 family is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TJA1051 family is a minimum of 30kΩ. If 100 TJA1051 family transceivers are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the TJA1051 family theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

Detailed Design Procedures

CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network.

Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 8-2). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

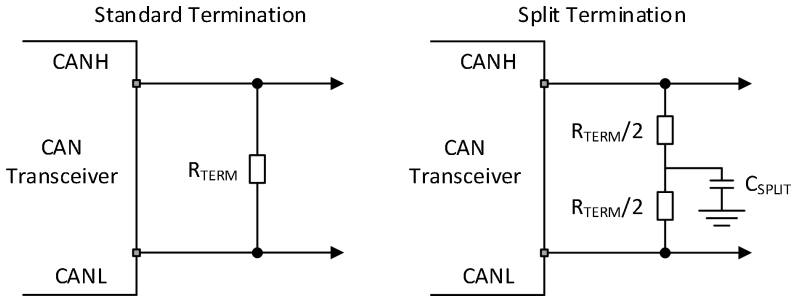


Figure 8-2. CAN Bus Termination Concepts

The family of transceivers have variants for both 5V only applications and applications where level shifting is needed for a 3.3V microcontroller.

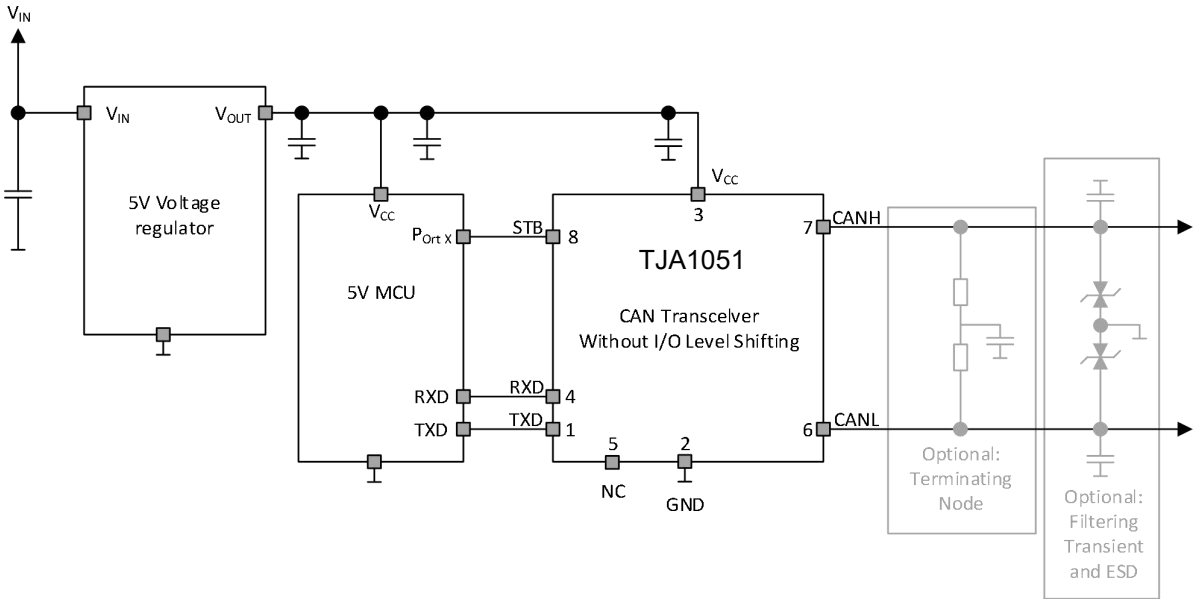


Figure 8-3. Typical CAN Bus Application Using 5V CAN Controller

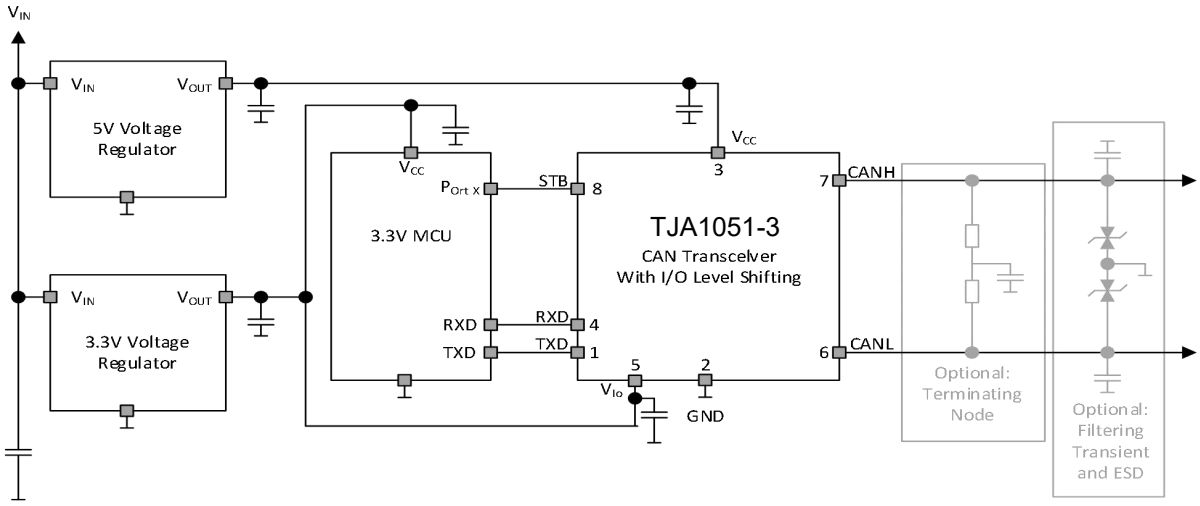


Figure 8-4. Typical CAN Bus Application Using 3.3V CAN Controller

Power Supply Recommendations

These devices are designed to operate from a V_{CC} input supply voltage range between 4.5V and 5.5V. Some devices have an output level shifting supply input, V_{IO}, designed for a range between 3V and 5.5V. Both supply inputs must be well regulated. A bulk capacitance, typically 4.7µF, should be placed near the CAN transceiver's main V_{CC} supply output, and in addition a bypass capacitor, typically 0.1µF, should be placed as close to the device V_{CC} and V_{IO} supply terminals. This helps to reduce supply voltaeg ripple present on the outputs of the switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes and traces.

Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial enviroments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The TJA1051 family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

Layout Guidelines

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.
- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1, C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two
- resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C3. Split
- termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For devices in this series with VIO ports, bypass capacitors should be placed as close to the pin as possible (example C6 and C7). For device options without V_{IO} I/O level shifting, this pin is not internally connected and can be left floating or tied to any existing net, for example a split pin connection.
- Terminal 8: is shown assuming the mode terminal, S, will be used. If the device will only be used in normal mode, R4 is not needed and R5 could be used for the pull down resistor to GND.

Layout Example

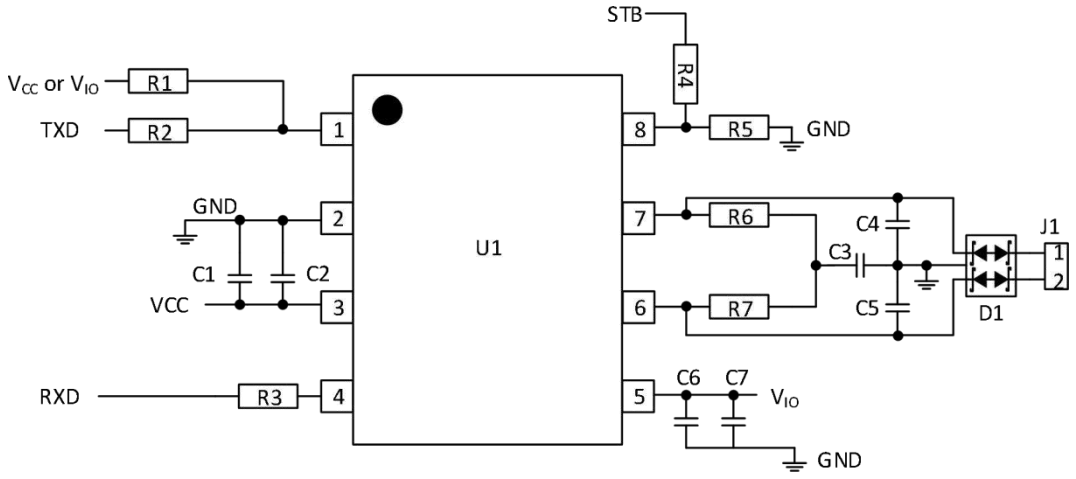
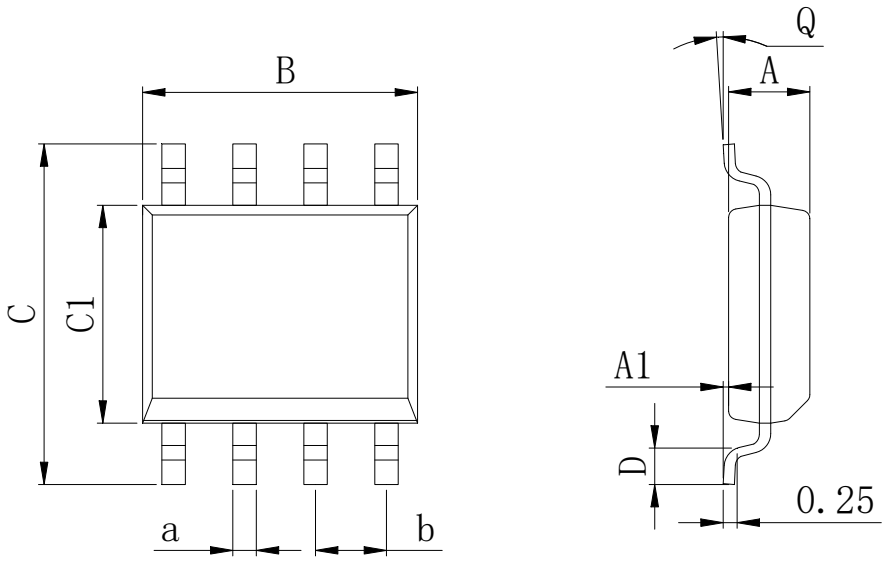


Figure 10-1. Layout Example

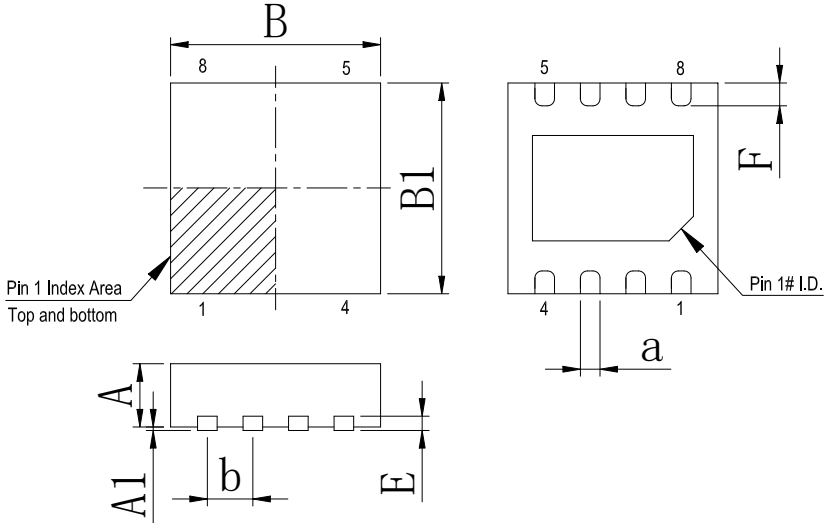
Physical Dimensions

SOP-8 (150mil)



Dimensions In Millimeters(SOP-8)									
Symbol:	**A**	**A1**	**B**	**C**	**C1**	**D**	**Q**	**a**	**b**
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

DFN-8 3*3



Dimensions In Millimeters(DFN-8 3*3)								
Symbol:	**A**	**A1**	**B**	**B1**	**E**	**F**	**a**	**b**
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2015-11	New	1-22
V1.1	2025-1	Document Reformatting	1-22

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