Features

- **Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates, Up to 100 Mbps, 50Mbps Clock**
- **Type-1 Receivers: 25 mV Hysteresis**
- **-1 V to 3.4 V Common-Mode Voltage Range**
- **Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Disabled or VCC ≤ 1.5 V**
- **Bus-Pin Protection: ±8 kV HBM model**
- **–40°C to 85°C Operation Temperature Range**

Description

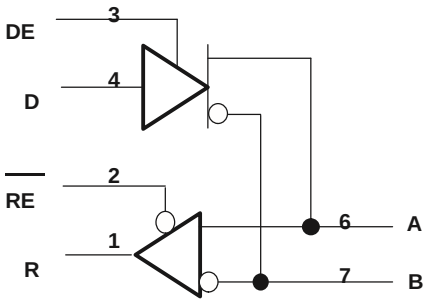
The TPT9H111 is a 3.3V Multipoint-Low-Voltage Differential (M-LVDS) line driver and receiver, which can support 100 Mbps data rates. Driver outputs and receiver inputs are protected against ±8kV ESD strikes without latch-up. The driver output has been designed to support multipoint buses with the loads no less than 30 Ω, and can support the controlled slew rate on drivers.

The TPT9H111 is Type-1 receiver that detects the bus state with a differential input of 50 mV over a common-mode voltage range of -1 V to 3.4 V. The receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. The device is characterized for operation from –40°C to 85°C. The device is available as half-duplex in an 8-lead SOP package.

Applications

- Backplane Multipoint Data/Clock Transmission
- Cellular Base Stations
- Network Switches and Routers
- Industrial Control
- Communication Infrastructure

Simplified Schematic



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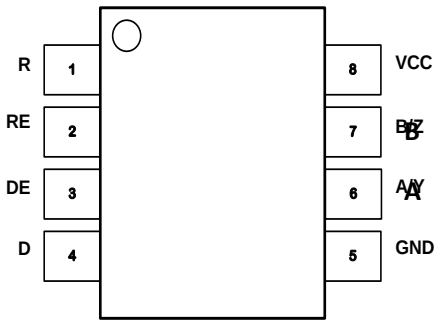
Revision History

Date	Revision	Notes
2018/12/14	Rev. Pre 0.1	Definition Draft
2019/03/27	Rev.0	Release Version, confirm spec limit
2023/07/12	Rev.A1	Updated the typo in figure1 in page 11, updated the package information in page 16&17

Pin Configuration and Functions

TPT9H111

SOP8



in No.	Pin Name	I/O	Description
1	R	Digital output	Receiver Output
2	/RE	Digital input	Receiver Output Enable
3	DE	Digital input	Driver Output Enable
4	D	Digital input	Driver Input
5	GND	Ground	Ground
6	A	Bus input	Noninverting Receiver Input
7	B	Bus input	Inverting Receiver Input
8	V_{CC}	Power	Power Supply

Device Function Tables

Table 1. Truth Table Abbreviations

Abbreviation	Description
H	High level
L	Low level
X	Don’t care
I	Indeterminate
Z	High impedance
NC	Disconnected

Table 2. Driver

Inputs	Enable	Outputs	
D	**DE**	**A**	**B**
L	H	L	H
H	H	H	L
Open	H	L	H
X	Open	Z	Z
X	L	Z	Z

Table 3. Type-1 Receiver

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	**RE**	**R**
$V_{ID} \geq 50$ mV	L	H
–50 mV < V_{ID} < 50 mV	L	?
$V_{ID} \leq$ –50 mV	L	L
X	H	Z
X	Open	Z

Table 4. Type-1 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT
V_{IA}	**V_{IB}**	**V_{ID}**	**V_{IC}**	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.425	3.335	0.050	3.4	H
3.375	3.425	–0.050	3.4	L
–0.975	–1.025	0.050	–1	H
–1.025	–0.975	–0.050	–1	L

Absolute Maximum Ratings Note 1

Parameters	Rating
V_{CC} to GND	–0.5 V to 4 V
Voltage at Logic pin: D, DE, /RE, R Note 2	-0.3V to 4V
Voltage at Bus pin: A, B	-1.8V to +4V
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

ESD Rating

		Value	Unit
HBM, ANSI/ESDA/JEDEC JS-001	Bus Pin	8	kV
	All Pin Except Bus Pin	4	kV
CDM, ANSI/ESDA/JEDEC JS-002	All Pin	1	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOP	130		°C/W

Note: θ_{JA} =130°C/W is typical value of SOP8 provided by package assembly house

Recommended Operation Conditions

		Min	Typ	Max	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal V_A, V_B	–1.4		3.8	V
$\lvert V_{ID} \rvert$	Magnitude of differential input voltage	0.05		VCC	V
T_A	Operating free-air temperature	–40		85	°C

Electrical Characteristics

All test condition is V_{CC} = 3.0 to 3.6V, T_A = -40°C to 85°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Icc	Driver only	RE and DE at V_{CC}, R_L = 50 Ω, All others open		13	22	mA
	Both disabled	RE at V_{CC}, DE at 0 V, R_L = No Load, All others open		2	4	mA
	Both enabled	RE at 0 V, DE at V_{CC}, R_L = 50 Ω, All others open		15	24	mA
	Receiver only	RE at 0 V, DE at 0 V, R_L = 50 Ω, All others open		4	13	mA
I_A	Receiver or transceiver with driver disabled input current	V_A = 3.8 V, V_B = 1.2 V,	0		32	µA
		V_A = 0 V or 2.4 V, V_B = 1.2 V	–20		20	µA
		V_A = –1.4 V, V_B = 1.2 V	–32		0	µA
I_B	Receiver or transceiver with driver disabled input current	VB = 3.8 V, VA = 1.2 V	0		32	µA
		VB = 0 V or 2.4 V, VA = 1.2 V	–20		20	µA
		VB = –1.4 V, VA = 1.2 V	–32		0	µA
I_{AB}	Receiver or transceiver with driver disabled differential input current (I_A – I_B)	V_A = V_B, 1.4 ≤ V_A ≤ 3.8 V	-4		4	µA
$I_{A (OFF)}$	Receiver or transceiver power-off input current	V_A = 3.8 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	0		32	µA
		V_A = 0 V or 2.4 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–20		20	µA
		V_A = –1.4 V, V_B = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	–32		0	µA
$I_{B (OFF)}$	Receiver or transceiver power-off input current	V_B = 3.8 V, V_A = 1.2 V, 0 V ≤ V_{CC} ≤ 1.5 V	0		32	µA
		VB = 0 V or 2.4 V, VA = 1.2 V, 0 V ≤ VCC ≤ 1.5 V	–20		20	µA
		VB = –1.4 V, VA = 1.2 V, 0 V ≤ VCC ≤ 1.5 V	–32		0	µA
$I_{AB(OFF)}$	Receiver input or transceiver power-off differential input current (I_A – I_B)	V_A = V_B, 0 V ≤ V_{CC} ≤ 1.5 V, –1.4 ≤ V_A ≤ 3.8 V	–4		4	µA

All test condition is V_{CC} = 3.0 to 3.6V, T_A = -40°C to 85°C, unless otherwise noted.

Driver Electrical Characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$\|V_{AB}\|$	Differential output voltage magnitude	See Figure 1	480		650	mV
$\Delta\|V_{AB}\|$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 2	0.8		1.2	V
$\Delta V_{OS (SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 6	0		VCC	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		VCC	V

$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 4			1.2 Vcc	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		–0.2 Vcc			V
I_{IH}	High-level input current (D, DE)	V_{IH} = 2 V	0		10	µA
I_{IL}	Low-level input current (D, DE)	V_{IL} = 0.8 V	0		10	µA
$\|I_{OS}\|$	Differential short-circuit output current magnitude	See Figure 3			75	mA
I_{OZ}	High-impedance state output current (driver only)	–1.4 V ≤ V_Y or V_Z ≤ 3.8 V, Other output = 1.2 V	–32		32	µA

All test condition is V_{CC} = 3.0 to 3.6V, T_A = -40°C to 85°C, unless otherwise noted.

Driver Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4		3.3		ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.9		ns
t_r	Differential output signal rise time			1.6		ns
t_f	Differential output signal fall time			1.8		ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			450		ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)	100 MHz clock input(4)		1		ps
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 5		4.5		ns
t_{PLZ}	Disable time, low-level-to-high-impedance output			3.5		ns
t_{PZH}	Enable time, high-impedance-to-high-level output			4.0		ns
t_{PZL}	Enable time, high-impedance-to-low-level output			5.0		ns

All test condition is V_{CC} = 3.0 to 3.6V, T_A = -40°C to 85°C, unless otherwise noted.

Receiver Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IT+}	Positive-going differential input voltage threshold	See Figure 8 and Table 1 and Table 2			50	mV
V_{IT-}	Negative-going differential input voltage threshold		-50			mV
V_{HYS}	Differential input voltage hysteresis, ($V_{IT+} - V_{IT}$)			25		mV
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current (RE)	V_{IH} = 2 V	–10		0	µA
I_{IL}	Low-level input current (RE)	V_{IL} = 0.8 V	–10		0	µA
I_{OZ}	High-impedance output current	V_O = 0 V or 3.6 V	-10		15	µA

C_A or C_B	Input capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V,(2) Other input at 1.2 V		7		pF
C_{AB}	Differential input capacitance	V_{AB} = 0.4 sin(30E6πt) V(2)		7		pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)		0.99		1.01	

All test condition is V_{CC} = 3.0 to 3.6V, T_A = -40°C to 85°C, unless otherwise noted.

Receiver Switching Characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
t_{pLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 9	2	4.5	6	ns
t_{pHL}	Propagation delay time, high-to-low-level output		2	4.8	6	ns
t_r	Output signal rise time			0.9	2.3	ns
t_f	Output signal fall time			0.8	2.3	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)			100		ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) (3)	100 MHz clock input		1		ps
t_{pHZ}	Disable time, high-level-to-high-impedance output	See Figure 10		4.6		ns
t_{pLZ}	Disable time, low-level-to-high-impedance output			3.2		ns
t_{pZH}	Enable time, high-impedance-to-high-level output			7.4		ns
t_{pZL}	Enable time, high-impedance-to-low-level output			3.4		ns

Test Circuits, Configurations and Waveforms

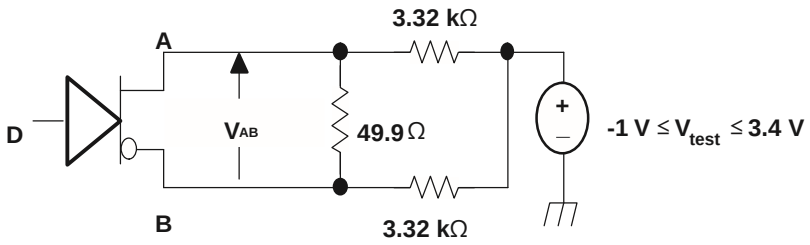


Figure 1. Differential Output Voltage Test Circuit

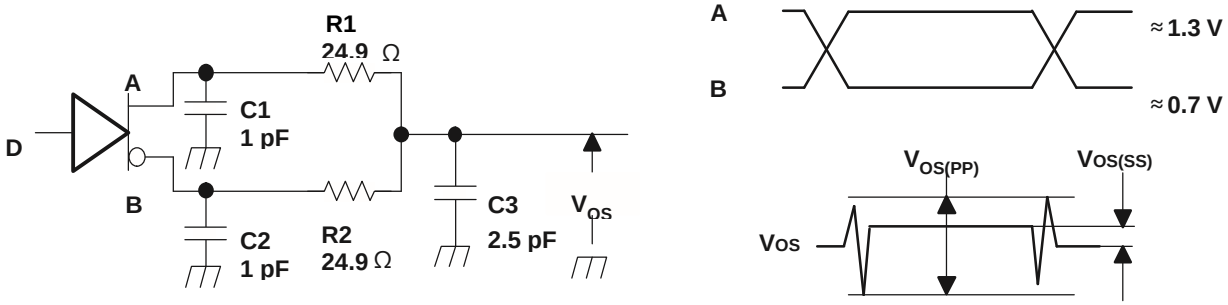


Figure 2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

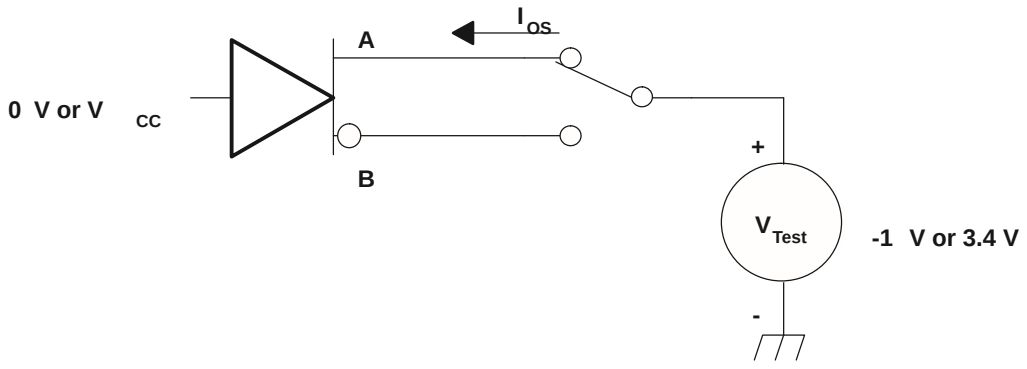


Figure 3. Driver Short-Circuit Test Circuit

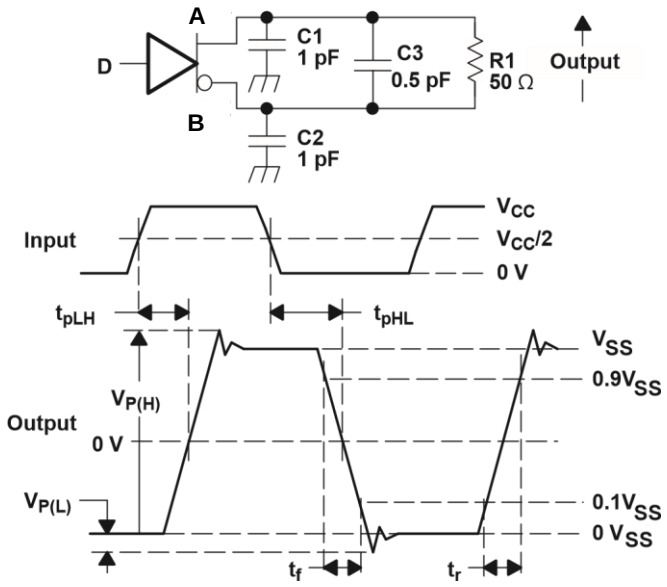


Figure 4. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

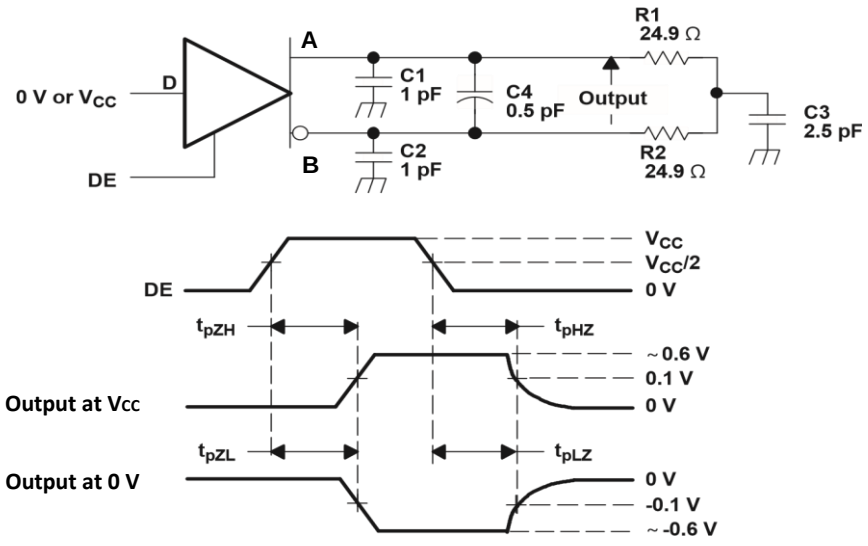


Figure 5. Driver Enable and Disable Time Circuit and Definitions

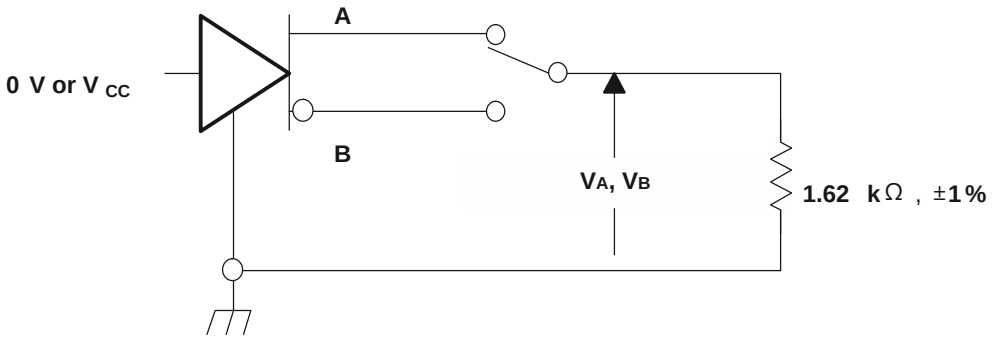


Figure 6. Maximum Steady State Output Voltage

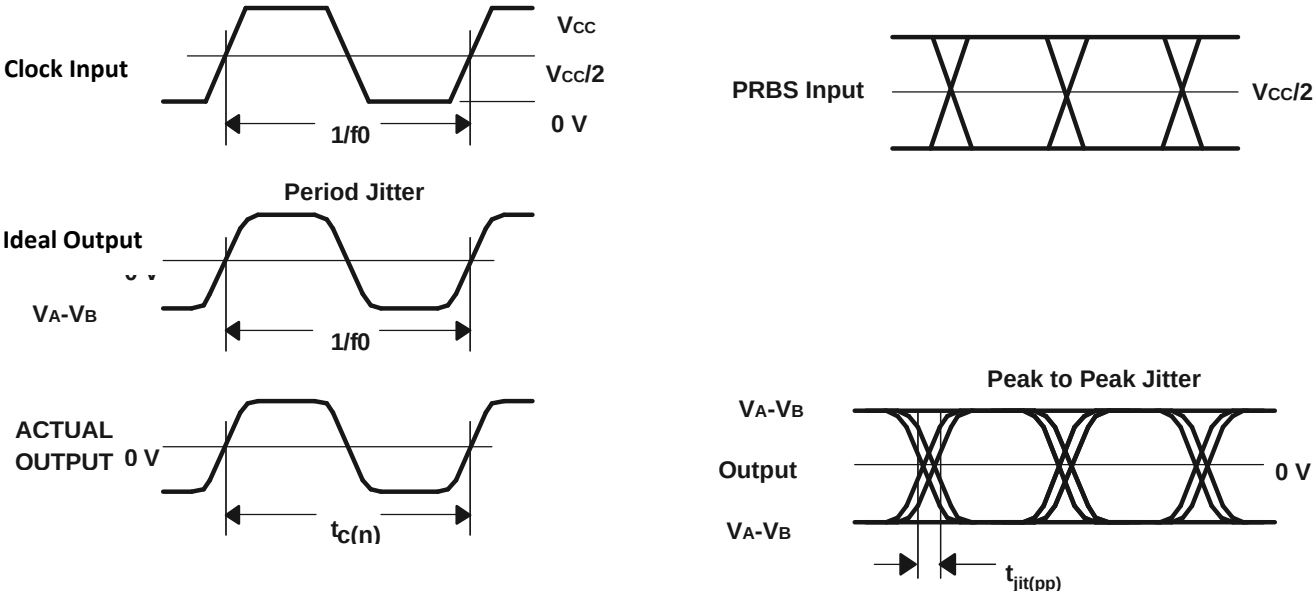


Figure 7. Driver Jitter Measurement Waveforms

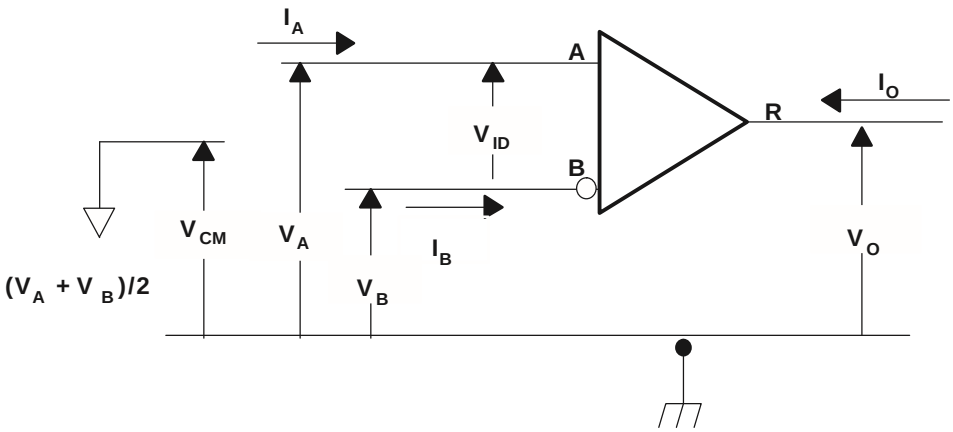


Figure 8. Receiver Voltage and Current Definitions

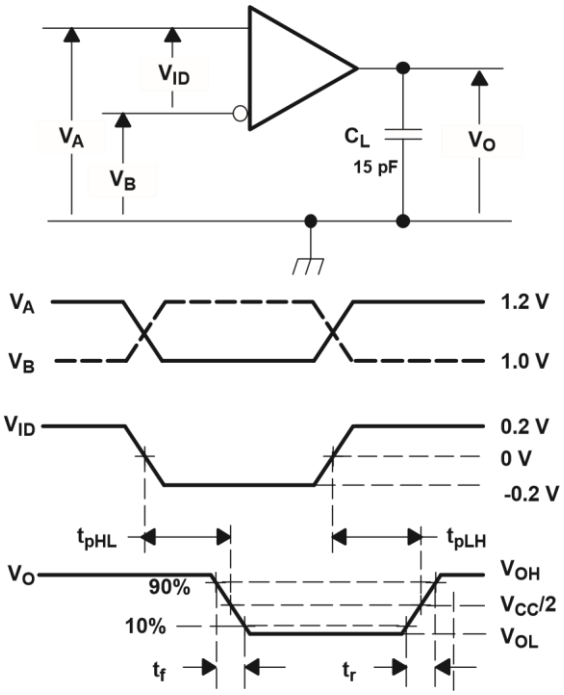


Figure 9. Receiver Timing Test Circuit and Waveforms

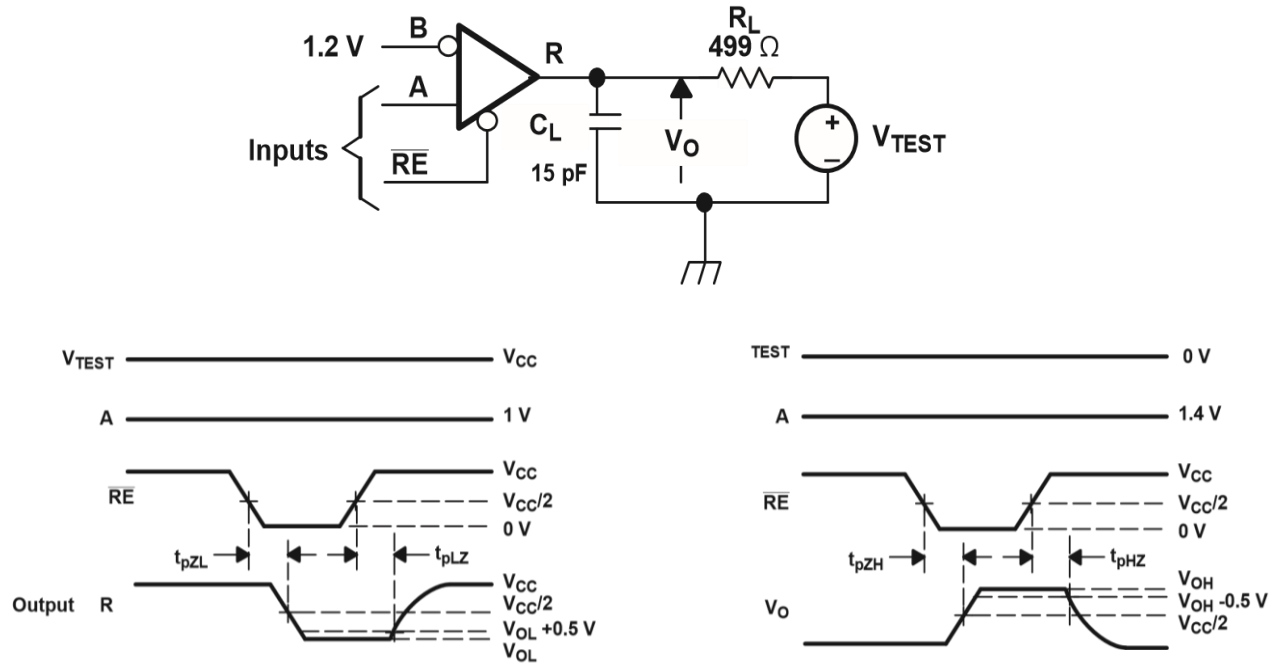


Figure 10. Receiver Enable/Disable Time Test Circuit and Waveforms

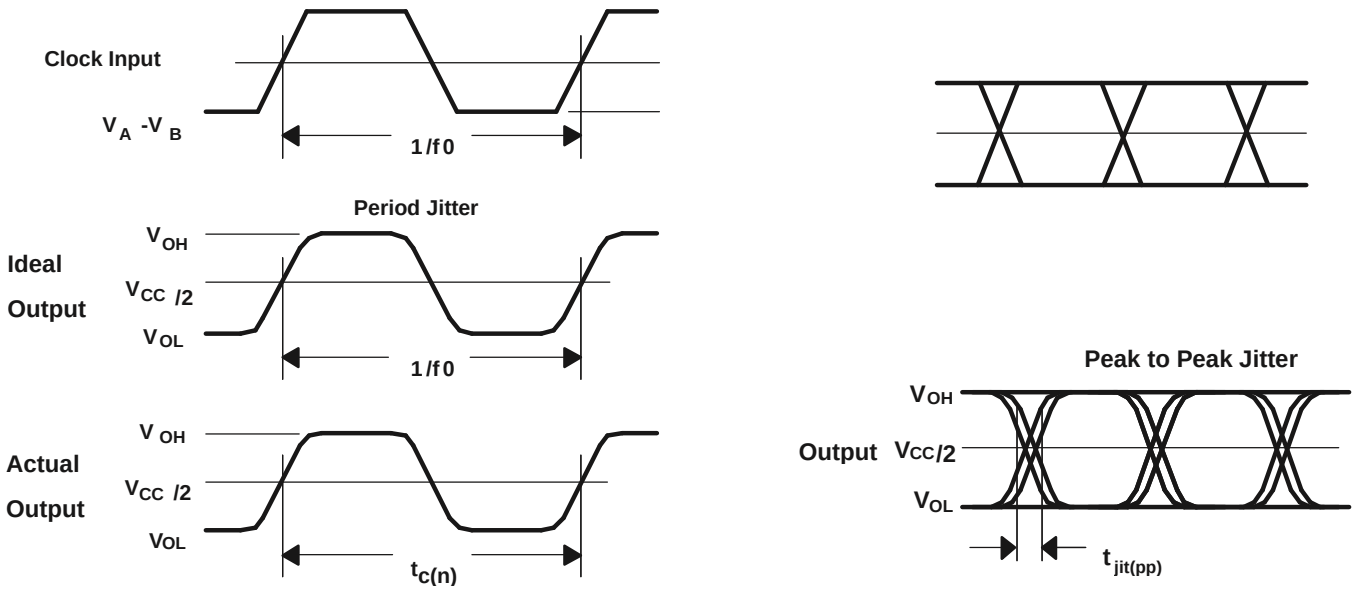
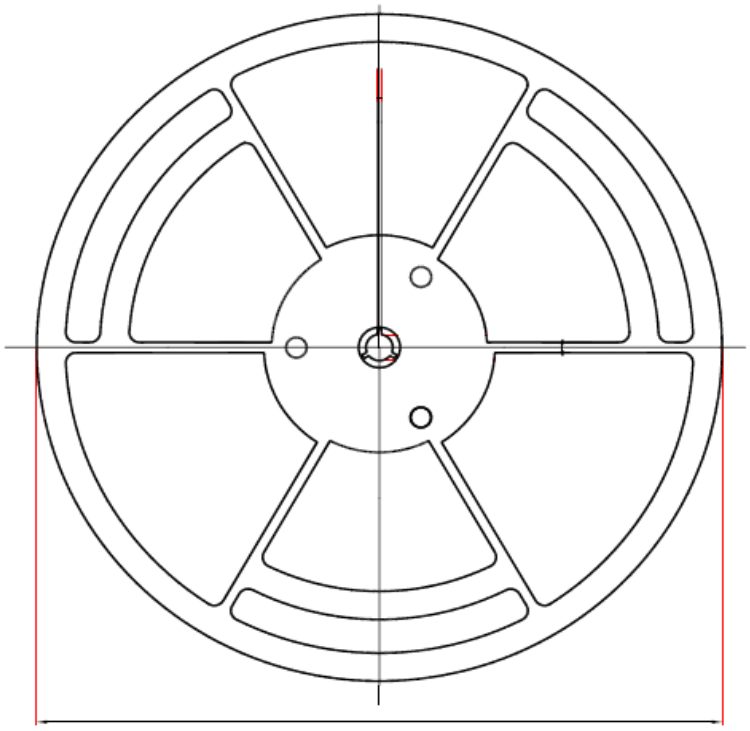
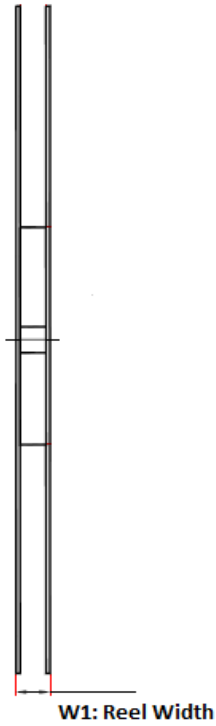
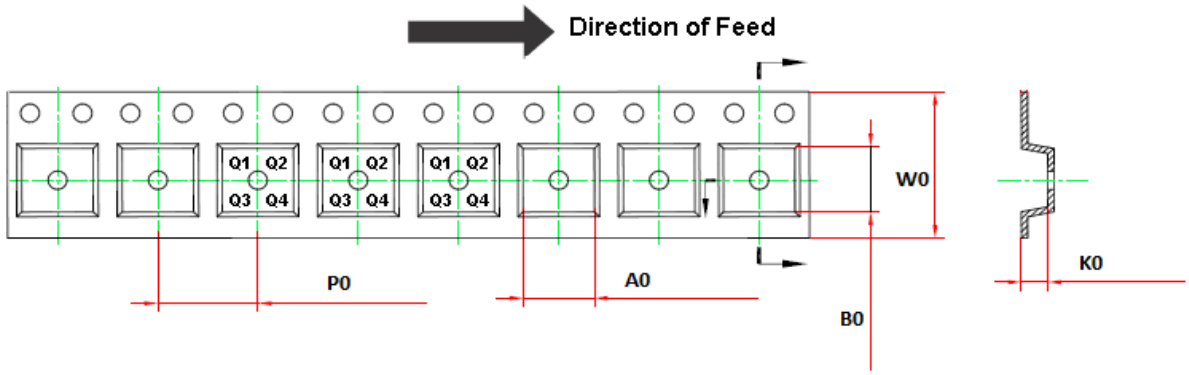


Figure 11. Receiver Jitter Measurement Waveforms

Tape and Reel Information





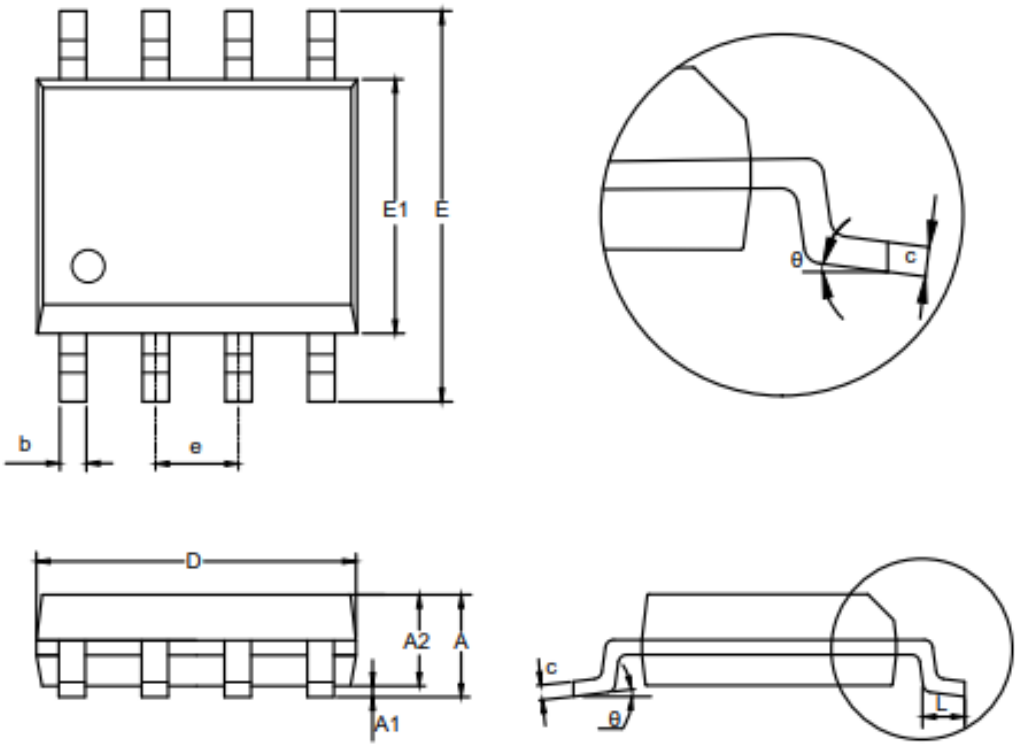


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT9H111L1-SO1R-S	8-Pin SOP	330.0	6.5	2.0	12.0	17.6	5.4	8.0	Q1

Package Outline Dimensions

SO1R (SOP8)

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT9H111L1-SO1R-S	−40 to 85°C	SOP-8	T9H111	MSL1	Tape and Reel, 4000	Green

(1) Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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