

MSKSEMI 美森科

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

TS5A3157DBVR-MS

Product specification

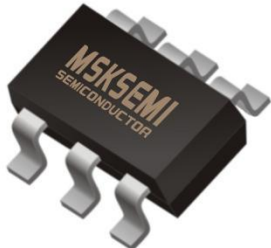
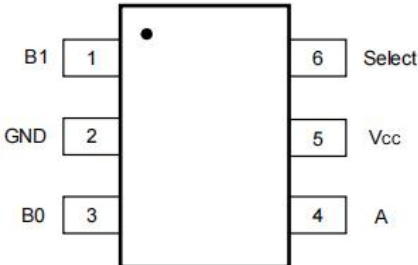

DESCRIPTION

The TS5A3157DBVR-MS is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power-supply range (from VCC to GND). The Select pin has over voltage protection that allows voltages above VCC, up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

FEATURES

- Low power dissipation
- High speed
- Standard CMOS logic levels
- High bandwidth, improved linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- be used for Clock Switching, Data Mux'ing, etc.
- Low R_{DS(on)}
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- Operating temperature -25 ~ +125
- package SOT-23-6

Reference News

SOT-23-6	Pin Configuration	MARKING
		

ORDER INFORMATION

P/N	PKG	QTY
TS5A3157DBVR-MS	SOT23-6	Tape and Reel, 3000

PIN DESCRIPTIONS

Pin	I/O	Pin Function
A, B0 , B1	I/O	Data port
Select	I	Controlling choice
VCC	/	Power supply port
GND	/	Ground

FUNCTIONS DESCRIPTION

Select input port	Function
L	B0 Connected to A
H	B1 Connected to A

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 ~ +7.0	V
DC Switch Voltage ⁽¹⁾	V_S	-0.5 ~ $V_{CC}+0.5$	V
DC Input Voltage ⁽¹⁾	V_{IN}	-0.5 ~ +7.0	V
DC Input Diode Current @ $V_{IN} < 0$ V	I_{IK}	-50	mA
DC Output Current	I_{out}	128	mA
DC V_{CC} or Ground Current	I_{CC}/I_{GND}	100	mA
Storage Temperature Range	T_{stg}	-65 ~ +150	°C
Junction Temperature Under Bias	T_J	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	T_L	260	°C
Power Dissipation @ +85°C	P_D	180	mW

NOTE:

Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. QCSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

QCSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS (2)

Characteristic		Symbol	Min	Max	Unit
Supply Voltage Operating		VCC	1.65	5.5	V
Select Input Voltage		VIN	0	VCC	V
Switch Input Voltage		VIN	0	VCC	V
Output Voltage		VOUT	0	VCC	V
Operating Temperature		TA	-55	+125	
Input Rise and Fall Time	Control Input VCC = 2.3 V ~ 3.6 V	tr,tf	0	10	ns/V
	Control Input VCC = 4.5 V ~ 5.5 V		0	5.0	

Note:

2. Select input must be held HIGH or LOW, it must not float.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	VCC	TA = 25C			TA = -40C ~ +85C		Unit
				Min	Typ	Max	Min	Max	
DC ELECTRICAL CHARACTERISTICS									
VIH	High Level Input Voltage		1.65 ~ 1.95				0.75Vcc		V
			2.3 ~ 2.8				1.5		
			3 ~ 4.2				2.4		
			4.5 ~ 5.5				0.6Vcc		
VIL	Low Level Input Voltage		1.65 ~ 1.95					0.25VCC	V
			2.3 ~ 2.8					0.4	
			3 ~ 5.5					0.3Vcc	
IIN	Input Leakage Current	0 < VIN < 5.5 V	0 ~ 5.5		±0.05	±0.1		±1	uA
IOFF	OFF State Leakage Current	0 < A, B < Vcc	1.65 ~ 5.5		±0.05	±0.1		±1	uA
ICC	Quiescent Supply	VIN = Vcc or GND IOUT = 0	5.5			1.0		10	uA
	Analog Signal Range		VCC	0		VCC	0	VCC	V
RON	Switch On Resistance ⁽³⁾	VIN = 0 V, IO = 30 mA	4.5		3.0			7.0	Ω
		VIN = 2.4 V, IO = -30 mA			5.0			12	Ω
		VIN = 4.5 V, IO = -30 mA			7.0			15	Ω
		VIN = 0 V, IO = 24 mA	3.0		4.0			9.0	Ω
		VIN = 3 V , IO = -24 mA			10			20	Ω
		VIN = 0 V, IO = 8 mA	2.3		5.0			12	Ω
		VIN = 2.3 V, IO = -8 mA			13			30	Ω
		VIN=0V, IO =4 mA			6.5			20	Ω
		VIN = 1.65 V, IO = -4 mA	1.65		17			50	Ω
RRANGE	On Resistance Over Signal Range ⁽³⁾⁽⁷⁾	IA = -30 mA 0 ≤ VBn ≤ VCC	4.5					25	Ω
		IA = -24 mA 0 ≤ VBn ≤ VCC	3					50	Ω

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	VCC	TA=25			TA = -40 ~ +85		Unit
				Min	Typ	Max	Min	Max	
RRANGE	On Resistance Over Signal Range(3)(7)	IA = -8 mA 0 ≤ VBn ≤ VCC	2.3					100	Ω
		IA = -4 mA 0 ≤ VBn ≤ VCC	1.65					300	Ω
Δ RON	On Resistance Match Between Channels(3)(4)(5)	IA = -30 mA VBn = 3.15	4.5		0.15				Ω
		IA = -24 mA VBn = 2.1	3		0.2				Ω
		IA = -8 mA VBn = 1.6	2.3		0.5				Ω
		IA = -4 mA VBn = 1.15	1.65		0.5				Ω
RFLAT	On Resistance Flatness(3)(4)(6)	IA = -30 mA 0 ≤ VBn ≤ VCC	5		6.0				Ω
		IA = -24 mA 0 ≤ VBn ≤ VCC	3.3		12				Ω
		IA = -8 mA 0 ≤ VBn ≤ VCC	2.5		28				Ω
		IA = -4 mA 0 ≤ VBn ≤ VCC	1.8		125				Ω

AC ELECTRICAL CHARACTERISTICS

tPHL tPLH	Propagation Delay Bus to Bus (8)	Figure 1 VI = OPEN	1.65 ~ 1.95						nS
			2.3 ~ 2.7					1.2	nS
			3.0 ~ 3.5					0.8	nS
			4.5 ~ 5.5					0.3	nS
tPZL tPZH	Output Enable Time, Turn On Time (A to Bn)	Figure 1 VI = 2*VCC for tPZL, VI = 0 V for tPZH	1.65 ~ 1.95			23	7.0	24	nS
			2.3 ~ 2.7			13	3.5	14	nS
			3.0 ~ 3.5			6.9	2.5	7.6	nS
			4.5 ~ 5.5			5.2	1.7	5.7	nS
tPLZ tPHZ	Output Disable Time, Turn Off Time (A Port to B Port)	Figure 1 VI = 2*VCC for tPLZ, VI = 0 V for tPHZ	1.65 ~ 1.95			12.5	3.0	13	nS
			2.3 ~ 2.7			7.0	2.0	7.5	nS
			3.0 ~ 3.5			5.0	1.5	5.3	nS
			4.5 ~ 5.5			3.5	0.8	3.8	nS

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions	VCC	TA = 25			TA = -40 ~ +85		Unit
					Min	Typ	Max	Min	Max	
tB-M	Break Before Make Time (7)		Figure2 , CL = 50 pF , RL = 600 Ω	1.65 ~ 1.95				0.5		nS
				2.3 ~ 2.7				0.5		nS
				3.0 ~ 3.5				0.5		nS
				4.5 ~ 5.5				0.5		nS
Q	(7) Charge Injection		Figure 3, CL = 0.1 nF , VGEN = 0 V , RGEN = 0 Ω	5.0		7.0				pC
				3.3		3.0				pC
OIRR	Off Isolation (9)		Figure 4, RL = 50 Ω , f = 10MHz	1.65 ~ 5.5		-57				dB
Xtalk	Crosstalk		Figure 5, RL = 50 Ω , f = 10MHz	1.65 ~ 5.5		-54				dB
BW	-3 dB Bandwidth		Figure 8, RL = 50 Ω	1.65 ~ 5.5		350M				Hz
THD	Total Harmonic Distortion (7)		RL = 600 Ω, 0.5VP-P f = 600 Hz ~ 20 kHz	5.0		0.011				%
CIN	Select Pin Input Capacitance (10)			0		2.3				pF
CIO-B	B Port Off Capacitance	(10)	Figure 6	5.0		5.0				pF
CIOA-ON	A Port Capacitance when Switch is Enabled (10)		Figure 7	5.0		15.5				pF

Note:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized but not tested in production.
5. $\Delta R_{ON} = R_{ON\ max} - R_{ON\ min}$ measured at identical VCC, temperature and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
7. Guaranteed by Design.
8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Off Isolation = $20 \log_{10} [V_A/V_{Bn}]$.
10. TA = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

TEST CIRCUITS

NOTE: Input driven by 50 Ω source terminated in 50 Ω
 NOTE: C_L includes load and stray capacitance
 NOTE: Input PRR = 1.0 MHz; t_W = 500 ns

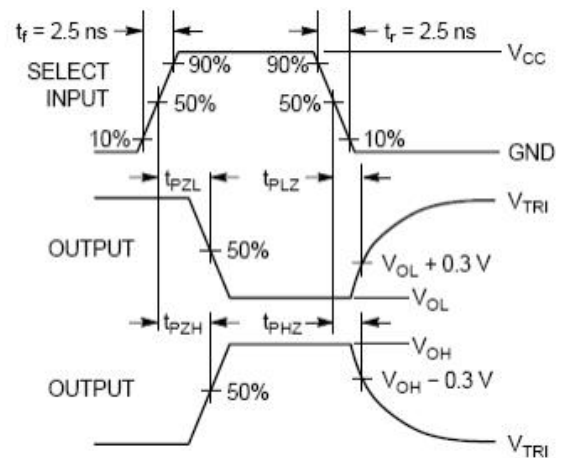
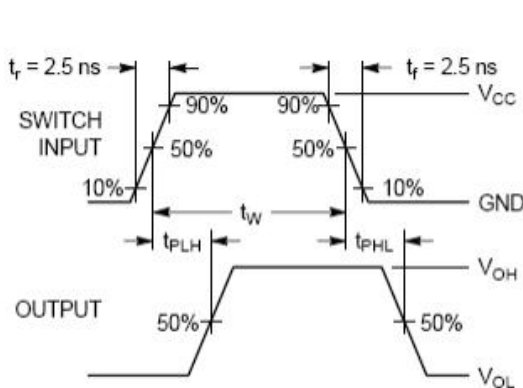
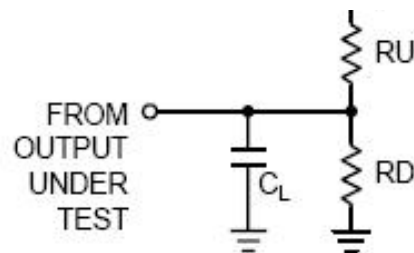


Figure 1. AC Test Circuit ,AC Waveforms

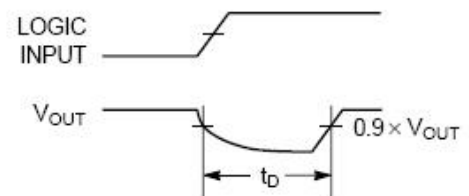
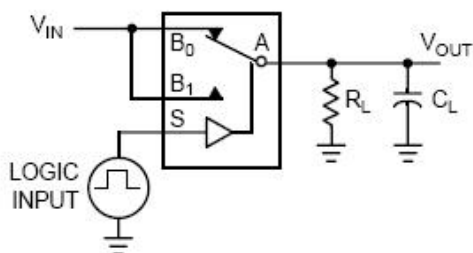
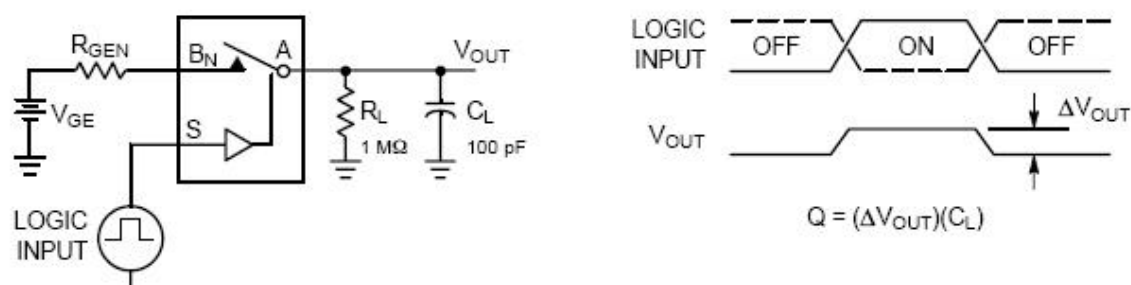
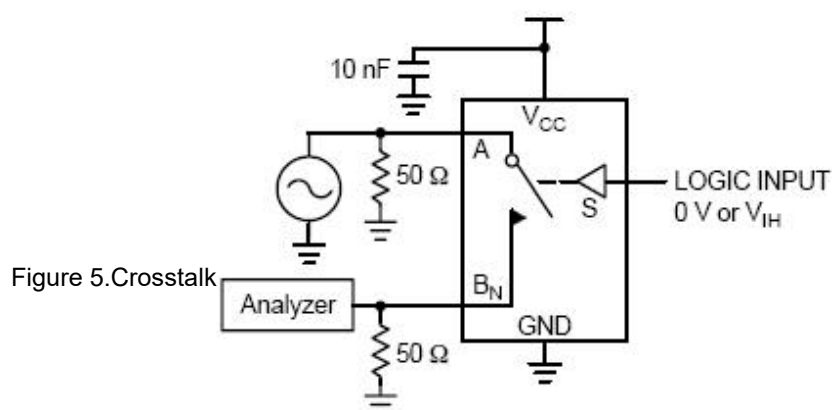
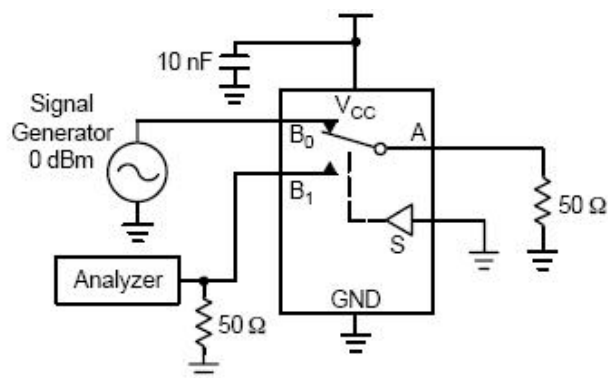
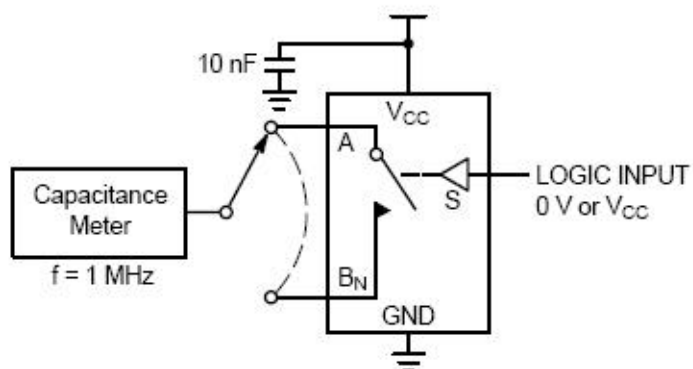


Figure 2. Break Before Make Interval Timing

TEST CIRCUITS (continued)

Figure 3. Charge Injection Test

Figure 4. Off Isolation

Figure 5. Crosstalk

Figure 6. Channel Off Capacitance

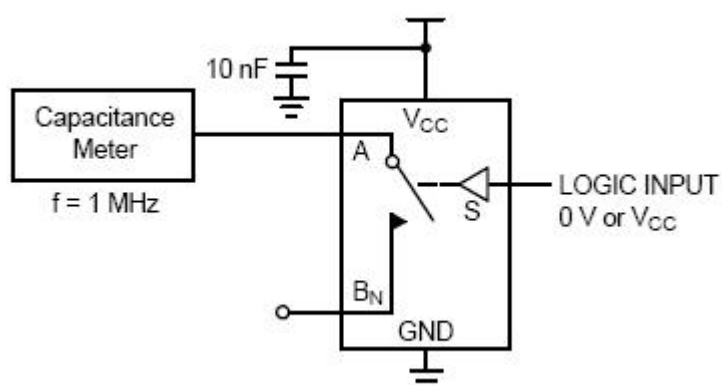


Figure 7. Channel On Capacitance

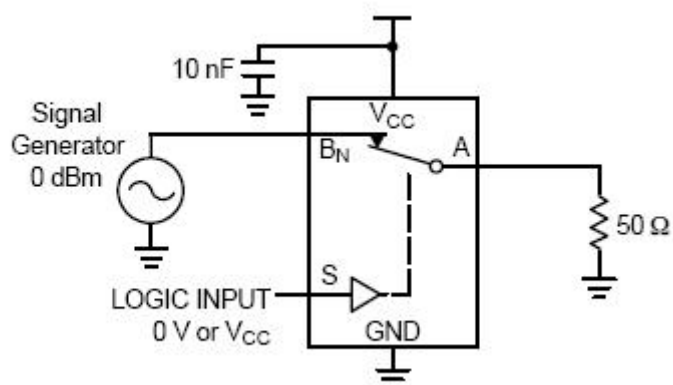
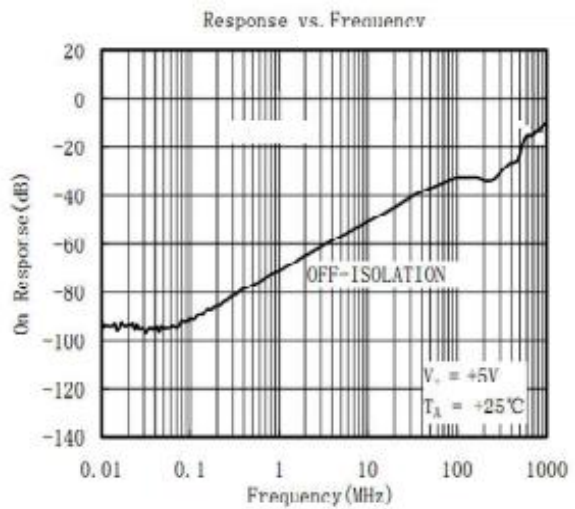
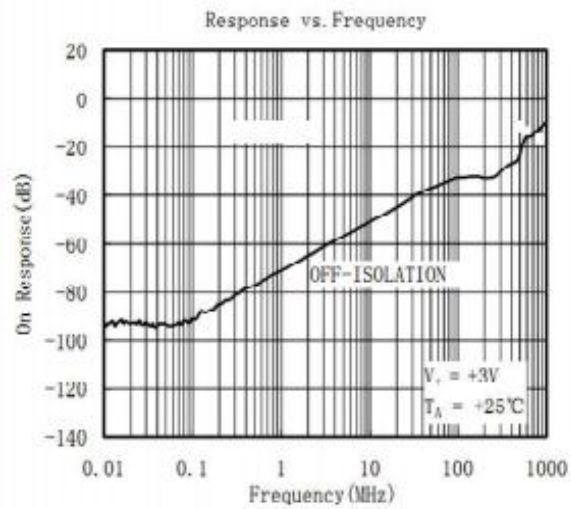
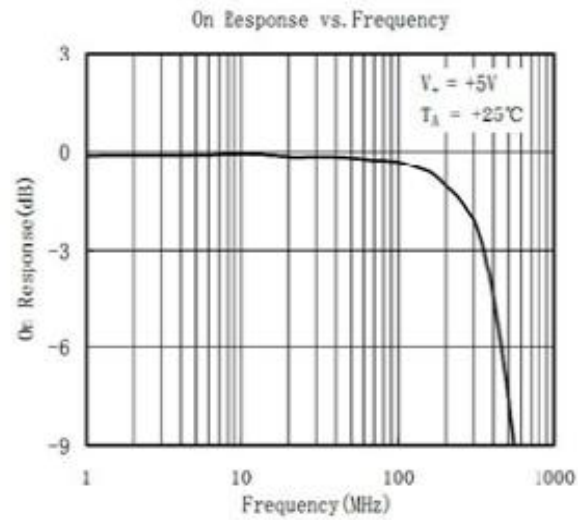
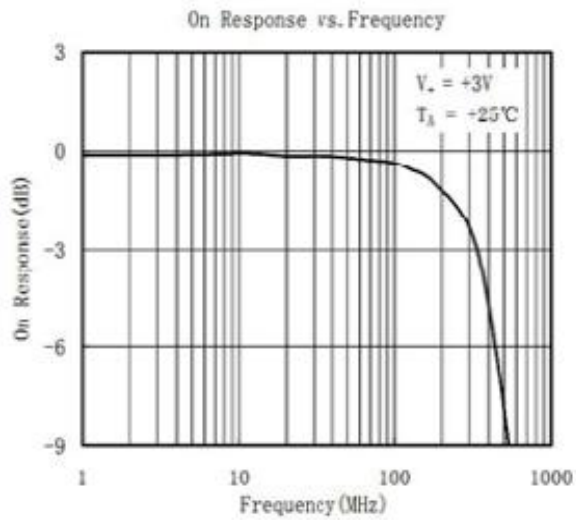
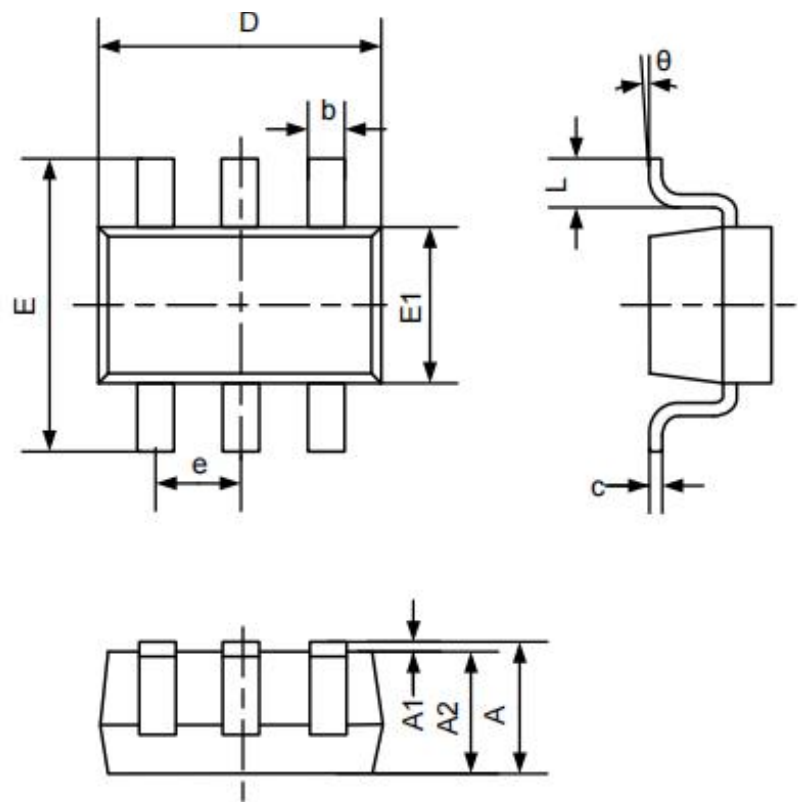


Figure 8. Bandwidth



PACKAGE OUTLINE

SOT-23-6



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A			1.240
A1	0.010	0.050	0.090
A2	1.050	1.100	1.150
b	0.300	0.350	0.400
c	0.117		0.157
D	2.870	2.920	2.970
E	2.720	2.800	2.880
E1	1.550	1.600	1.650
e	0.950BSC		
1	1.900BSC		
L	0.320	0.400	0.480
θ	0°		5°

Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specification of any and all MSKSEMI Semiconductor products described or contained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

■ MSKSEMI Semiconductor strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringement of intellectual property rights or other rights of third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the MSKSEMI Semiconductor product that you intend to use.