Low Power, Wide Input Range, Unity-Gain Difference Amplifiers

Features

- High Reliability:
  Input Protection to ±65 V (power on & off)
  Over Temperature Protection
- CMRR: 104 dB min
- CMRR Temperature Drift: 0.2 ppm/°C max
- High Precision:
  Input Offset Voltage: 100 µV max
  Input Offset Drift: 0.5 µV/°C
  Low Input Bias Current: 5 pA
  Gain Error: 15 ppm max
  Gain Error Temperature Drift: 0.3 ppm/°C max
- Wide Input Rang: 2 times of Supplies
- Bandwidth: 500 kHz
- Supply Current: 330 µA per channel
- Wide Power Supply Range: 2.7 V to 36 V
- Specified Temperature Range: -40 °C to +125 °C

Applications

- Li-Ion Battery Formation & Grading
- Precision Data Acquisition
- Communication Systems
- Sensor Signal Conditioning
- Industrial Control

Application Examples

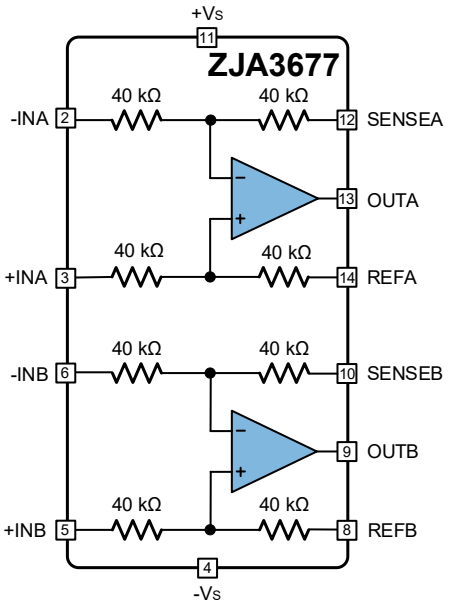

Figure 1. ZJA3677

General Description

The ZJA3676 and ZJA3677 are general-purpose, unity-gain difference amplifiers intended for precision signal conditioning in power critical applications that require both high performance and low power. They provide exceptional 104 dB common-mode rejection ratio (CMRR) and 500 kHz bandwidth while amplifying signals almost double the supply rails. They are trimmed for gain drift better than 0.3 ppm/°C and high CMRR.

Their unique design enables the ZJA3676 and ZJA3677 to with stand ±65 V during power-up and power-down, protecting the entire system. Additionally, on-chip over-temperature protection (OTP) ensures reliable operation under harsh environments.

The ZJA3676/7 operate on single supplies (2.7 V to 36 V) or dual supplies (±1.35 V to ±18 V). The quiescent supply current is 330 µA per channel, which is ideal for battery-operated and portable systems.

The ZJA3676 is available in 8-lead MSOP and SOIC packages, and the ZJA3677 is offered in a 14-lead SOIC package. Both are specified for performance over the temperature range of -40 °C to +125 °C and are fully RoHS and MSL-1 compliant.

ZJA3676 Product Family

Product	Gain	Number of Channels	Package
ZJA3676	1	1	SOIC/MSOP-8
ZJA3677	1	2	SOIC-14
ZJA3678	0.5, 2	1	SOIC/MSOP-8
ZJA3679	0.5, 2	2	SOIC-14

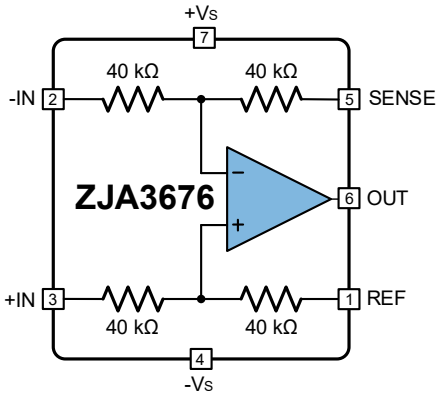

Figure 2. ZJA3676

Table of Contents

Version (Release A)[1]

Revision History

Dec. 2024——Release A

English version

Updated Figure 47/48, Ordering Guide, Orderable Device Explanation, Related Parts

Dec. 2023——Release A

Sep. 2023——Initial

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Pin Configurations and Function Descriptions

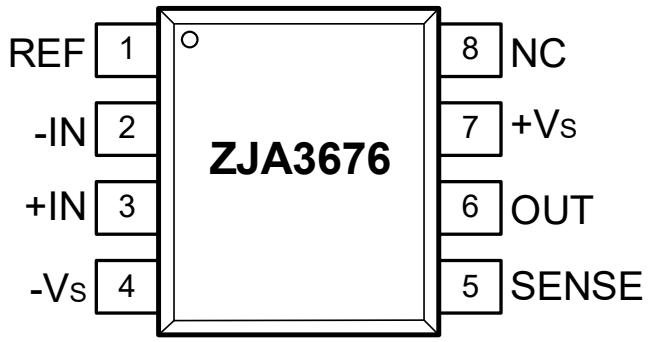


Figure 3. ZJA3676 Pin Configuration (8-lead SOIC)

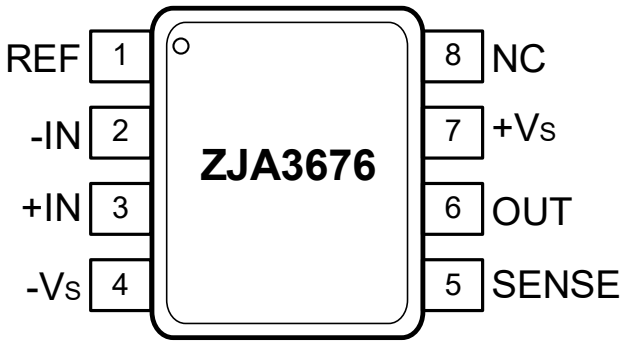


Figure 4. ZJA3676 Pin Configuration (8-lead MSOP)

Mnemonic	Pin No.	I/O[1]	Description
REF	1	AI	Reference voltage input
-IN	2	AI	Inverting input
+IN	3	AI	Non-inverting input
$-V_S$	4	P	Negative power supply
SENSE	5	AI	Sense terminal
OUT	6	AO	Output
$+V_S$	7	P	Positive power supply
NC	8	--	No Connect. This pin is not internally connected

[1] AI: Analog Input; P: Power; AO: Analog Output.

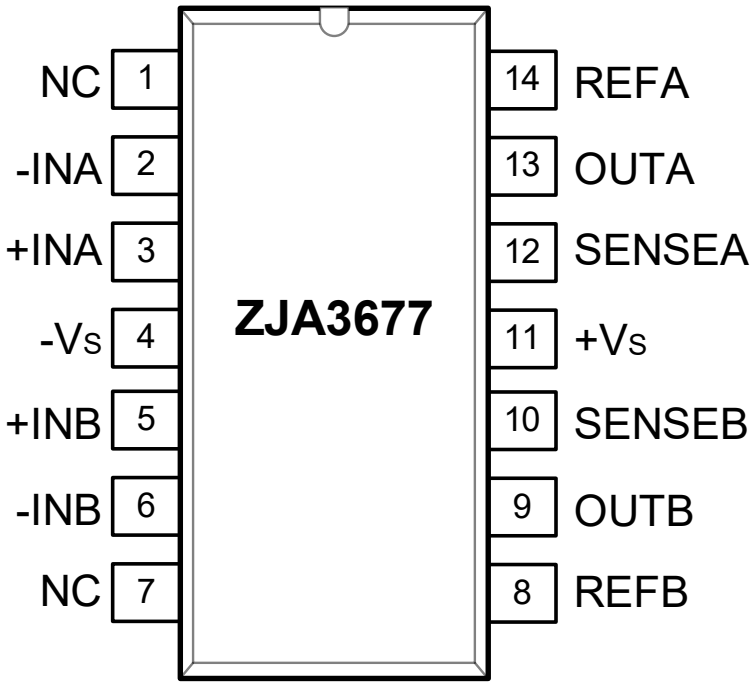


Figure 5. ZJA3677 Pin Configuration (14-lead SOIC)

Mnemonic	Pin No.	I/O[1]	Description
NC	1	--	No Connect. This pin is not internally connected
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
$-V_S$	4	P	Negative power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
NC	7	--	No Connect. This pin is not internally connected
REFB	8	AI	Channel B reference voltage input
OUTB	9	AO	Channel B output
SENSEB	10	AI	Channel B sense terminal
$+V_S$	11	P	Positive power supply
SENSEA	12	AI	Channel A sense terminal
OUTA	13	AO	Channel A output
REFA	14	AI	Channel A reference input

[1] AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Maximum Voltage at Any Input Pin	($-V_S$) + 65 V
Minimum Voltage at Any Input Pin	($-V_S$) - 65 V
Output Short-Circuit Duration to GND [2]	Continuous
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C
Maximum Reflow Temperature [3]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [4]	
Human Body Model (HBM) [5]	3.5 kV
Charged Device Model (CDM) [6]	2 kV

Thermal Resistance [7]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	158	43	°C/W
MSOP-8	190	44	°C/W
SOIC-14	120	36	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Limited by Over Temperature Protection (OTP).

[3] IPC/JEDEC J-STD-020Compliant

[4] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[5] ANSI/ESDA/JEDEC JS-001 Compliant

[6] ANSI/ESDA/JEDEC JS-002 Complaint

[7] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at T_A = 25 °C, V_S = ±15 V, V_{REF} = 0 V, R_L = 10 kΩ, G = 1, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
System Offset [1]	V_{OS}	B Grade			15	100	µV
		B Grade, -40 °C to 85 °C				200	µV
		B Grade	●			300	µV
		A Grade			30	150	µV
		A Grade, -40 °C to 85 °C				300	µV
		A Grade	●			500	µV
System Offset Drift	TCV_{OS}	B Grade, -40 °C to 85 °C			0.5	2	µV/°C
		B Grade	●			3	µV/°C
		A Grade, -40 °C to 85 °C			1.0	4	µV/°C
		A Grade	●			5	µV/°C
Power Supply	PSRR	V_S = ±2.25 V to ±18 V			0.1	0.6	µV/V
		V_S = ±2.25 V to ±18 V	●			1.1	µV/V
Common Mode Rejection Ratio	CMRR	V_S = ±15 V, V_{CM} = ±10 V, R_S = 0 Ω		104	124		dB
			●	96			dB
Common Mode Rejection Ratio Drift			●		0.03	0.2	ppm/°C
Input Operating Voltage Range [2]	IVR			-2 (V_S + 0.1)		+2 (V_S - 1.5)	V
Input Impedance [3]							
Differential Mode	R_{IN}				80		kΩ
Common Mode					40		kΩ
DYNAMIC PERFORMANCE							
Bandwidth					500		kHz
Slew Rate					1.0		V/µs
Settling Time	t_S	C_L = 100 pF, 0 to 10 V step, to 0.01 %			18		µs
		C_L = 100 pF, 0 to 10 V step, to 0.001 %			20		µs
Channel Separation		f = 1 kHz			140		dB

[1] Includes input bias and offset current errors, referred to output (RTO).
[2] The input voltage range can also be limited by the absolute maximum input voltage or by the output swing. See the Input Voltage Range section in the Theory of Operation section for details.
[3] Internal resistors are trimmed to be ratio matched and have ±10% absolute accuracy.

GAIN							
Gain Error					0.0002	0.0015	%
			•			0.0030	%
Gain Drift			•		0.04	0.3	ppm/°C
Gain Nonlinearity		V_{OUT} = 20 V_{P-P}				5	ppm
OUTPUT CHARACTERISTICS							
Output Voltage Swing [4]		R_L = 10 kΩ	•	(-V_S) + 0.2		(+V_S) - 0.2	V
Short-Circuit Current	I_{SC}	Source			28		mA
		Sink			-15		mA
Capacitive Load Drive					200		pF
NOISE [5]							
Voltage Noise	$e_{n,p-p}$	f = 0.1 Hz to 10 Hz			2.5		μV_{P-P}
Voltage Noise Density	e_n	f = 1 kHz			65		nV/$\sqrt{Hz}$
POWER SUPPLY							
Supply Current [6]					330	360	µA
			•			370	µA
Operating Voltage Range [7]				±1.35		±18	V
TEMPERATURE RANGE							
		Specified Temperature Range		-40		+125	°C

[4] Output voltage swing varies with supply voltage and temperature.
[5] Includes amplifier voltage and current noise, as well as noise from internal resistors.
[6] Supply current varies with supply voltage and temperature.
[7] Unbalanced dual supplies can be used, such as -V_S = -0.5 V and +V_S = +2 V. The positive supply rail must be at least 2 V above the negative supply and reference voltage.

Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_S = ±15 V, R_L = 10 kΩ, G = 1.

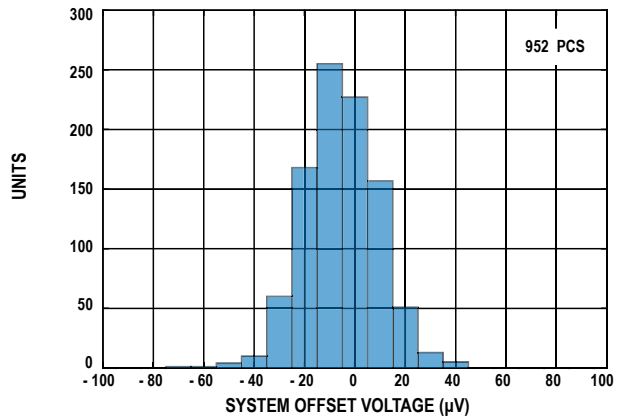


Figure 6. Distribution of System Offset Voltage

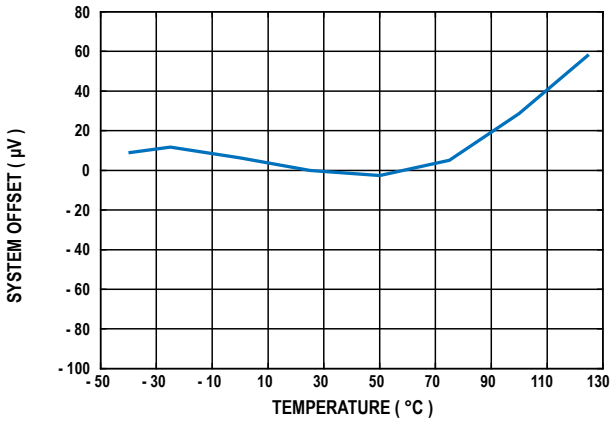


Figure 7. System Offset vs. Temperature, Normalized at 25 °C

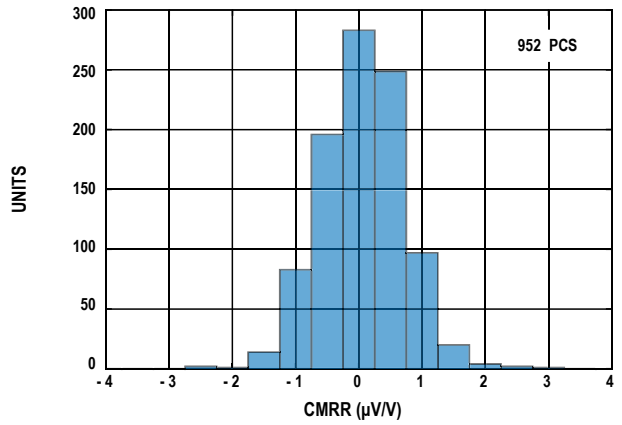


Figure 8. Distribution of Common-Mode Rejection Ratio (CMRR)

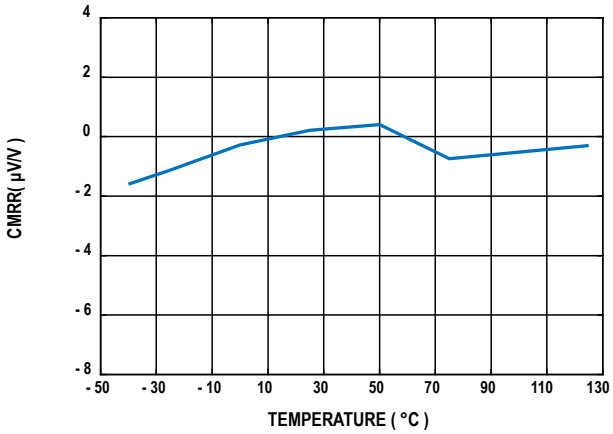


Figure 9. CMRR vs. Temperature

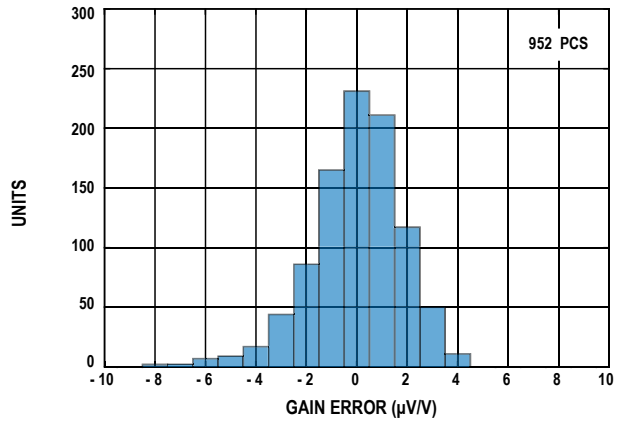


Figure 10. Distribution of Gain Error

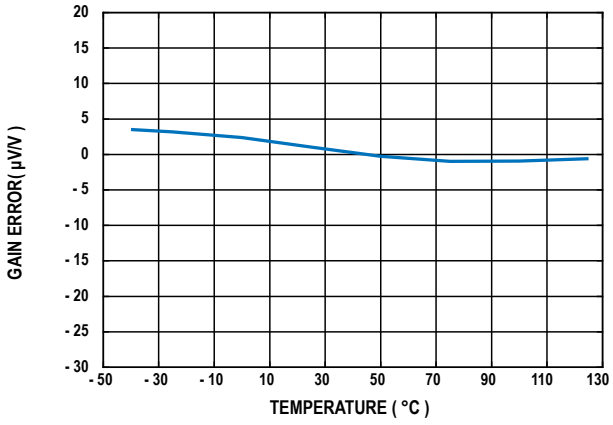


Figure 11. Gain Error vs. Temperature

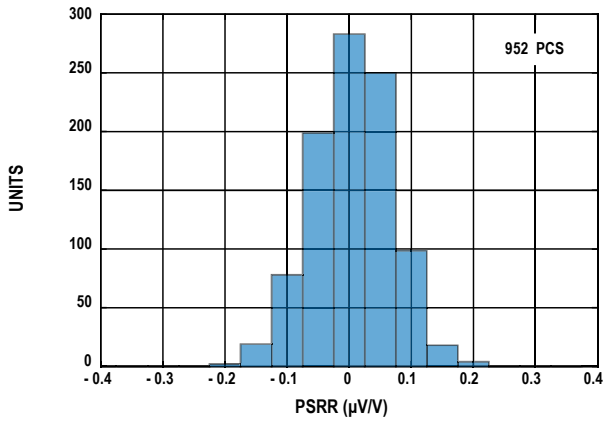


Figure 12. Distribution of PSSR

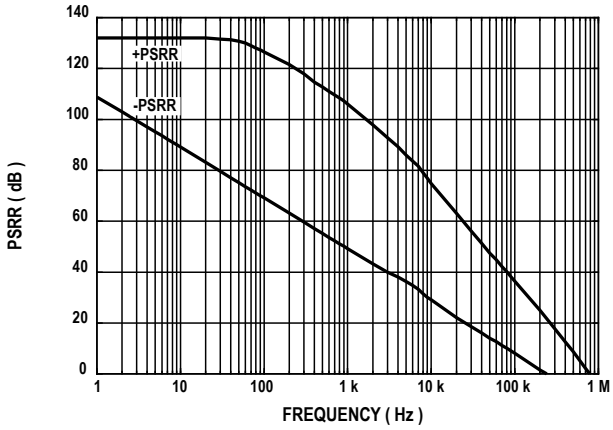


Figure 13. Power Supply Rejection Ratio (PSRR) vs. Frequency

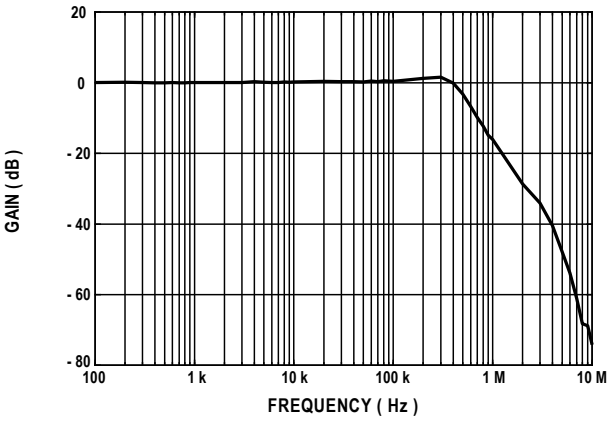


Figure 14. Gain vs. Frequency

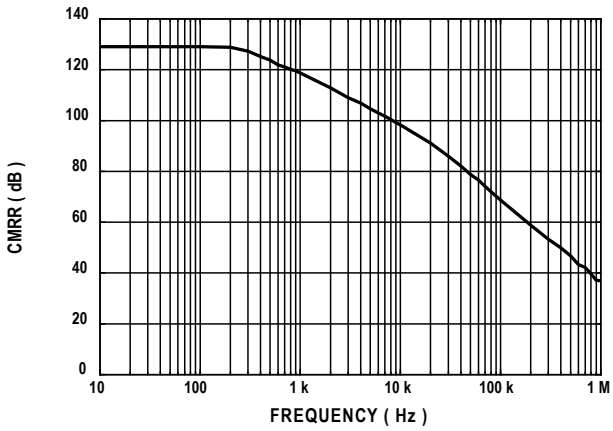


Figure 15. Common Mode Rejection Ratio (CMRR) vs. Frequency

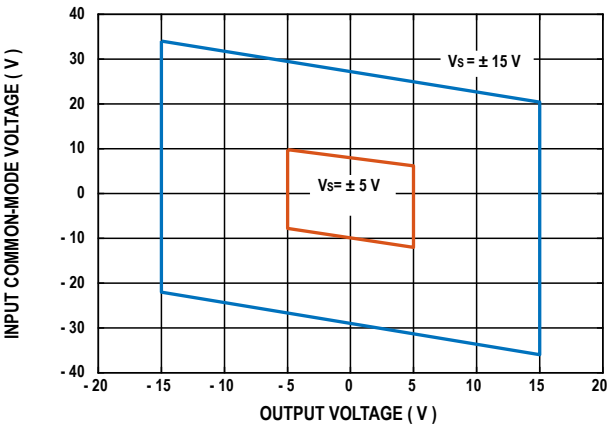


Figure 16. Input Common-Mode Voltage vs. Output Voltage (±15 V and ±5 V Supplies)

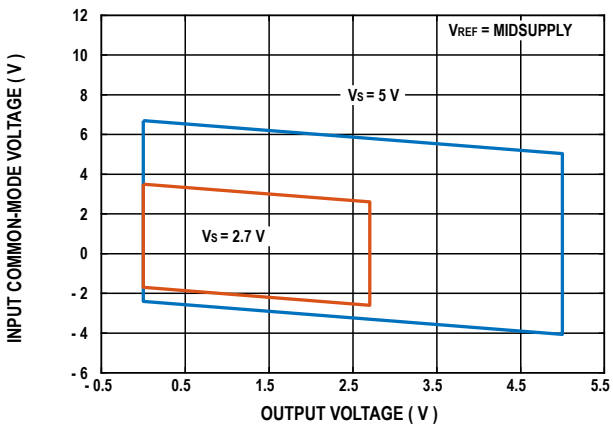


Figure 17. Input Common-Mode Voltage vs. Output Voltage (5 V and 2.7 V Supplies, V_{REF} = Midsupply)

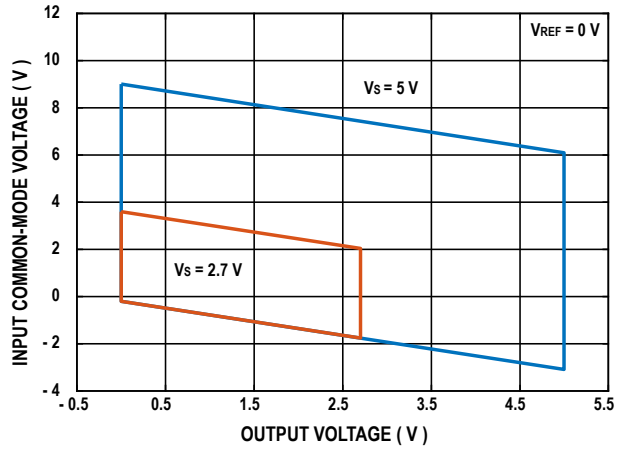


Figure 18. Input Common-Mode Voltage vs. Output Voltage (5 V and 2.7 V Supplies, V_{REF} = 0 V)

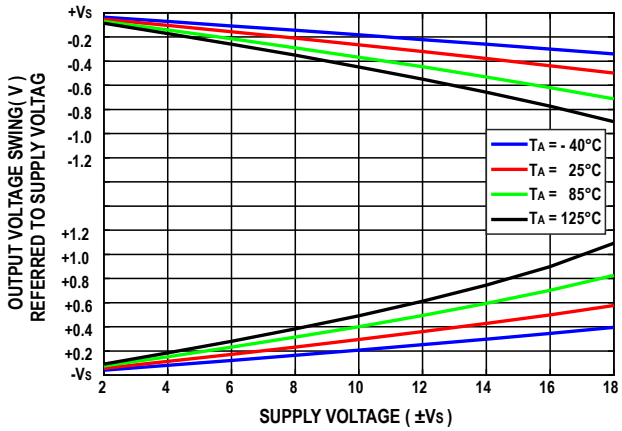


Figure 19. Output Voltage Swing vs. Supply Voltage and Temperature (R_L = 2 kΩ)

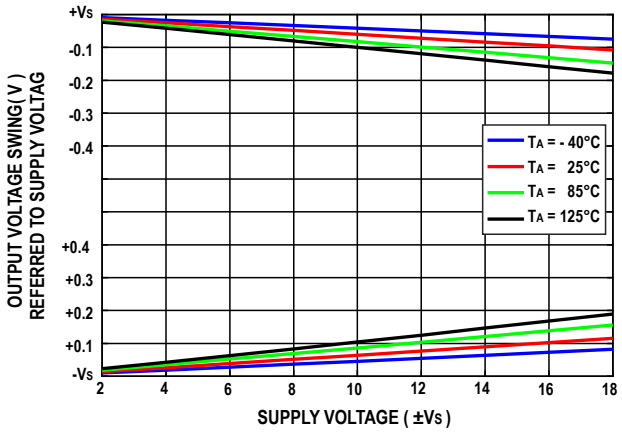


Figure 20. Output Voltage Swing vs. Supply Voltage and Temperature (R_L = 10 kΩ)

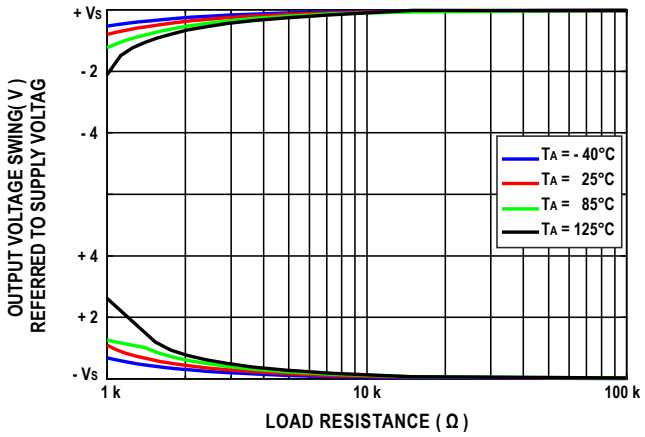


Figure 21. Output Voltage Swing vs. Load Resistance and Temperature (V_S = ±15 V)

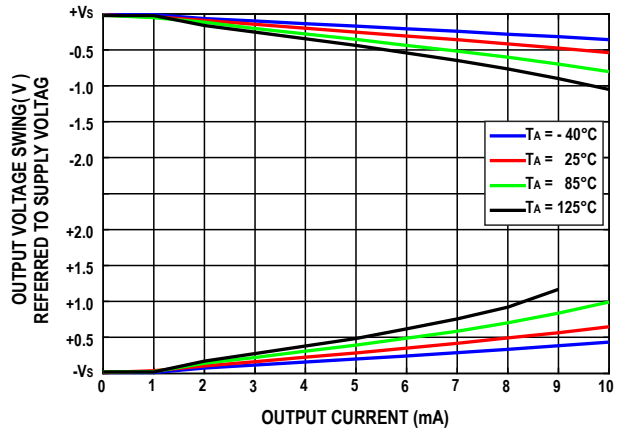


Figure 22. Output Voltage Swing vs. Output Current and Temperature (V_S = ±15 V)

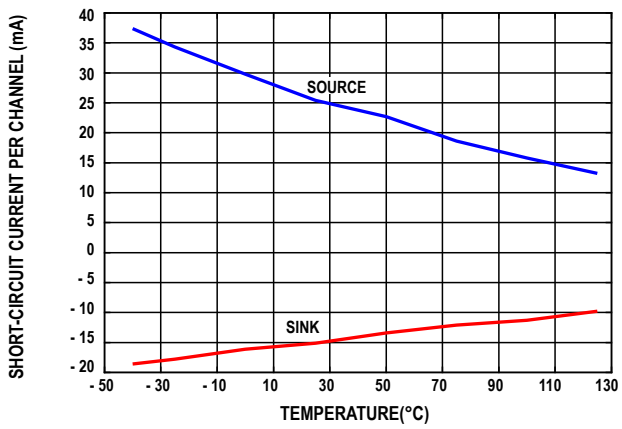


Figure 23. Short-Circuit Currentper Channel vs. Temperature

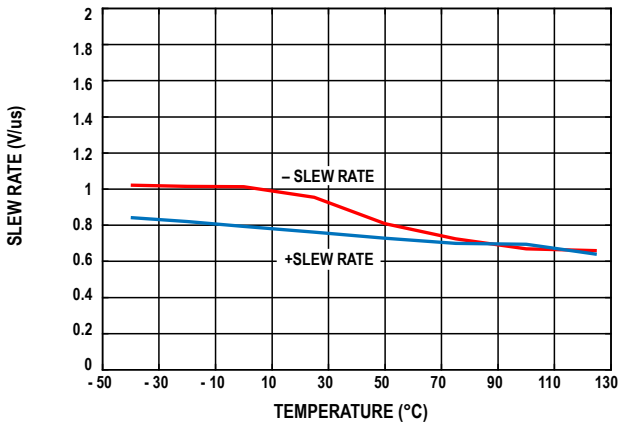


Figure 24. Slew Rate vs. Temperature (VIN = 20 V_{P-P}, 1 kHz)

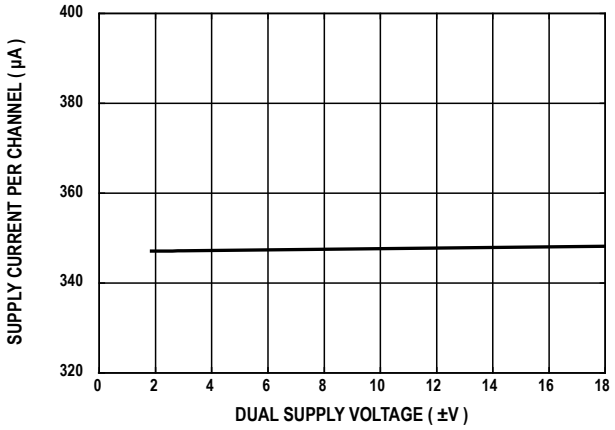


Figure 25. Supply Currentper Channel vs. Dual Supply Voltge (VIN = 0 V)

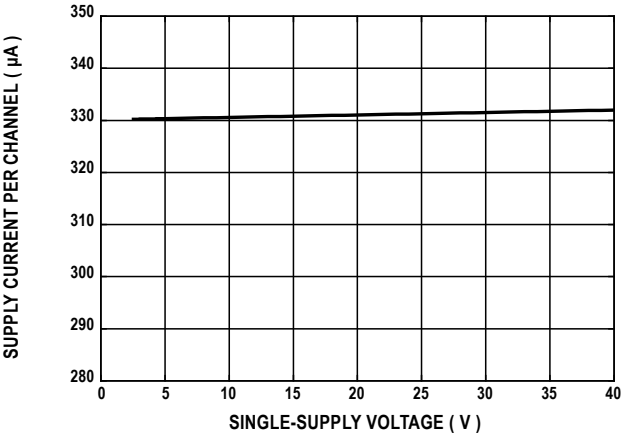


Figure 26. Supply Currentper Channel vs. Single Supply Voltge (VIN = 0 V, V_{REF} = 0 V)

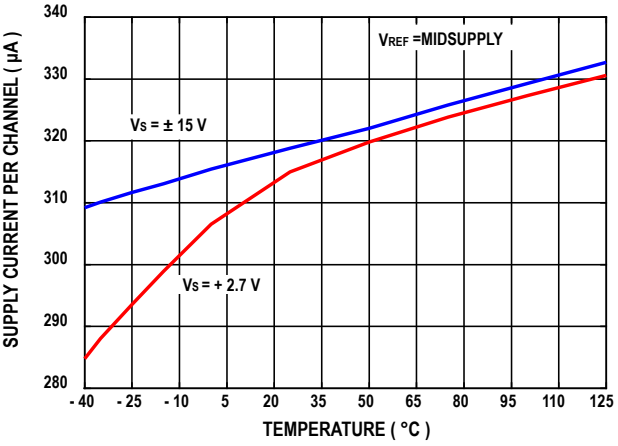


Figure 27. Supply Currentper Channel vs.Temperature

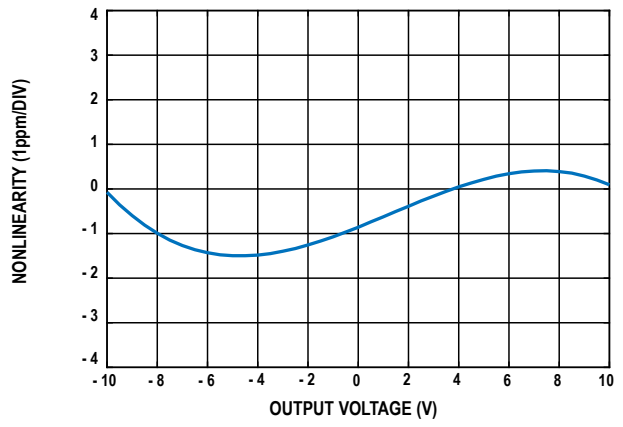


Figure 28. Gain Nonlinearity (V_S = ±15 V, R_L ≥ 2 kΩ)

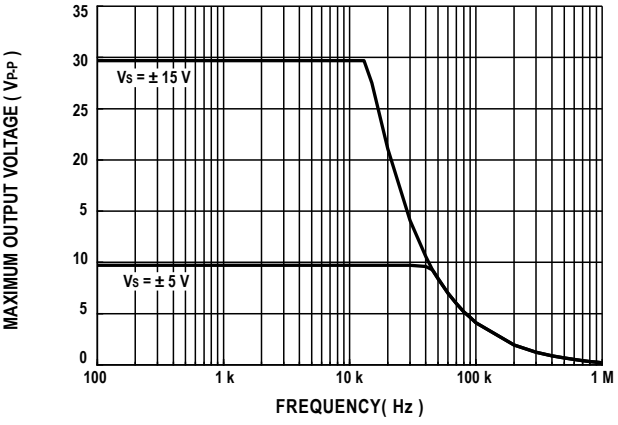


Figure 29. Maxmum Output Voltage vs. Frequency (V_S = ±15 V, ±5 V)

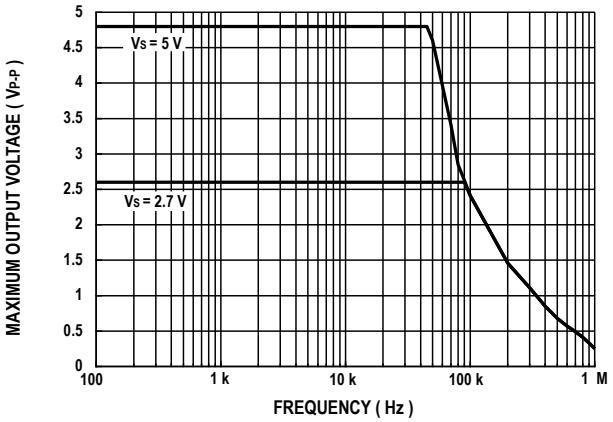


Figure 30. Maxmum Output Voltage vs. Frequency (V_S = 5 V, 2.7 V)

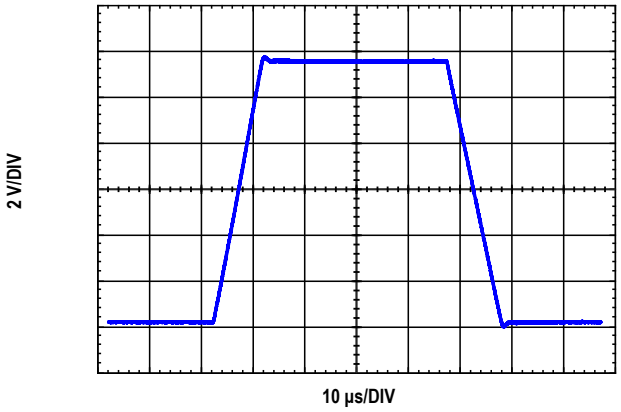


Figure 31. Large Signal Step Response

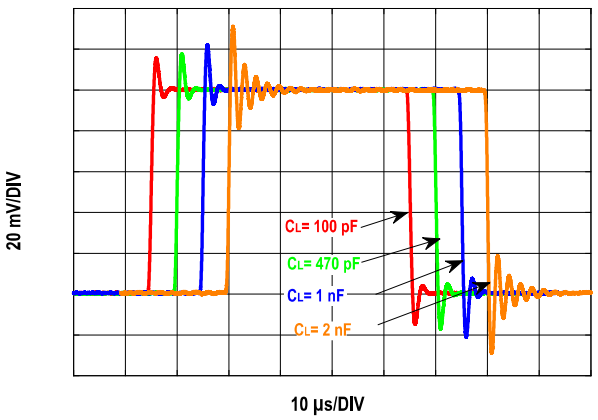


Figure 32. Small Signal Step Response for Various Capacitive Loads

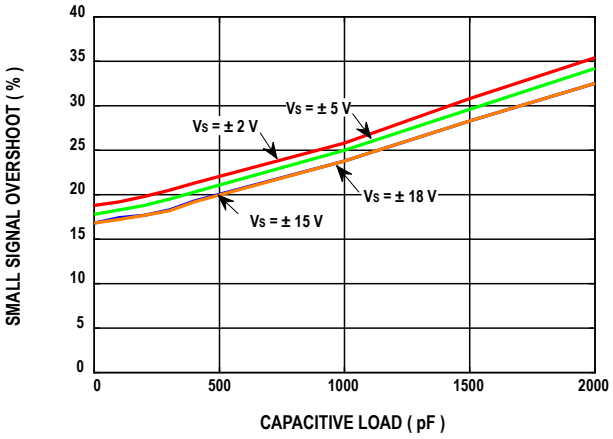


Figure 33. Small Signal Overshoot vs. Capacitive Load(R_L ≥ 2 kΩ)

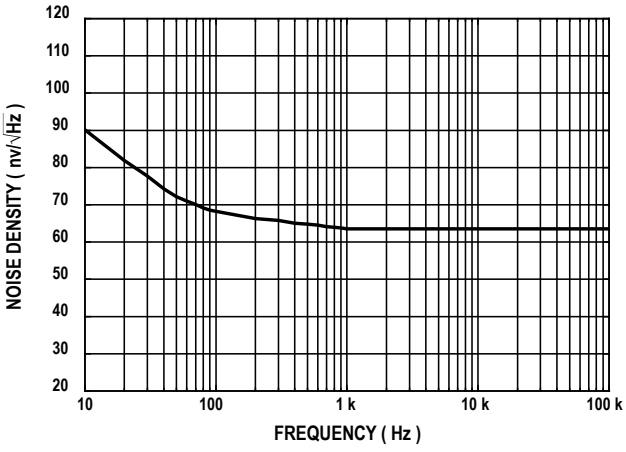


Figure 34. Voltage Noise Density vs. Frequency

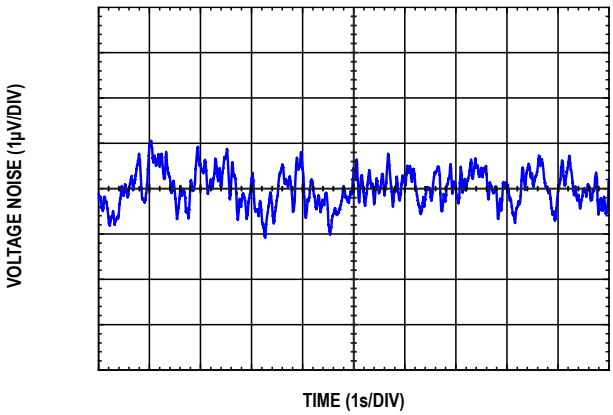


Figure 35. 0.1 Hz to 10 Hz Voltage Noise

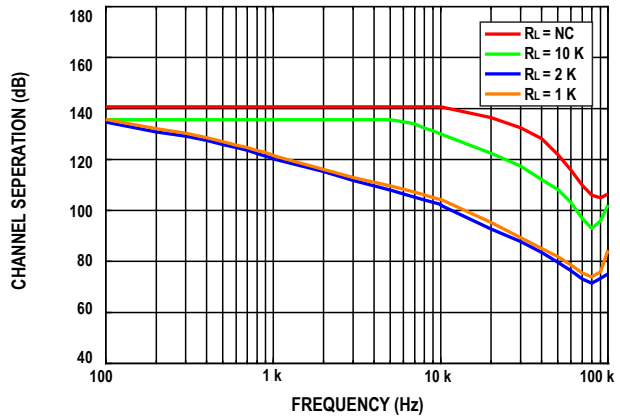


Figure 36. Channel Separation vs. Frequency

Theory of Operation

Circuit Information

Each channel of the ZJA3676 and ZJA3677 consists of a low power, low noise op amp and four trimmed (ZHIJINGTRIM®) on-chip resistors (See Figure 1 and Figure 2). These resistors can be externally connected to make a variety of amplifier configurations, including difference, noninverting, and inverting configurations. Taking advantage of the integrated resistors of the ZJA3676/ZJA3677 provides the designer with several benefits over a discrete design, including smaller size, lower cost, and improved ac and dc performance. The ZJA3676 and ZJA3677 offer temperature characteristics that are difficult to achieve using discrete components. Even if achievable, the cost of using discrete components would likely be significantly higher.

DC Performance

Much of the dc performance of op amp circuits depends on the accuracy of the surrounding resistors. As is shown in Figure 37, the output voltage is found to be

$$V_{OUT} = V_{+IN}\left(\frac{R_2}{R_1+R_2}\right)\left(1+\frac{R_4}{R_3}\right) - V_{-IN}\left(\frac{R_4}{R_3}\right)$$

$$= (V_{+IN}-V_{-IN})\left(\frac{R_4}{R_3}\right)\left[1+\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{2\left(1+\frac{R_1}{R_2}\right)}\right] + \left(\frac{V_{+IN}+V_{-IN}}{2}\right)\left(\frac{R_4}{R_3}\right)\left(\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\right)$$

$$= V_D \cdot G \cdot \left[1+\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{2(1+G^{-1})}\right] + V_{CM}\cdot G\cdot\left(\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{1+G^{-1}}\right), G=\frac{R_4}{R_3},\ V_D = V_{+IN}-V_{-IN},\ V_{CM}=\frac{V_{+IN}+V_{-IN}}{2}$$

$$= V_D \cdot \left(1+\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{2}\right) + V_{CM}\cdot\left(\frac{\frac{R_3}{R_4}-\frac{R_1}{R_2}}{2}\right), G = 1\ for\ ZJA3676/ZJA3677$$

This equation demonstrates that the gain accuracy and CMRR of the ZJA3676/ZJA3677 is determined primarily by the matching of resistor ratios (R_3 / R_4 - R_1 / R_2) / 2. Even a 0.1 % mismatch in one resistor degrades the CMRR to 1 / (0.1% / 2), which is 66 dB, for a G = 1 difference amplifier. as long as the following ratio of the resistors is tightly matched:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

The difference amplifier output voltage equation can be reduced to

$$\boldsymbol{V_{OUT} = \frac{R_4}{R_3}\cdot(V_{+IN}-V_{-IN})}$$

The resistors on the ZJA3676/ZJA3677 are trimmed to match accurately. As a result, the ZJA3676/ZJA3677 provide superior performance over a discrete solution, enabling higher CMRR (96 dB min over specified temperature range), higher gain accuracy (better than 15 ppm at room temperature), and lower gain drift (0.3 ppm/°C max), even over specified temperature range of -40 °C to 125 °C.

AC Performance

Component sizes and trace lengths are much smaller in an IC than on a PCB, therefore, the corresponding parasitic elements are also smaller, which results in improved ac performance of the ZJA3676/ZJA3677. For example, the positive and negative input terminals of the ZJA3676/ZJA3677 op amps are intentionally not pinned out, meaning that there is no direct connection to the inputs of the amplifier. The op amps are connected internally through the resistors, and there is no direct access to the pins. By not connecting these nodes to the traces on the PCB, the capacitance remains low, resulting in improved loop stability and excellent CMRR over frequency of 104 dB.

Driving ZJA3676/ZJA3677

Care must be taken to drive the ZJA3676/ZJA3677 with a low impedance source in order to avoid significantly degrading the gain accuracy and CMRR. Because all configurations present several kilohms of input resistance, the ZJA3676/ZJA3677 do not require a high current drive from the source and therefore are easy to drive. See Figure 39.

Input Voltage Range

The ZJA3676/ZJA3677 are able to measure input voltages beyond the supply rails. The internal resistors divide down the voltage before it reaches the internal op amp and provide protection to the op amp inputs. Figure 37 shows an example of how the voltage division works in a difference amplifier configuration. For the ZJA3676/ZJA3677 to measure correctly, the input voltages at the input nodes of the internal op amp must stay below 1.5 V, which is (+Vs) - 1.5 V, of the positive supply rail and can exceed the negative supply rail by 0.1 V, which is (-Vs) + 0.1 V. Refer to the Power Supplies section for more details.

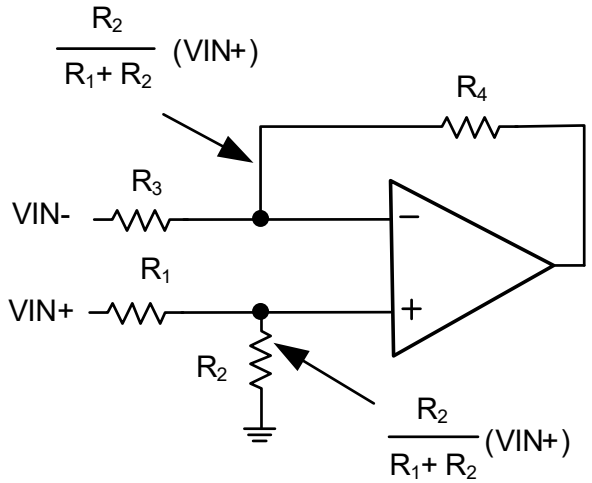


Figure 37. Voltage Division in the Difference Amplifier Configuration

The ZJA3676/ZJA3677 have integrated ESD diodes at the inputs that provide overvoltage protection. This feature simplifies system design by eliminating the need for additional external protection circuitry, and lower the parasitic parameters. The voltages at any of the inputs of the devices can safely range from ($-V_S$) - 65 V to ($-V_S$) + 65 V. For example, on ±10 V supplies, input voltages can go as high as -75 V to +55 V. Care must be taken to not exceed the ($-V_S$) - 65 V to ($-V_S$) + 65 V input limits to avoid risking damage to the devices.

Power Supplies

The ZJA3676/ZJA3677 operate over a wide range of supply voltages. They can operate on a single supply as low as 2.7 V and as high as 36 V, under appropriate setup conditions. For optimal performance, the user must ensure that the internal op amp is biased correctly through proper setup conditions. The internal input terminals of the op amp must have sufficient voltage headroom to operate properly. Proper operation of the device requires at least 1.5 V between the positive supply rail and the op amp input terminals. As shown in Figure 38, this relationship is expressed in the following equation:

$$\frac{R_1}{R_1 + R_2} \cdot V_{REF} < +V_S - 1.5\ V$$

For example, when operating on ±Vs = ±2 V dual supplies and V_{REF} = 0 V, it can be seen from Figure 38 that the input terminals of the op amp are biased at 0 V, allowing more than the required 1.5 V headroom. However, if V_{REF} = 1 V under the same conditions, the input terminals of the op amp are biased at 0.5 V, barely allowing the required 1.5 V headroom. This setup does not allow any practical voltage swing on the noninverting input. Therefore, the user must increase the supply voltage or decrease V_{REF} to restore proper operation.

The ZJA3676/ZJA3677 are typically specified at single and dual supplies, but they can be used with unbalanced supplies, as well, for example, $-V_S$ = -5 V, $+V_S$ = 20 V. The difference between the two supplies must be kept below 36 V and at least 2.7 V.

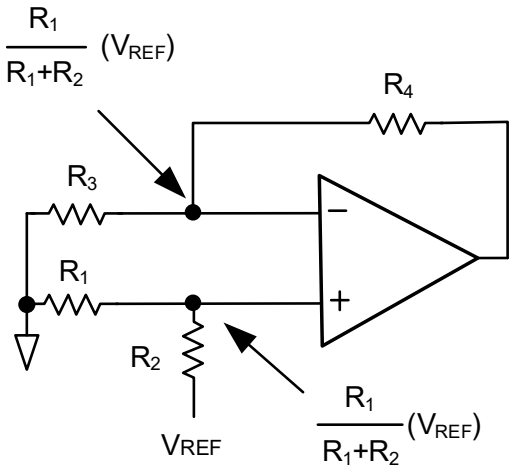


Figure 38. Ensure Sufficient Voltage Headroom on the Internal Op Amp Inputs

Use a stable dc voltage to power the ZJA3676/ZJA3677. Noise on the supply pins can adversely affect performance. Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close as possible to each supply pin. Use a tantalum capacitor of 10 µF between each supply and ground. The tantalum capacitor can be farther away from the supply pins and, typically, other precision integrated circuits can share the capacitor. Refer to Layout Example session for details.

Applications and Implementation

Configurations

The ZJA3676/ZJA3677 can be configured in several ways (see Figure 40 to Figure 44). Note that Figure 41 shows the ZJA3676/ZJA3677 as difference amplifiers with a midsupply reference voltage at the noninverting input, allowing the ZJA3676/ZJA3677 to be used as a level shifter, which is appropriate in single-supply applications that are referenced to midsupply. As with the other inputs, the reference must be driven with a low impedance source to maintain the internal resistor ratio. An example using the low power, low noise ZJA3007-1 as a reference is shown in Figure 39.

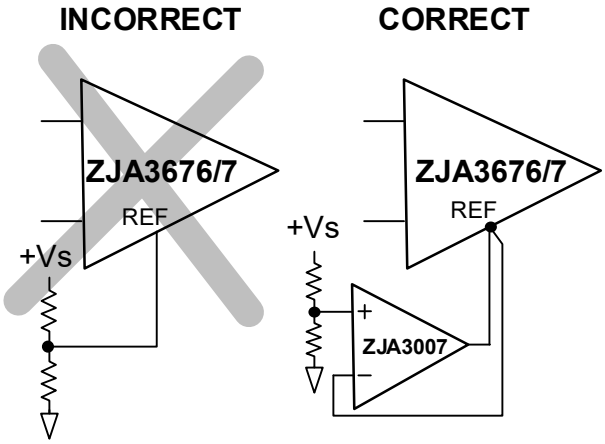


Figure 39. Driving the REF Pin

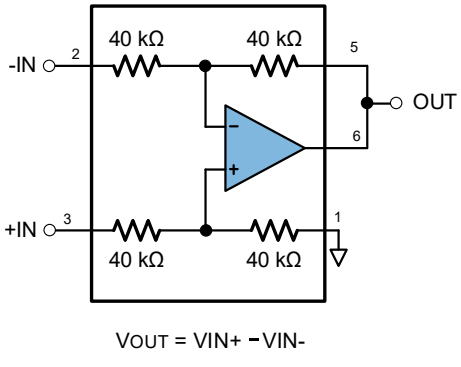


Figure 40. Difference Amplifier, Gain = 1

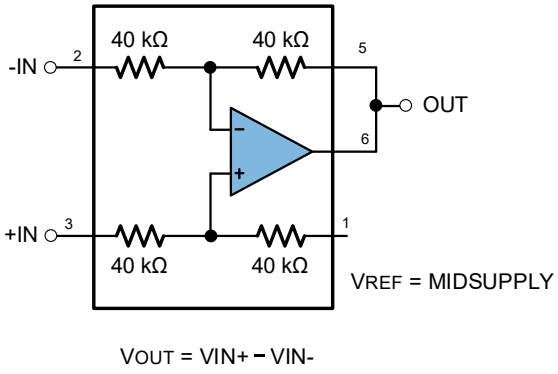


Figure 41. Difference Amplifier, Gain = 1, Referenced to Midsupply

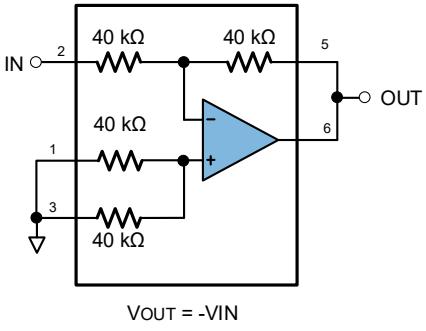


Figure 42. Inverting Amplifier, Gain = -1

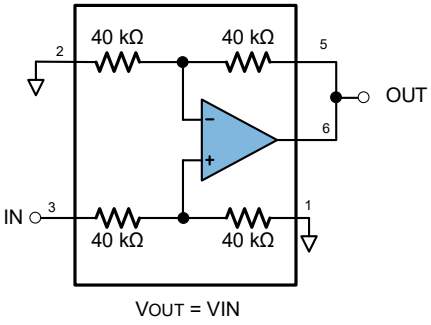


Figure 43. Noninverting Amplifier, Gain = 1

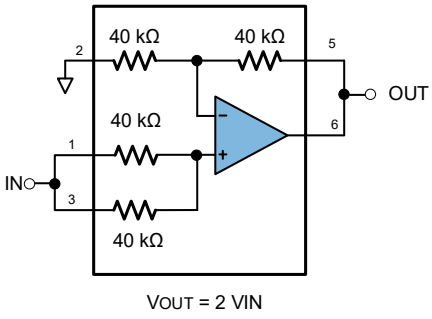


Figure 44. Noninverting Amplifier, Gain = 2

Differential Output

Certain systems require a differential signal for improved performance, such as the inputs to differential analog-to-digital converters. Figure 45 shows how the ZJA3676/ZJA3677 can be used to convert a single-ended output from an ZJA3601 instrumentation amplifier into a differential signal. The internal matched resistors of the ZJA3676 at the inverting input maximize gain accuracy while generating a differential signal. The resistors at the noninverting input can be used as a divider to set and track the common-mode voltage accurately to midsupply, especially when running on a single supply or in an environment where the supply fluctuates. The resistors at the noninverting input can also be shorted and set to any appropriate bias voltage. Note that the V_{BIAS} = V_{CM} node indicated in Figure 45 is internal to the ZJA3676 because it is not pinned out, meaning that there is no direct connection to the inputs of the amplifier. Figure 45 represents a differential output amplifier configuration with the use of +OUT and -OUT.

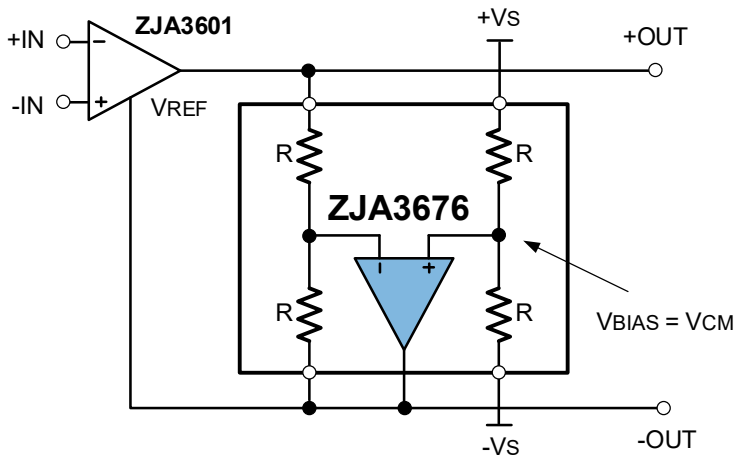


Figure 45. Differential Output with Supply Tracking on Common-Mode Voltage Reference

The differential output voltage and common-mode voltage is shown in the following equations:

$$V_{DIFF\_OUT} = V_{+OUT} - V_{-OUT}$$

$$= GAIN(ZJA3601) \cdot (V_{+IN} - V_{-IN})$$

$$V_{CM} = \frac{+V_S - (-V_S)}{2} = V_{BIAS}$$

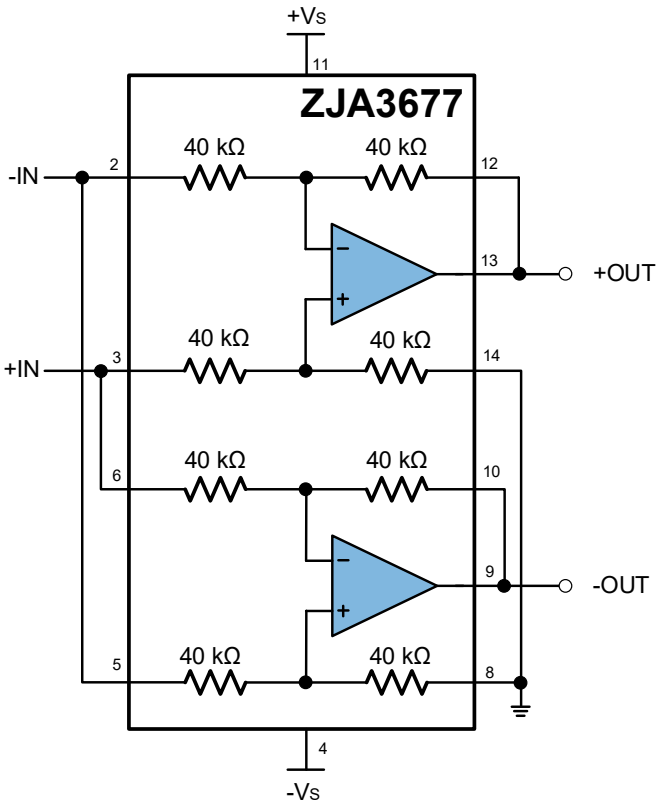


Figure 46. ZJA3677 Differential Output Configuration

The two difference amplifiers of the ZJA3677 can be configured to provide a differential output, as shown in Figure 46. This differential output configuration is suitable for various applications. The differential output voltage has a gain of 2 as shown in the following equation:

$$V_{DIFF\_OUT} = V_{+OUT} - V_{-OUT} = 2 \cdot (V_{+IN} - V_{-IN})$$

Current Source

The ZJA3676 difference amplifier can be implemented as part of a voltage to current converter or a precision constant current source, as shown in Figure 47. Using an integrated precision solution such as the ZJA3676/ZJA3677 provides several advantages over a discrete solution, including space-saving, improved gain accuracy, and temperature drift. The internal resistors are tightly matched to minimize error and temperature drift. If the external resistors, R_1 and R_2, are not well matched, they become a significant source of error in the system. Therefore, precision resistors or ZJM5491-1 are recommended to maintain performance. The ZJR1004-9 provides a precision voltage reference that also reduces error in the signal chain.

The ZJA3676 has rail-to-rail output capability that allows higher current outputs.

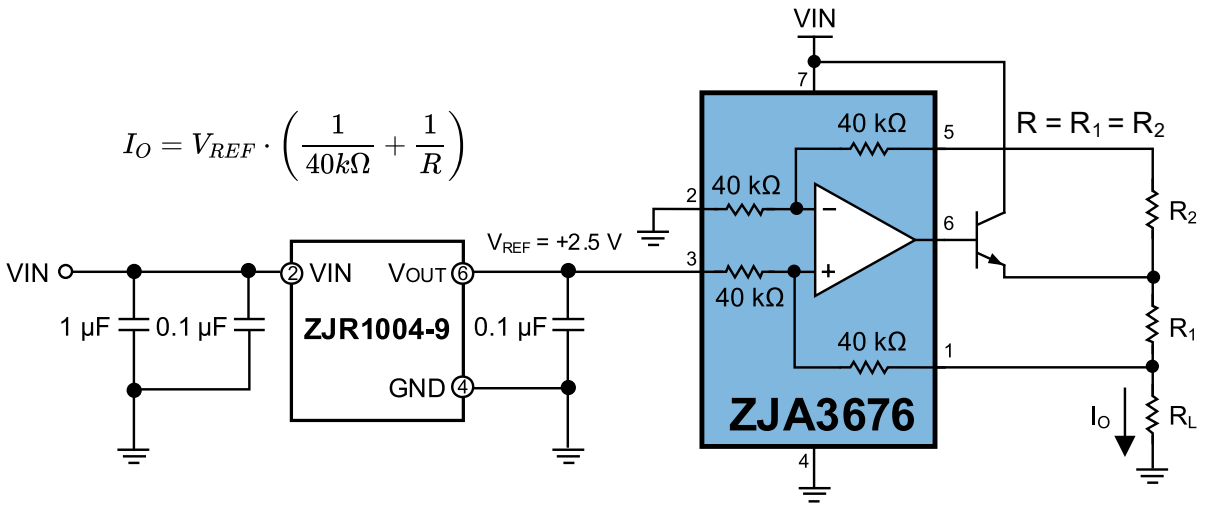


Figure 47. Building Constant Current Source by ZJR1004 and ZJA3676

Voltage and Current Monitoring

Voltage and current monitoring are critical in the following applications: power line protection, motor control applications, and battery monitoring. The ZJA3676/ZJA3677 can be used to monitor voltages and currents in a system especially the sensor interface is differential and following signal conditioning is in single-ended, as shown in Figure 48

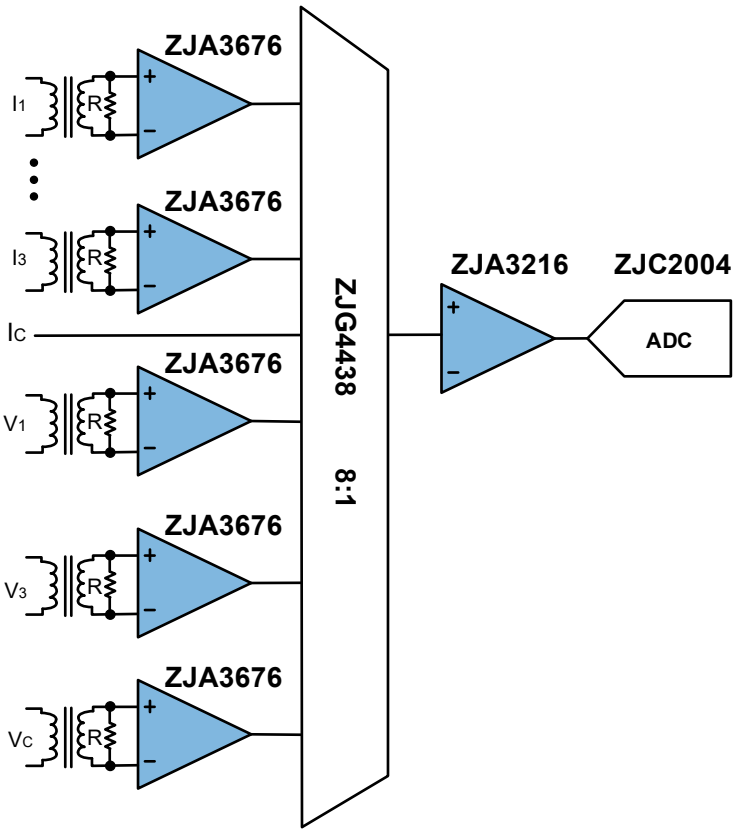


Figure 48. Voltage and Current Monitoring in 3-Phase Power Line Protection Using the ZJA3676

Figure 48 shows an example of how the ZJA3676 can be used to monitor voltage and current on a 3-phase power supply. I_1 through I_3 are the currents to be monitored, and V_1 through V_3 are the voltages to be monitored on each phase. I_C and V_C are the common or zero

lines. Couplers or transformers interface the power lines to the front-end circuitry and provide attenuation, isolation, and protection. On the current monitoring side, current transformers (CTs) step down the power line current and isolate the front-end circuitry from the high voltage and high current lines. Across the inputs of each difference amplifier is a shunt resistor that converts the coupled current into a voltage. The value of the resistor is determined by the characteristics of the coupler or transformer and desired input voltage ranges to the ZJA3676. On the voltage monitoring side, potential transformers (PTs) are used to provide coupling and galvanic isolation. The ZJA3676 helps to build a robust system because it allows input voltages that are almost double its supply voltage, while providing additional input protection in the form of the integrated ESD diodes.

Not only does the ZJA3676/ZJA3677 monitor the voltage and currents on the power lines, the ZJA3676 is able to reject very high common-mode voltages that may appear at the inputs. The ZJA3676 also performs the differential to single-ended conversion on the input voltages. The 80 kΩ differential input impedance that the ZJA3676 presents is high enough that it does not load the input signals.

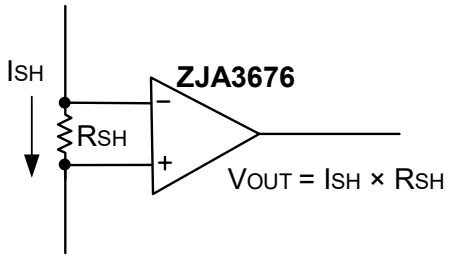
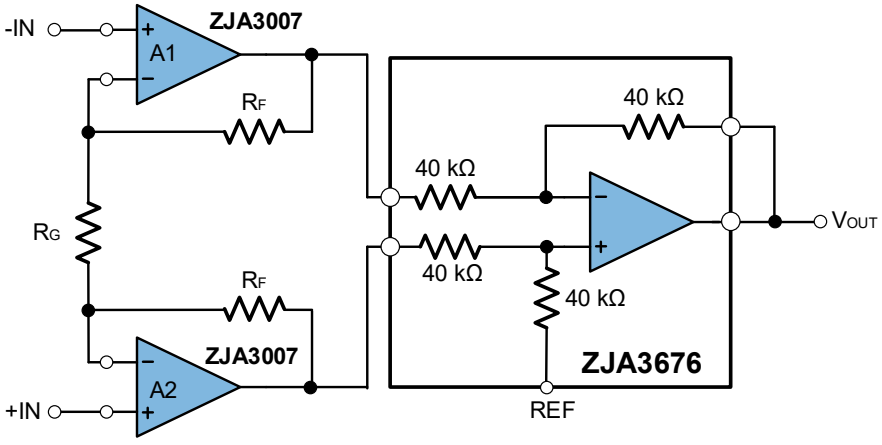


Figure 49. ZJA3676 Monitoring Current Through a Shunt Resistor

Figure 49 shows how the ZJA3676 can be used to monitor the current through a small shunt resistor (R_{SH}), which is useful in applications such as motor control and battery monitoring. ZJA3676's high precision and exceptional CMRR delivers the system accuracy.

Building Instrumentation Amplifier

The ZJA3676 can be used as building blocks for a low power, low cost instrumentation amplifier. An instrumentation amplifier provides high impedance inputs and delivers high CMRR.



$$V_{OUT} = \left(1 + 2\frac{R_F}{R_G}\right)(V_{+IN} - V_{-IN})$$

Figure 50. Building Low Power Precision Instrumentation Amplifier by ZJA3007 and ZJA3676

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible in order to minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

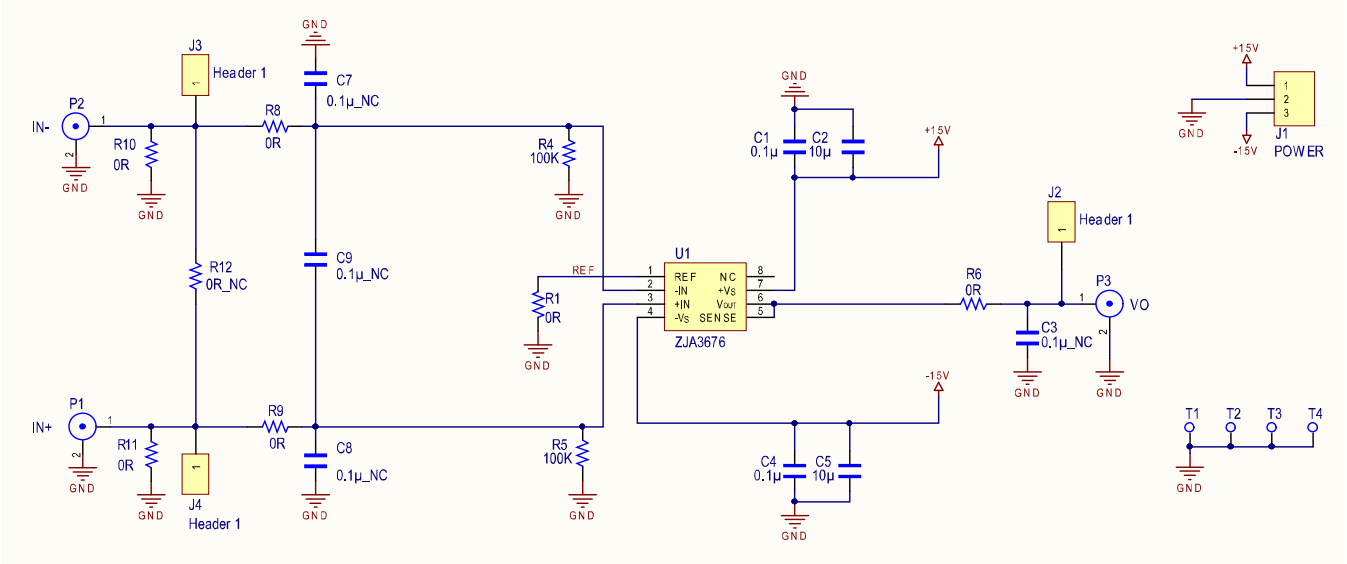


Figure 51. ZJA3676 Evaluation Board Schematic

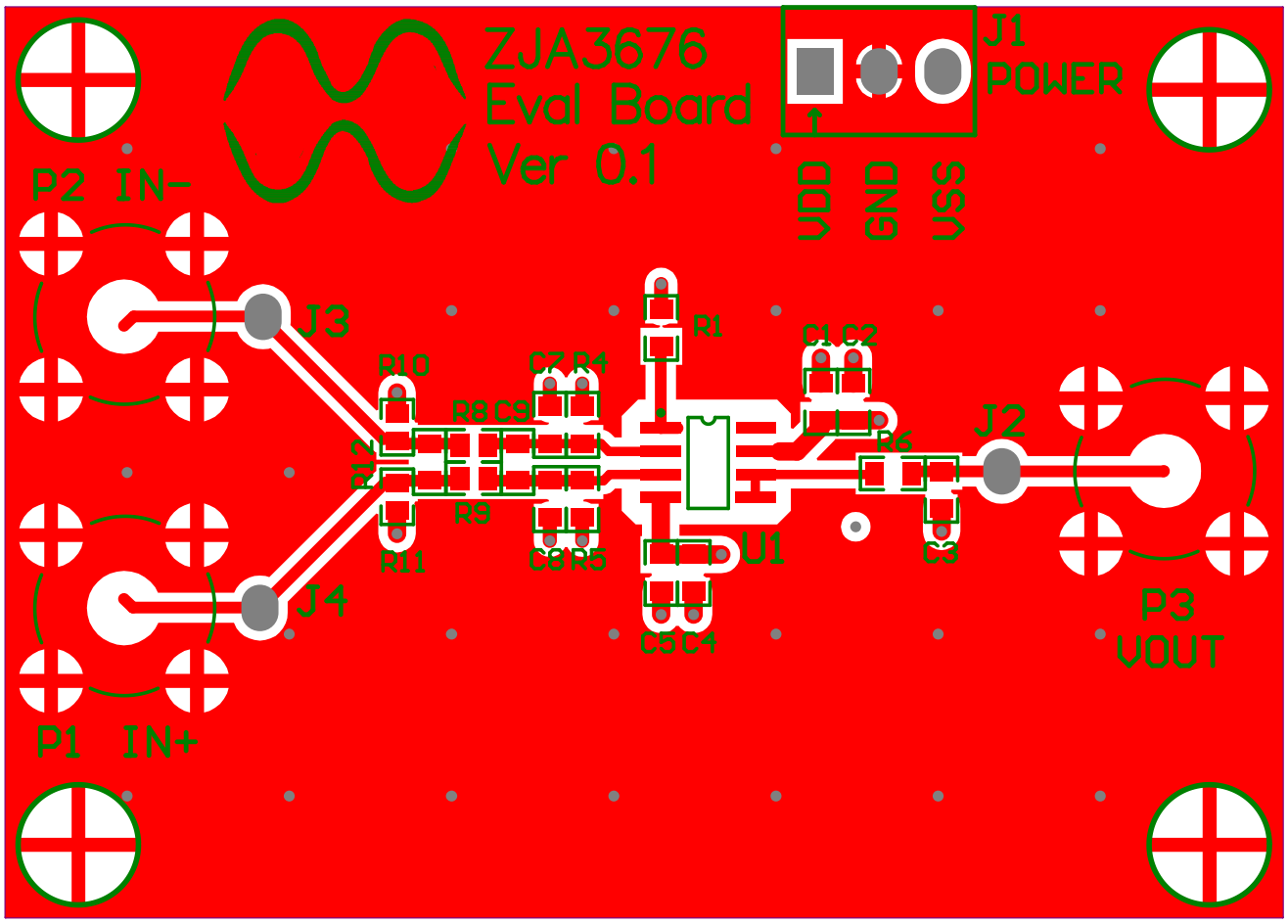


Figure 52. Layout of ZJA3676 Evaluation Board (Top Layer)

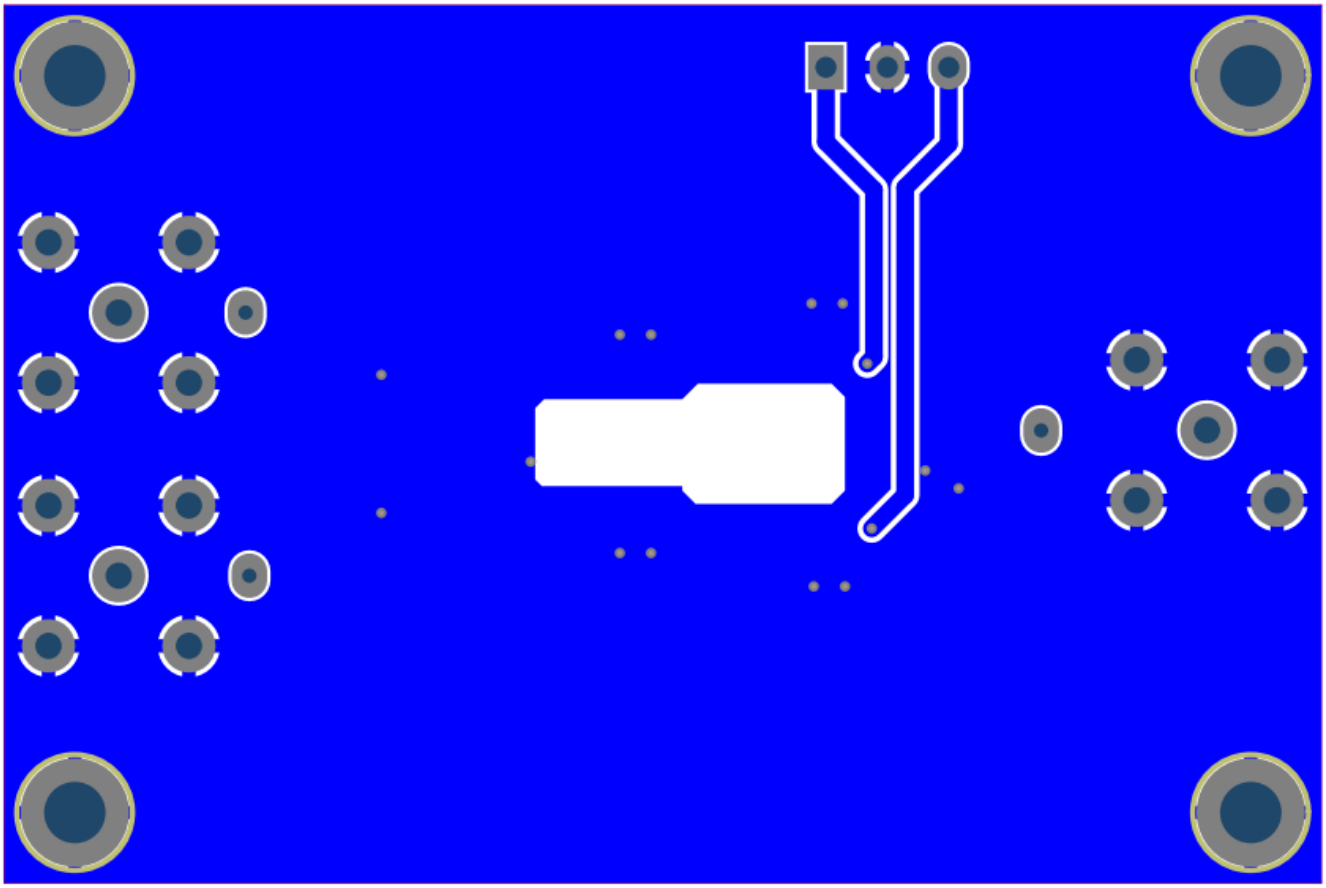


Figure 53. Layout of ZJA3676 Evaluation Board (Bottom Layer)

Outline Dimensions

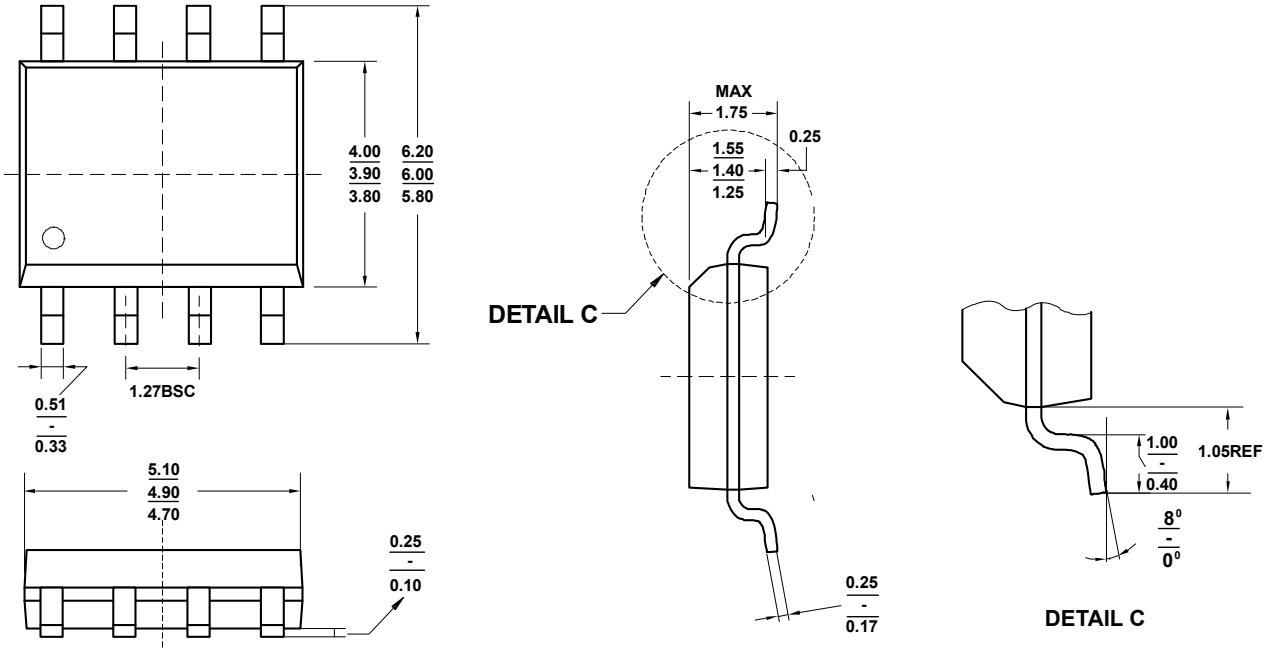


Figure 54. 8-Lead SOIC Package Dimensions shown in millimeters

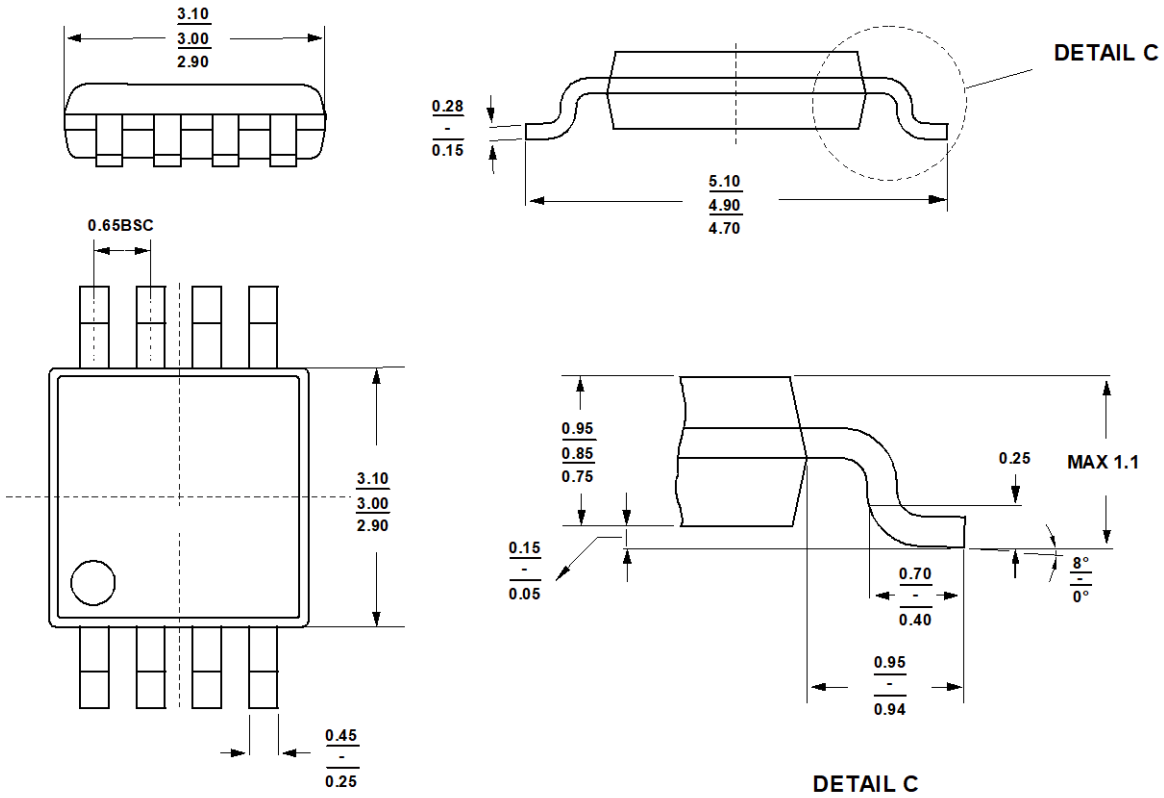


Figure 55. 8-Lead MSOP Package Dimensions shown in millimeters

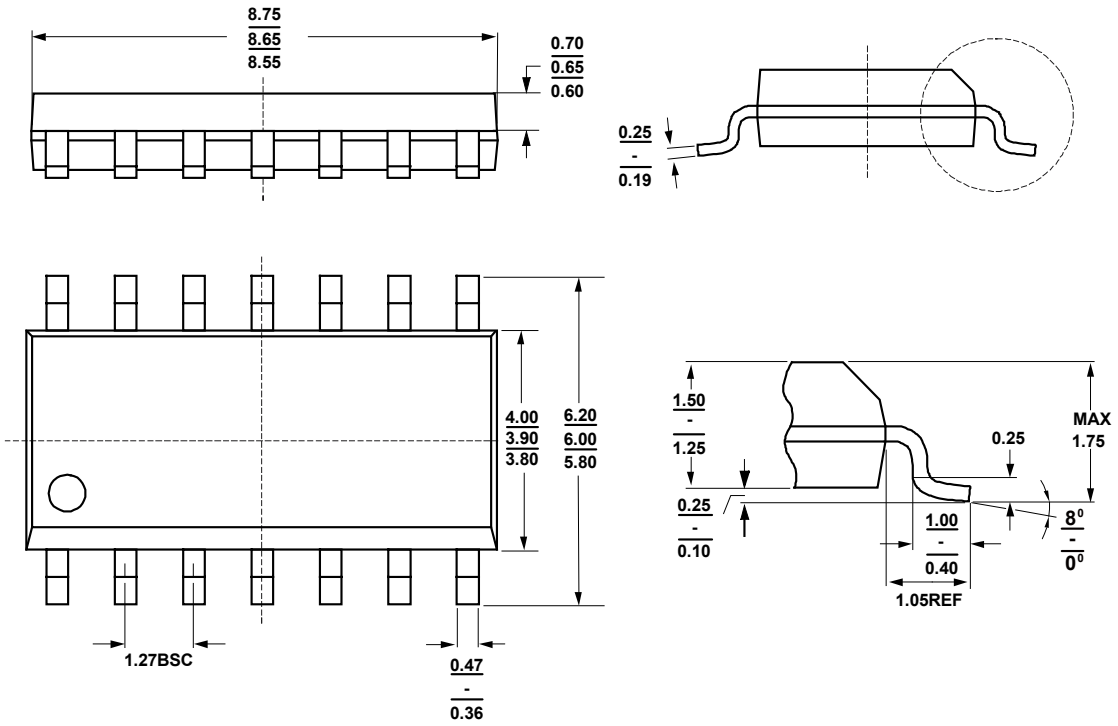


Figure 56. 14-Lead SOIC Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Vos max. (μV)	Package	External Package
ZJA3676	ZJA3676BSABT	100	SOIC-8	Tube
	ZJA3676BSABR			13” reel
	ZJA3676ASABT	300	SOIC-8	Tube
	ZJA3676ASABR			13” reel
	ZJA3676BUABT	100	MSOP-8	Tube
	ZJA3676BUABR			13” reel
	ZJA3676AUABT	300	MSOP-8	Tube
	ZJA3676AUABR			13” reel
ZJA3677	ZJA3677BSDBT	100	SOIC-14	Tube
	ZJA3677BSDBR			13” reel
	ZJA3677ASDBT	300	SOIC-14	Tube
	ZJA3677ASDBR			13” reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT23; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV